



VLSI TECHNOLOGY, INC.

**APPLICATION
SPECIFIC LOGIC
PRODUCTS
DATA BOOK**

1988

Application Specific
Logic Products Division

\$10.00



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DATA BOOK

This data book presents a complete technical description of the VLSI Technology, Inc. Application Specific Logic Products Division product line. Where devices have been fully characterized, either by VLSI Technology or by one of its partners, specific information is presented in the form of data sheets. Information on partially characterized devices, devices currently under development, or devices that have their own Users Manuals containing data sheets, is in the form of product briefs. More complete data can be obtained on any device from the Logic Products Division Applications Department.

In order to facilitate computer generation of this data book, overbars (i.e. \overline{CS}) have been replaced by a preceding minus sign (i.e. $-CS$) on all new or recently revised data sheets. Older data sheets will retain their overbars until a major revision is performed.

GENERAL

The primary business objective of VLSI Technology, Inc., (VLSI) is to provide systems designers with total application-specific integrated circuit (ASIC) solutions. To accomplish this, it has created a unique blend of expert design tools, leading-edge process technologies, state-of-the-art fabrication facilities, and a wide range of products, including a variety of "catalog" devices.

The Application Specific Logic Products Division of VLSI Technology is respon-

sible for the manufacture and marketing of a diverse logic-based product line that encompasses both innovative and proven, well established catalog devices. This line includes microprocessors and coprocessors, peripheral circuits, and products for data communications and telecommunications applications.

Unlike other suppliers of such devices, however, VLSI is also a recognized leader in ASICs. As such, it not only possesses the design, process, and fabrication capabilities necessary to produce the highest-quality off-the-shelf components, but is also able to treat its logic products as an integral part of a complete solution. One of the primary vehicles for accomplishing this is the megacell; the functions represented by individual devices can be implemented as megacells in VLSI's software libraries and used for semicustom circuit design and functions developed as megacells for specific applications can be turned into catalog products.

MEGACELLS

The megacell is a relatively new concept in the world of IC and system design. As such ASIC companies as VLSI offer better tools for IC design, simulation, and testing, it becomes necessary for systems manufacturers to design custom ICs to keep up with their competition. Megacells help decrease design time by providing large building blocks that are equivalents of standard off-the-shelf products. By using

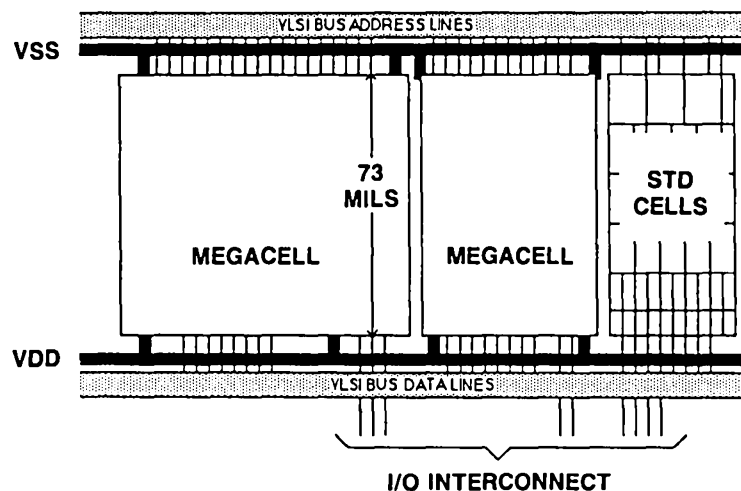
megacells and VLSI's design tools, manufacturers can have a custom IC design capability without all of the normal custom development costs.

The VLSI Technology family of megacells represents commonly used peripherals that are good candidates for integration as parts of customer-driven designs, which can be either customer-specific or market-specific. In customer-specific designs, it is possible, for example, to combine these integration elements with other megacells and logic to become single-chip equivalents of computer systems that are already in production. This increased level of integration provides cost and space reduction that can keep the system designs competitive. In a market-specific design, upward-compatible enhancements that meet the needs of many customers can be added and the device offered as a new standard product.

VLSI's megacells are designed to have a fixed height and variable widths, offering the best trade-off between unusable internal space and placement ease. As shown in Figure 1, they can be configured to make a very dense final design with a minimum of wasted silicon real estate.

Of equal importance with the physical layout format of the cells is the structure of the interconnect bus. This bus must be generic enough to allow a wide variety of functions to be connected

FIGURE 1. VLSI TECHNOLOGY MEGACELLS ARE OF A FIXED HEIGHT, WITH VARIABLE WIDTHS



uniformly and efficiently, and must be fast enough to not itself become a limiting factor as system performance increases.

The internal structure of the bus created by VLSI for use with its megacells contains an m-bit data bus and an n-bit address bus, both of which are expandable in width to accommodate changes in system requirements. The bus operates synchronously at a rate of 3 million transfers a second, which is equivalent to the performance of a 10 MHz 8086 or 12 MHz 68000 microprocessor. The bus definition allows for internal access times of 50 ns and cycle times in the 200 ns range. With standard pad drivers, external loads can be driven while supporting a 3 MHz bus frequency; faster speeds can be obtained by using faster pad drivers. To create a standard product from a megacell, an interface circuit is incorporated that exactly matches the slower timing of the external bus to the internal bus.

MEGACELL-BASED DESIGN RATIONALE

There are many reasons why megacells make sense for new designs, including reduced board space, lower power, increased reliability and reduced design times.

Typical applications that can benefit from the use of megacells are those that contain three or four LSI components and a handful of "glue" components. All of these components can be combined into a single component if the functions can be partitioned into logical groups with a reasonable number of I/O pins. In this type of application, the total pin count might be reduced from 300 pins for a discrete solution to less than 100 pins, and the circuit board area reduced from approximately 20 square inches to 2 square inches.

The power consumption of megacell designs can be very small in comparison with the HMOS designs they replace, since all of the VLSI Technology megacell family is implemented in high speed, low power, two-micron CMOS technology. In addition, because several functions can be put on one piece of silicon, the interconnect capacitance and inductances are minimized, thereby reducing the power to a fraction of what

was needed in previous designs.

The reliability of a megacell-based design is typically better than the collection of discrete components it replaces because there are fewer pins, fewer bonding wires and lower total power consumption. In most systems, the largest contributor to reliability problems is IC pin connections, with such other factors as die temperature and die size being secondary. The more functional blocks that can be combined on a single piece of silicon, the fewer the number of interconnections that have to be bonded to package pins, resulting in higher overall reliability of the component and system using it.

Since megacells can be used as high level building blocks, overall design times can be reduced significantly by taking existing designs using standard products and integrating additional support logic directly onto the chip. An example of this technique would be the integration of a VL68C45 CRT controller with a memory interface and video shift registers to form a single-chip video adapter. An additional option might be to include character ROMs or RAM arrays, although the addition of these commodity components is not always cost effective.

CURRENT FAMILY OF MEGACELLS

Megacells are designed by very carefully studying the data sheets and systems implementations of the original part vendors, but an important part of validating a megacell design is to subject it to many different hardware and software environments. Only after a part has been tested in several applications can a vendor feel confident that the megacell exactly emulates the original function, including all of the undocumented "features". The VLSI Technology philosophy is to offer members of the megacell family as standard products as well as cells so that this validation can take place very quickly after the introduction of the standard product. Since customer-specific design times typically take from two to four months, megacell designs can be started before the standard product validation has been done. This lead time allows customers to get a head start introducing designs.

DESIGNING A CIRCUIT USING MEGACELLS

The design process is started by using a megacell schematic "icon" as part of the schematic entry of the user's design. Provided with the megacell icon is a data sheet detailing the internal timing requirements of the megacell. The designer works from this data sheet as if using an off-the-shelf standard product, except that the logic and timing of the bus are somewhat easier to use.

USING VTitest DURING THE DESIGN PHASE

When the schematic entry of the design is complete, the designer uses a test language assistance program (VTitest) to capture a set of simulation vectors that can be used to test the design after silicon has arrived. Once the designer is satisfied that the vector set is sufficient to cover all possible stuck faults, a final test program can be compiled through this program. The output from this program is a test program containing SETF statements that can be easily moved onto an industry-standard tester, such as a Sentry tester system.

ADDITIONAL LOGIC FOR TEST SIMPLIFICATION

In all cases, some additional logic will be necessary to facilitate testing the megacells. This additional logic consists of multiplexers on pins to allow all of the connections of the megacell to be accessed from the periphery of the circuit. This dictates that all designs be contained in packages having at least as many pins as the most pin-intensive megacell used internally. To enable the test mode, an illegal condition on the interface is often used, such as Read Strobe and Write Strobe being asserted together while the chip is selected. This would normally never occur in an application, so it is a safe combination to use. When enabled, the I/O pads of a specific megacell are connected to the I/O pins of the component, and the standard product test program run to verify the functionality of the core.

USING VTitest SOFTWARE TO HELP CREATE TEST PROGRAMS

VTitest is a software package that eliminates the need for the design engineer to be an expert in testers and testing. The designer works in a test language called

VLSI Test Language (VTL), which allows simultaneous development of the circuit design and test program, providing notification early in the design stages of when tester-specific details affect the testability of the design. Through the test language, designers can create a file describing the physical characteristics, timing, stimulus patterns and expected responses of a circuit under development (Figure 2). The remaining software translates the description into commands that run the simulation, verify the expected response, and store requested response values predicted from a simulator. Finally, VTltest generates a complete test program that includes all specifications for the timing generators, strobes, and registers, all pattern loading, requested dc parametric and summary test routines, and the test vectors needed to test the circuit functionality.

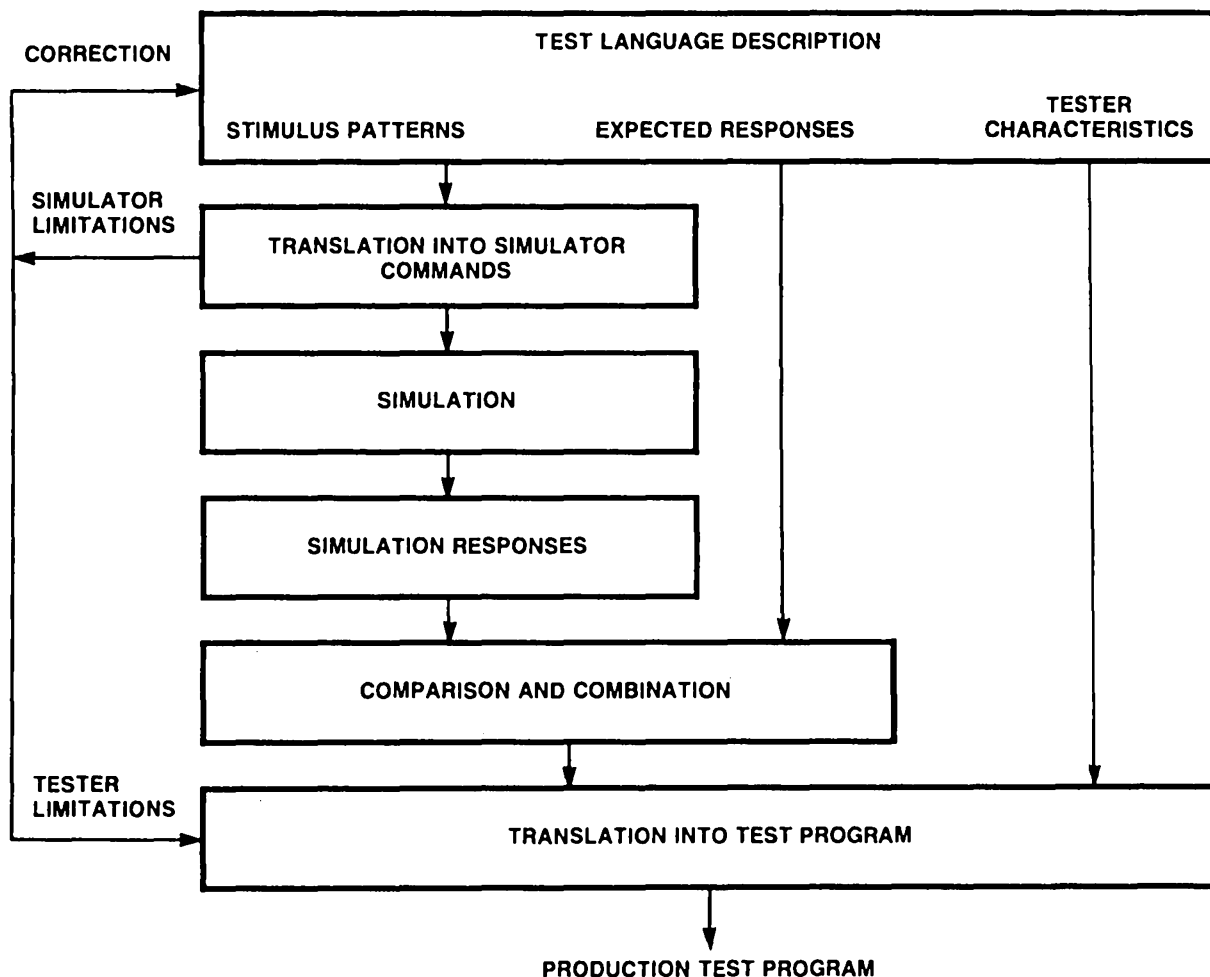
Besides identifying tester limitations associated with the test program, the software suggests ways to work around them. In that way, design engineers can become familiar with tester limitations and make the optimum design-vs-testing trade-off. When the testability of a circuit becomes a problem, the design engineer can add additional circuitry to help out. Common practice is to break up long counter strings to reduce the number of states required to exercise each individual stage.

The test vectors generated by the software have a one-to-one correspondence with the vectors used during the simulation, so the information normally lost during post-processing is retained. Another benefit is that, since a tester is not needed to develop the test program and initially debug it, the test system is available for production time and work can be done during normal hours.

To interface with specific testers, the software needs routines that contain tester-specific information. These routines also identify portions of the test or simulation language description that can not be executed by the tester, simplifying the task of making portable test software. Interface routines are currently written in Xidak's Mainsail language for both VLSI's simulator and the Sentry Series 7, 10, and 20 testers.

When defining an IC, designers can define the stimuli and the expected responses through the test language, creating modules that describe aspects of the circuit's functions or dc test conditions. The resulting circuit description contains a complete set of operational parameters, all information necessary to create a data sheet is present. Since that information actually drives the simulator and develops the test program, it always remains up-to-date.

FIGURE 2. THE STRUCTUE OF THE VLSI TECHNOLOGY TEST LANGUAGE MAKES TEST PROGRAM GENERATION SIMPLE AND STRAIGHT-FORWARD



DEFINING THE TEST PROGRAM FLOW

Several types of software modules are required to create a complete test description. Designers use the first module, MAIN, both to describe the overall flow of the test and to initialize the test software for execution. The contents of the MAIN module declare the duration of a test, select the required parameter modules, and specify their order of execution. The MAIN module partitions the testing into a number of steps that can be easily understood from a high level.

The DURATION statement determines the length of the tester cycle, and normal-time selects the timing parameter module of that name. The WRITE commands place remarks in the test program file for documentation purposes.

The physical characteristics of the IC are defined through the pin definition (PINDEF) module, which contains a declaration of the number of circuit pins and statements that the test software uses to identify pins during testing. Those pin definition statements also define pin type (input, output, bidirectional, power, etc.). In addition, the module may define the device type and state whether it is static or dynamic. Labels for each element of the pin list can specify such pin types as input, output, bidirectional, power ground, three-state, open-drain, open-source, or no connection.

Minimum, nominal, and maximum timing parameters are defined in the TIMEPARAM module. Designers can test the circuit under different timing conditions by defining multiple modules and assigning each module its own identifier.

An additional module, EDGETIME, creates transition edges using the parameters defined by TIMEPARAM. These edges determine when the stimulus values are placed on the input pins and when the response values are measured during each test cycle, indicating such timing points as when outputs should be sampled and when inputs should be changed. For example, to create a clock that remains low for 80 ns, high for 100 ns, and repeats every 200 ns would require the definition of four edges. The first edge would be at 0 ns, the second at 80 ns, the third at 180

ns, and the fourth at 200 ns. The last edge defines the period of the cycle and is also used for the duration declaration.

For each test cycle, the CYCLE module describes the stimulus for input pins and the response for output pins. If parameter values are included within parentheses in the module heading, a variety of values can be placed on the input pins. Each time the module is called, the appropriate values are passed to it. This module takes transition edges from the EDGETIME module and determines when to apply stimulus values to the I/O pins and when to measure outputs during each test cycle. CYCLE statements in the modules specify whether a specific pin is to be stimulated or measured. A transition edge at a pin may be specified by "@" time. If not specified, the stimulus values are placed on the pin at the beginning of the cycle and the responses are measured at the end of the cycle.

With FUNCTIONTEST modules, the designer partitions the test into functional blocks or initialization procedures, particularly if the sections are to be used more than one. The first DCPARAM statement sets the minimum and maximum measurement values as well as the source that creates them (current or voltage). Defaults are provided if exact values have not been selected. An important attribute of this module is that some portions can be used more than once. These modules are executed when called by the MAIN routine or other FUNCTIONTEST routines. They may contain WHILE and other looping constructs to provide a means of conditionally executing statements.

SIMULATION AND TEST PROGRAM GENERATION

As the software generates the test program, it draws on the stimulus and response values to select each pin's timing generators and strobes on the basis of the value of the pin before the cycle starts, the number of transitions occurring on the pin during the cycle, and if the pin is to be an input or output during the cycle.

The selection of mask register is determined by the state of the registers at the start of the cycle and the pins that have been activated during the cycle. The appropriate values are inserted into

a test vector, which is stored in a vector file with the register set or enabling commands. Before storing the test vector, the software attempts to take advantage of any vector compaction capability of the tester.

After the test language is used to create the modules, the resulting description file is loaded into VLSItest, which parsing, the software creates a data base from the physical characteristics described in the PINDEF module and from the identifiers used throughout the circuit description. After the program is properly compiled, testing may begin.

The test language itself possesses all the power and flexibility needed to efficiently develop test programs. All variables and constants are 32-bit values that may be manipulated on a bit-by-bit basis by a variety of familiar operators, such as AND, OR, and XOR. Additionally, the language's looping constructs present a compact means of conditionally executing a series of tests.

COMPLETING THE DESIGN

Test engineering effort is still required when using this process, but the time spent can be a matter of only a few weeks, rather than the several-week period traditionally associated with creating a test program for a new product.

When simulation is complete and the design works satisfactorily, the layout process can begin. In most cases, designers are interested in minimizing design time and associated costs, so they pick standard cells for the additional blocks of logic that will surround the megacell cores. Cells are individually compiled, placed and routed to create blocks of logic until the entire non-megacell portion of the design is complete. For the best layout efficiency, the additional logic is either put into a block having the same height as a megacell, or it is put around the megacells to fill in the voids. When each portion of the design is completed, these blocks can be placed and interconnected using a tool call VLSICOMPOSE, which is a top level composition editor. This editor assists in interconnecting blocks of cells and optimizing both the placement and interconnection of cells. The overall goal of placing blocks to form the chip is to get the ratio of the X and Y dimen-



sions (the aspect ratio) as close to 1:1 as possible. The resulting square die gives the packaging engineer the most flexibility in package selection.

When the entire layout process is complete, a netlist of interconnections is extracted from the physical data base to allow comparison of what was intended to be with what actually was implemented. Once the extraction is complete and the netlist comparison between schematic and layout is successful, the device can be resimulated in software with more accuracy, since values of expected capacitance are extracted along with the connectivity information.

Finally, the layout is checked for design rule violations using the design rule checker (DRC) program.

When all of this has been successfully completed, the data base is sent to a design center, where the actual physical layout of the megacells is included in the data base. When everything checks out properly, a mask set is created and silicon is started. From this point, the fabrication time typically takes 8 weeks for the first pass prototypes.

SUMMARY

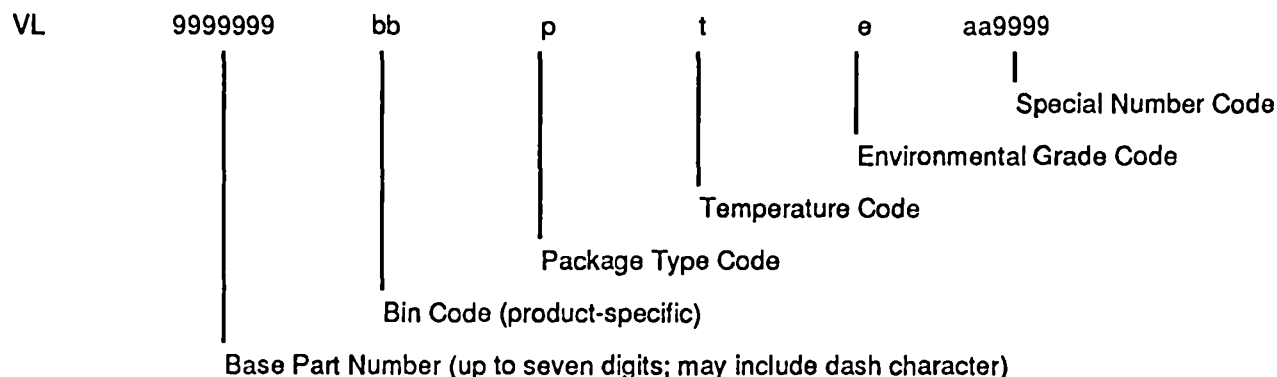
Megacells offer a way to quickly design chips that replace today's board level

function, while at the same time offering competitive costs, increased reliability, increased performance and reduced board space. The design process requires a wide range of design tools, including standard cells, cell compilers, simulators, routers, test program generators, and libraries of designs. VLSI Technology, Inc. specializes in offering these kinds of tools in addition to complete wafer services to provide a total solution to systems designers.

GENERAL

VLSI Technology, Inc., Logic Products devices are available in a variety of plastic and ceramic packages - including flatpacks, chip carriers, and pin grid arrays - and in different temperature ranges. Specific information on the packages and temperature ranges for particular devices is coded into the part number portion of the order information included in each data sheet.

This information is organized as:



SPECIAL NUMBER CODE

RC9999 is a ROM code number.
 SL9999 is a special lead number
 SM9999 is a special marketing number.
 SS9999 is a special specification number.

ST9999 is a special test number.

ENVIRONMENTAL GRADE CODE

Blank (no entry) = information is not applicable.
 I = a 48-hour dynamic burn-in.

TEMPERATURE CODE

C = 0°C to +70°C (commercial operating temperature range).
 I = -40°C to +85°C (industrial operating temperature range).
 M = -55°C to +125°C (military operating temperature range).

PACKAGE TYPE CODE

C = ceramic side-brazed dual in-line package (ceramic DIP).
 D = cerdip.
 F = flatpack.
 G = ceramic pin grid array (PGA).
 L = JEDEC type-B leadless chip carrier (LCC).
 P = plastic dual in-line package (plastic DIP).
 Q = plastic leaded chip carrier (PLCC).

The package forms indicated by the codes are illustrated in the outline drawings contained within this section.

PART NUMBER EXAMPLE

The part number VL68C45R-23PC SS0001 would indicate a CMOS revision R version of the 6845 CRT controller having a 2 MHz bus clock and a 3 MHz character clock, housed in a plastic DIP, operating over the commercial temperature range, and tested to a special specification (#0001).

**PACKAGE CONSIDERATIONS
DUAL IN-LINE PACKAGES**

The dual in-line package (DIP) has been in high-volume production for nearly twenty years, and is estimated to have been the package of choice for over 80% of all integrated circuits shipped in 1985. Some 1986 usage estimates are as high as 18 billion units worldwide. Generally, devices in DIPs can be purchased in two types of ceramic (cerdip and side-brazed) and in the very-familiar molded plastic package. Over 85% of all DIPs, or over 12 billion, sold worldwide in 1985 were plastic.

The ceramic side-brazed package is relatively expensive and is frequently imported. It has excellent mechanical characteristics, including the ability to survive extreme temperatures, salt water, and corrosive atmospheres. However, as the cost of the integrated circuit it houses becomes less and less expensive, the relative cost of the ceramic DIP becomes a major concern. In a large number of applications, this package is several times more expensive than the chip within it. As would be expected, this package is very popular in military electronics and in other potentially harsh mechanical environments. The side-brazed package, while representing less than 2% of all DIP packages shipped in 1985, represents a higher percentage of DIP revenue, due to its comparatively high average selling price (ASP).

The cerdip is a "sandwich" of two ceramic parts that are joined together by a cement-like epoxy. The die itself is mounted on a lead frame, and enjoys many of the cost economies associated with this approach. The cerdip has some of the mechanical advantages of the side-brazed ceramic at a lower cost. The cerdip represented about 14% of all DIP shipments in 1985.

The plastic DIP has been the catalyst for the computer revolution. The dramatic reduction in the cost of microprocessors, microprocessor peripherals, communications devices, and memories has been passed along to the manufacturers and the final users because plastic

packaging has remained extremely inexpensive. In addition, reliable automated 16-pin and 14-pin DIP insertion equipment has dramatically reduced manual "board stuffing" costs of DIPs. The plastic DIP itself is easy to manufacture. The die is mounted on a copper-alloy lead frame and the plastic material is molded around it. It is usually branded by a printing method with an epoxy-based ink but, recently, laser-scribing the number into the plastic body is gaining popularity, reducing costs even further.

Mechanically, the DIP has proven to be an extremely utilitarian package in most applications. Its short, stiff leads on 2.54 mm (0.1 inch, or 100 mil) centers allow reasonably easy insertion for both test and production by both manual and automatic techniques. While more expensive DIPs are placed in sockets, the overwhelming majority are soldered directly into the printed circuit board. The 64-pin DIP, the largest DIP in high-volume production, is used to house VLSI's VL2010 and VL2044 Multiplier/Accumulators. DIP configurations with higher pin counts tend to exhibit unacceptable mechanical problems, such as extremely high insertion and extraction forces.

DIPs are available, in even-pin-count steps, in packages as low as two pins. A variation of the DIP that has gained some acceptance is the SIP, or single in-line package. The SIP, mounted lying on its edge, uses very little printed circuit board space and frequently contains a number of memory die in high-density memory applications. However, as desirable as the SIP may seem, it is not the major evolutionary path of the DIP. The SIP allows little air circulation for cooling, is hard to handle, and is not generally accepted as a standard. The DIP evolution lies in surface mounting the device.

**SMALL-OUTLINE
INTEGRATED CIRCUITS**

The small-outline integrated circuit (SOIC) is a descendant of the DIP. Sometimes called the "Swiss" outline integrated circuit in honor of its

country of origin, this package solves many of the problems of the DIP, while retaining many of its advantages. The gull-wing lead rests on top of the printed circuit board rather than going through it. For most types, its leads are exactly half the length that the DIP's are, and it maintains the same basic rectangular package aspect ratio of the DIP. This, however, becomes a disadvantage in high-pin-count applications. For more than 28 pins, many designers prefer the square aspect of the plastic leaded chip carrier (PLCC) to the SOIC. The small package mass of the SOIC does not allow the same thermal dissipation that can be expected in a standard DIP, which becomes a minor problem as more chips are made in the generally lower power consuming CMOS process. Most importantly, the SOIC consumes only about 30% of the real estate consumed by the standard DIP. It is estimated that nearly 1.5 billion SOIC units will be shipped in 1986.

CHIP CARRIERS

Chip carriers have been around for several years in various forms, and are just now coming into widespread usage. Generally, the terminal spacing of chip carriers is 1.27 mm (50 mils), but several special types have 1.0 mm (40 mil) spacing for use by companies engaged in the pocket pager business. Some variations are available in 0.64 mm (25 mils) also. The ceramic versions of chip carriers have become very popular in military applications for the same reason the ceramic side-brazed DIP has: their mechanical ruggedness. Frequently, ceramic leadless chip carriers (LCCs) are soldered in; others use connectors, while still others have their own leads and are inserted as a leaded device. Due to the dissimilar coefficient of expansion of materials (package alumina and printed circuit board fiberglass) and the lack of pins on the leadless versions to provide flexibility or compliance, the ceramic leadless chip carriers should be soldered to a material that has the same thermal expansion characteristics as they have. This has become very popular

in military applications where weight and space are at a premium and, generally, cost is not the primary consideration.

The plastic leaded chip carrier (PLCC) has very quickly become the most popular of all the chip carriers. The PLCC represented about 61% of the chip carriers shipped in 1985 (approximately 400 million units). Although there is debate on the issue of board space consumption, the PLCC and SOIC consume about the same amount of board space in the 24- to 28-pin configurations. In lower pin count applications, the SOIC seems to be more space-effective; when over 24 pins or so, the PLCC seems to have the edge in most applications. In applications over 28 pins, the PLCC is the surface-mount package of choice. Its square aspect ratio allows many chip placements that the highly rectangular package of the SOIC does not. In addition, there are rectangular PLCCs to accommodate such rectangular die, such as memories.

CHIP-ON-BOARD MOUNTING

The ultimate in low-cost chip mounting is achieved by the chip-on-board (COB) technology, in which no discrete package is actually employed. The die is soldered onto a copper pad on a printed circuit board. Bonding wires connect the die to smaller bonding pads around the die. The die and wires are then covered by a dollop of epoxy. This technique, while inexpensive, is not

generally accepted in industrial or business equipment. It has been extensively employed in video game cartridges, and seems to work quite well there.

PIN GRID ARRAY

The pin grid array (PGA), or "bed of nails," has only been around for ten years, but had a usage of about 5 million in 1985, and its popularity is growing rapidly. This major package variation allows very high pin counts in relatively small spaces with excellent mechanical and thermal characteristics. The 149-pin VL82C389 Message Passing Co-processor (MPC) for Multibus® II systems is a prime example of PGA high-density trends. The major disadvantage of the PGA is its high cost. Virtually all of the 5 million PGA units shipped in 1985 were ceramic. Plastic pin grid arrays are well along in development, and will provide reliable, inexpensive packaging for the many high-pin-count ASIC, memory, and other circuits coming into wide usage.

FLATPACK

The flatpack holds less than 1% of the IC package market. True to its name, it is flat, small, and has flat leads usually in the same plane as the package body. It is generally harder to handle and test than the other package types, but provides a surface mounting alternative to the pin grid array in very-high-pin-count applications. It is usually surface

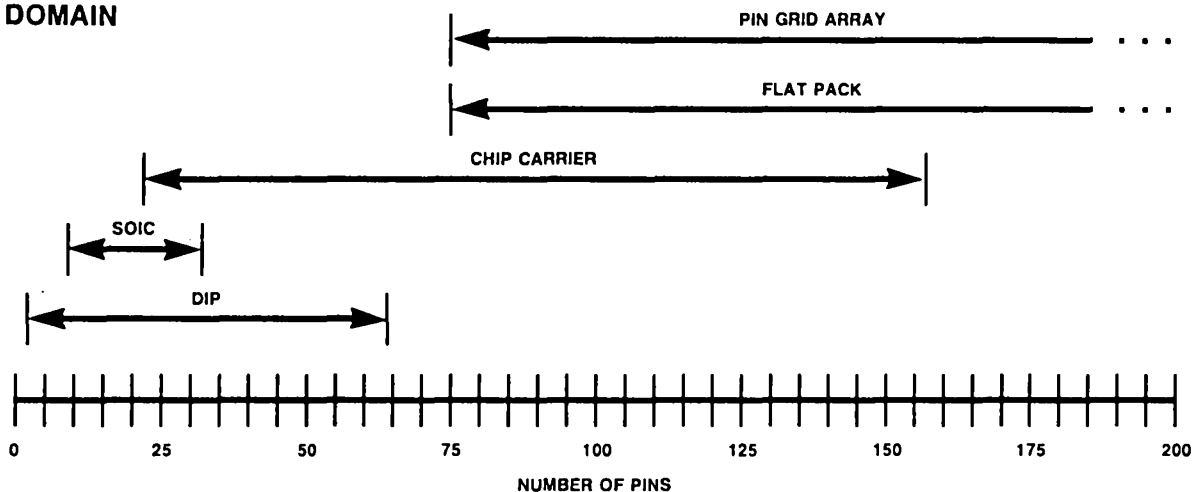
mounted, "socketed," or suspended through a cut-out hole in the printed circuit board.

SYSTEM CONSIDERATIONS

In the extremely competitive computer market that now exists, every repetitive cost, no matter how small, comes under close scrutiny. Drilling a hole in a printed circuit board costs about \$0.001, a fairly small amount until it is multiplied by the thousands of holes that frequently occur in each board. This becomes a significant consideration at the system level. Even though re-tooling costs are high, many companies are converting (some at least partially) to surface-mounting equipment. Surface mounting allows more chips in a much smaller area, but not all functions are yet available in surface-mount packages. Some companies have solved this problem by designing both through-the-board and surface-mount devices onto the same board. Others continue to use the older technology until they can re-tool for 100% surface mount.

Application-specific integrated circuits (ASICs) and their support devices are requiring packages with ever-increasing pin counts. The pin count domain diagram graphically depicts the typical domain of pin counts for five basic package types. While there is a good deal of overlap, chip carriers and pin grid arrays will become the package of choice in future systems containing devices of high pin count. Since the PGA device

PIN COUNT DOMAIN



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does not support surface-mount technology, chip carriers or flatpack technology will have to be implemented as pin counts exceed 170 using surface-mount systems.

CONCLUSION

There will be no panacea package that will exclude the use of all others in the future. While there are several criteria for the system designer,

Table 1 examines some of the characteristics of packages that will probably occupy the overwhelming majority of printed circuit boards in the future. Leadless chip carriers will be especially popular in military and harsh industrial applications. The DIP, with many billions already in use, will not disappear, but its percentage of market will decrease steadily. Pin grid arrays will remain

and increase in popularity as very large devices become more popular and plastic PGAs become readily available. Surface mounting is definitely a wave of the future for many systems. SOIC packaging will increase rapidly for devices of 28 terminals and under, while the mid-range and higher terminal count devices will be housed in PLCCs or flatpacks.

THERMAL CONSIDERATIONS

The devices in this data book have undergone thorough evaluation and characterization to ensure their operation over the specified temperature ranges. While safety margins are used for all parametric tests over the temperature range, the designer should not exceed the temperature limits, even for extremely short intervals. The following notes are presented to ensure a reliable, long-lived system using VLSI's products:

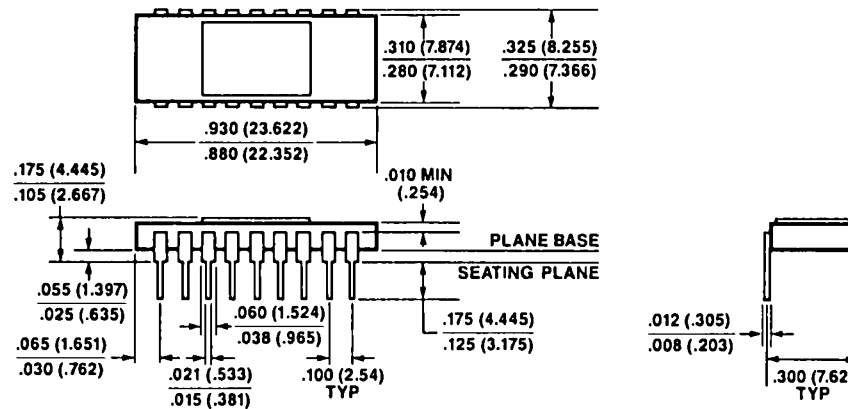
1. While few designs subject devices to extreme cold, such conditions may cause the devices to operate outside of their normal specified ranges. Therefore, the minimum operating temperature specification must be observed as well as the maximum operating temperature.
2. The ambient temperature (TA) specification refers to the air on the surface of the device. The printed circuit board design should be open enough to permit free air flow around the devices.
3. Avoid layouts that place NMOS, HMOS, or CMOS devices near such heat sources as power regulators and devices requiring heat sinks. If the design demands such proximity, ensure that the specified temperature range is not exceeded.
4. Ensure that the power supply voltage is within the specified range. Both low and high voltages beyond the specified limits may cause device overheating.

TABLE 1. PACKAGE CHARACTERISTICS

Feature	JEDEC Leadless Chip Carriers			DIP		SOIC	PLCC	PGA
	A	B	C	Ceramic	Plastic			
Uses Socket or Connector	Yes	Yes	No	Yes	Yes	No	Yes	Yes
Directly Solderable	No	No	Yes	Yes	Yes	Yes	Yes	Yes
Minimum Usual Terminal Count	14	14	14	6	6	8	16	40
Maximum Usual Terminal Count	156	156	156	64	64	28	156	225
Pin Spacing mm (mils)	1.27 (50)	1.27 (50)	1.27 (50)	2.5 (100)	2.5 (100)	1.27/1.0 (50/40)	1.27/1.0 (50/40)	2.5 (100)
Relative Cost (1 = Most Costly)	3	4	5	2	8	7	6	1

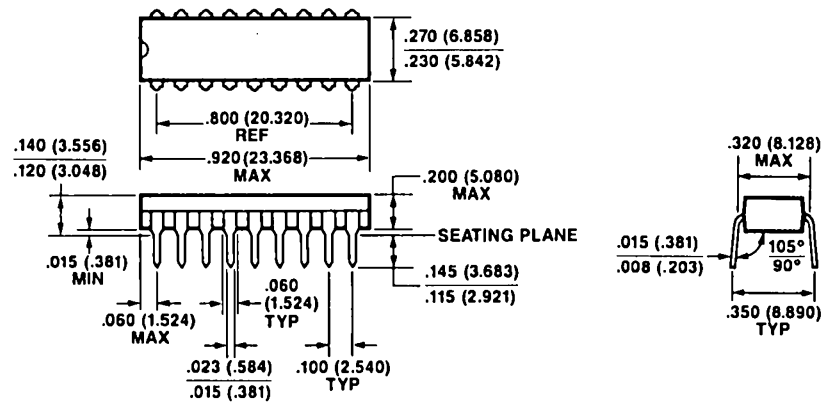
PACKAGE OUTLINES

18-PIN CERAMIC SIDE-BRAZED DUAL IN-LINE PACKAGE (DIP)



- NOTES: UNLESS OTHERWISE SPECIFIED.
1. ALL METRIC DIMENSIONS ARE IN PARENTHESES ().
 2. TOLERANCE TO BE $\pm .005$ (0.127).
 3. LEAD MATERIAL: ALLOY 42 (OR EQUIVALENT).
 4. LEAD FINISH: GOLD PLATE OVER NICKEL.

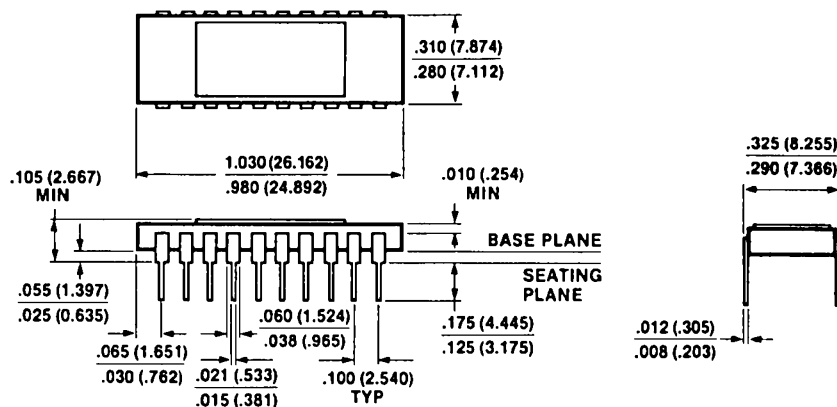
18-PIN PLASTIC DUAL IN-LINE PACKAGE (DIP)



- NOTES: UNLESS OTHERWISE SPECIFIED.
1. LEAD FINISH: MATTE TIN PLATE OR LEAD/TIN SOLDER.
 2. LEAD MATERIAL: ALLOY 42 OR COPPER.
 3. PACKAGE LENGTH DOES NOT INCLUDE END FLASH BURR, WHICH IS .010 (0.254) MAX. AT EACH END.
 4. TOLERANCE TO BE $\pm .005$ (0.127) UNLESS OTHERWISE NOTED.
 5. METRIC DIMENSIONS ARE IN PARENTHESES ().
 6. PIN 1 INDEX MARK MAY VARY IN SIZE AND SHAPE.

PACKAGE OUTLINES

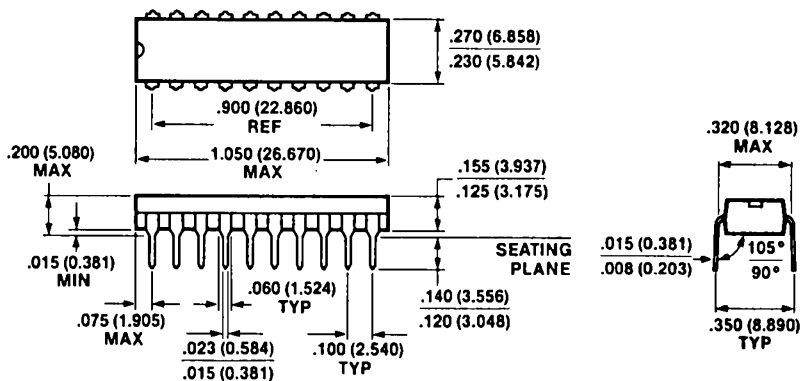
20-PIN CERAMIC SIDE-BRAZED DUAL IN-LINE PACKAGE (DIP)



NOTES: UNLESS OTHERWISE SPECIFIED.

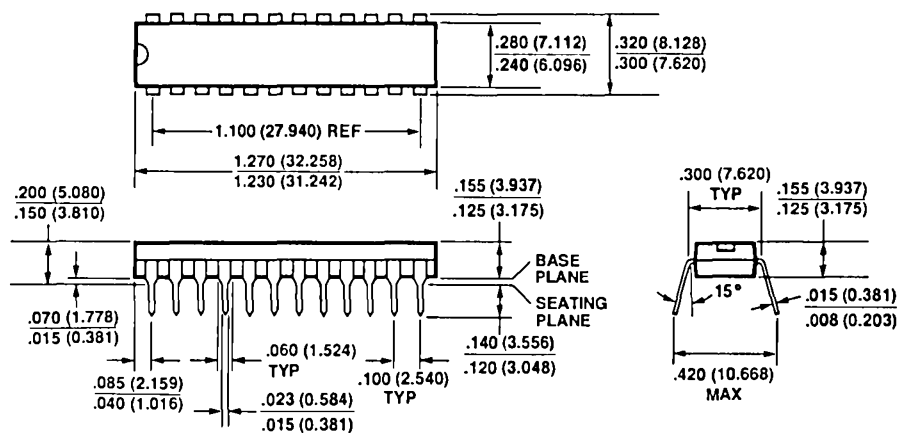
1. ALL METRIC DIMENSIONS ARE IN PARENTHESES.
2. TOLERANCE TO BE $\pm .005$ (0.127).
3. LEAD MATERIAL: ALLOY 42 (OR EQUIVALENT).
4. LEAD FINISH: GOLD PLATE OVER NICKEL.

20-PIN PLASTIC DUAL IN-LINE PACKAGE (DIP)



NOTES: UNLESS OTHERWISE SPECIFIED.

1. LEAD FINISH: MATTE TIN PLATE OR LEAD/TIN SOLDER.
2. LEAD MATERIAL: ALLOY 42 OR COPPER.
3. PACKAGE LENGTH DOES NOT INCLUDE END FLASH BURR, WHICH IS .010 (0.254) MAX AT EACH END.
4. TOLERANCE TO BE $\pm .005$ (0.127).
5. ALL METRIC DIMENSIONS ARE IN PARENTHESES.
6. PIN 1 INDEX MARK MAY VARY IN SIZE AND SHAPE.

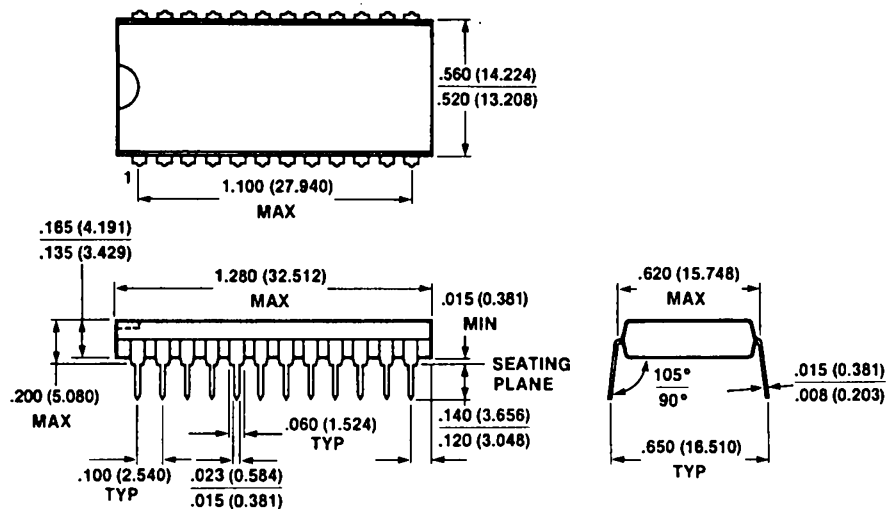
PACKAGE OUTLINES
24-PIN 0.3" WIDE PLASTIC DUAL IN-LINE PACKAGE ("SKINNY" DIP)


NOTES: UNLESS OTHERWISE SPECIFIED.

1. LEAD FINISH: MATTE TIN PLATE OR LEAD/TIN SOLDER.
2. LEAD MATERIAL: ALLOY 42 OR COPPER.
3. ALL METRIC DIMENSIONS ARE IN PARENTHESES.
4. PACKAGE LENGTH DOES NOT INCLUDE END FLASH BURR, WHICH IS .010 (0.254) MAX. AT EACH END.
5. TOLERANCE TO BE $\pm .005$ (0.127).

PACKAGE OUTLINES

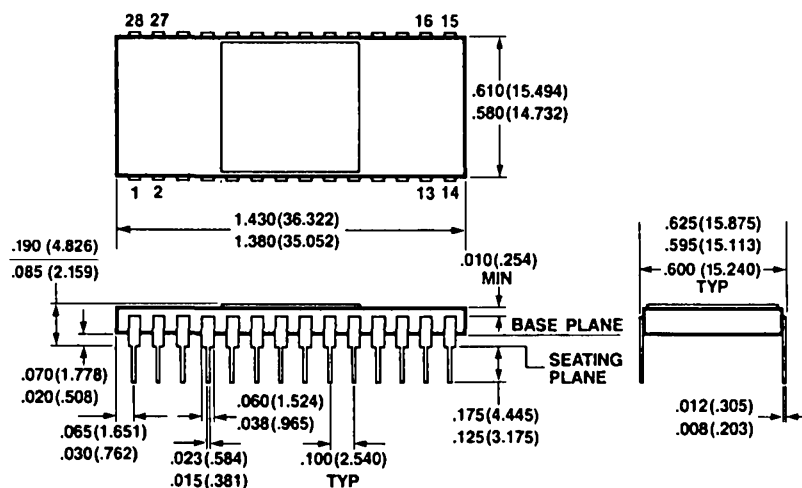
24-PIN PLASTIC DUAL IN-LINE PACKAGE (DIP)



NOTES: UNLESS OTHERWISE SPECIFIED.

1. LEAD FINISH: MATTE TIN PLATE OR LEAD/TIN SOLDER.
2. LEAD MATERIAL: ALLOY 42 OR COPPER.
3. PACKAGE LENGTH DOES NOT INCLUDE END FLASH BURR, WHICH IS .010 (0.254) MAX AT EACH END.
4. TOLERANCE TO BE $\pm .005$ (0.127).
5. ALL METRIC DIMENSIONS ARE IN PARENTHESES.
6. PIN 1 INDEX MARK MAY VARY IN SIZE AND SHAPE.

28-PIN CERAMIC SIDE-BRAZED DUAL IN-LINE PACKAGE (DIP)

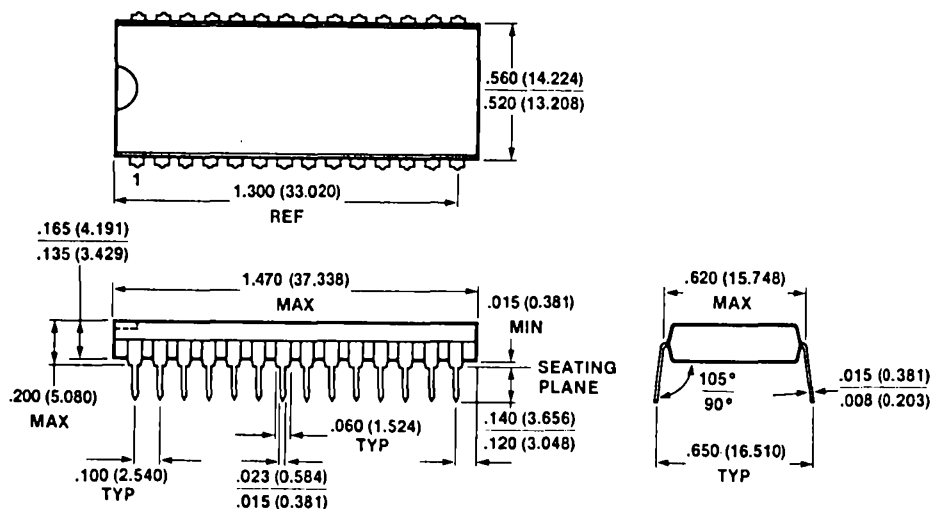


NOTES: UNLESS OTHERWISE SPECIFIED.

1. ALL METRIC DIMENSIONS ARE IN PARENTHESES.
2. TOLERANCE TO BE $\pm .005$ (0.127).
3. LEAD MATERIAL: ALLOY 42 (OR EQUIVALENT).
4. LEAD FINISH: GOLD PLATE OVER NICKEL.

PACKAGE OUTLINES

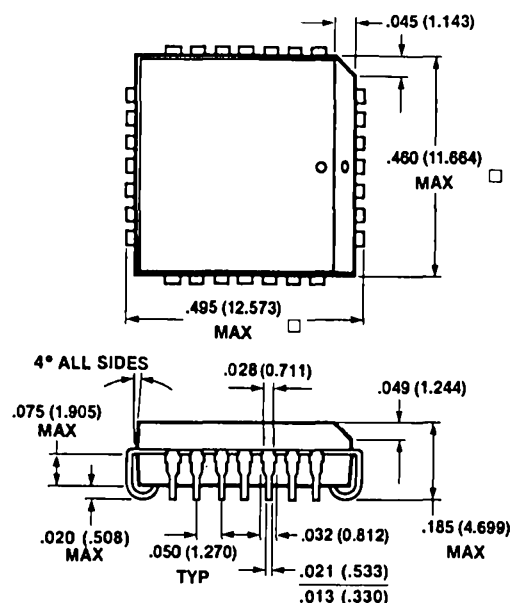
28-PIN PLASTIC DUAL IN-LINE PACKAGE (DIP)



NOTES: UNLESS OTHERWISE SPECIFIED.

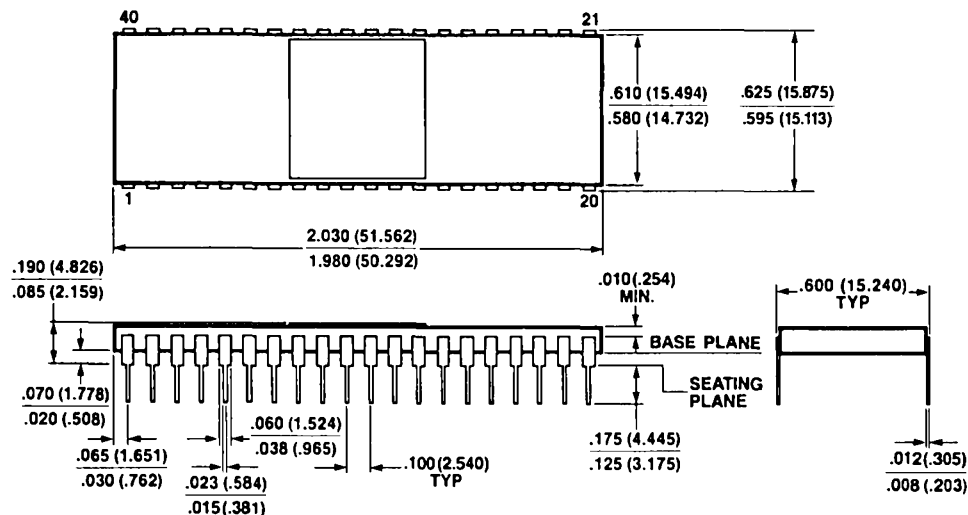
1. LEAD FINISH: MATTE TIN PLATE OR LEAD/TIN SOLDER.
2. LEAD MATERIAL: ALLOY 42 OR COPPER.
3. PACKAGE LENGTH DOES NOT INCLUDE END FLASH BURR WHICH IS .010 (0.254) MAX. AT EACH END.
4. TOLERANCE TO BE $\pm .005$ (0.127) UNLESS OTHERWISE NOTED.
5. ALL METRIC DIMENSIONS ARE IN PARENTHESES.
6. PIN 1 INDEX MARK MAY VARY IN SIZE AND SHAPE.

28-PIN PLASTIC LEADED CHIP CARRIER (PLCC)

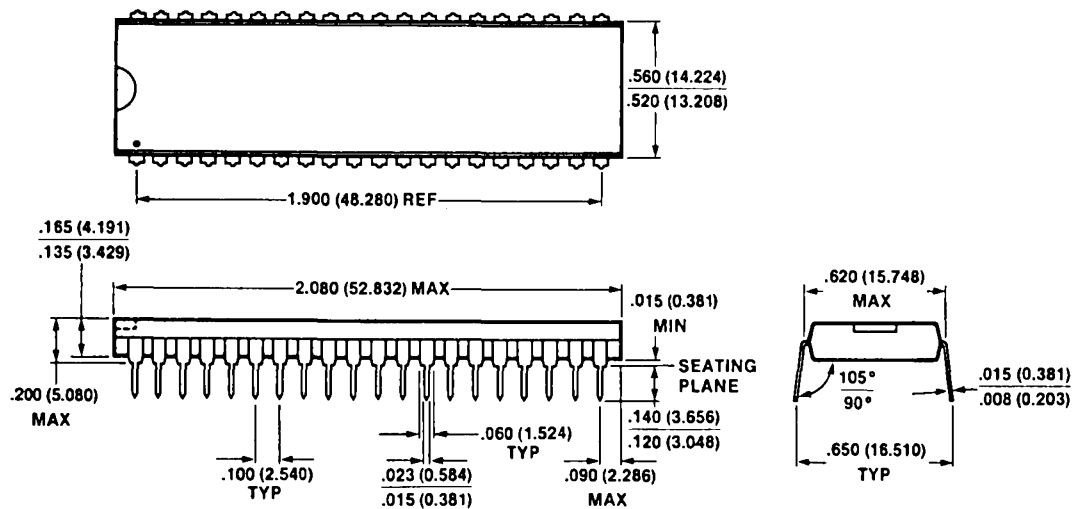


NOTES: UNLESS OTHERWISE SPECIFIED.

1. TOLERANCE TO BE $\pm .005$ (0.127).
2. LEADFRAME MATERIAL: COPPER.
3. LEAD FINISH: MATTE TIN PLATE OR SOLDER DIP.
4. SPACING TO BE MAINTAINED BETWEEN FORMED LEAD AND MOLDED PLASTIC ALONG FULL LENGTH OF LEAD.
5. MOLDED PLASTIC DIMENSION DOES NOT INCLUDE SIDE FLASH BURR, WHICH IS .010 (0.254) MAX ON FOUR SIDES.
6. ALL METRIC DIMENSIONS ARE IN PARENTHESES.

PACKAGE OUTLINES
40-PIN CERAMIC SIDE-BRAZED DUAL IN-LINE PACKAGE (DIP)


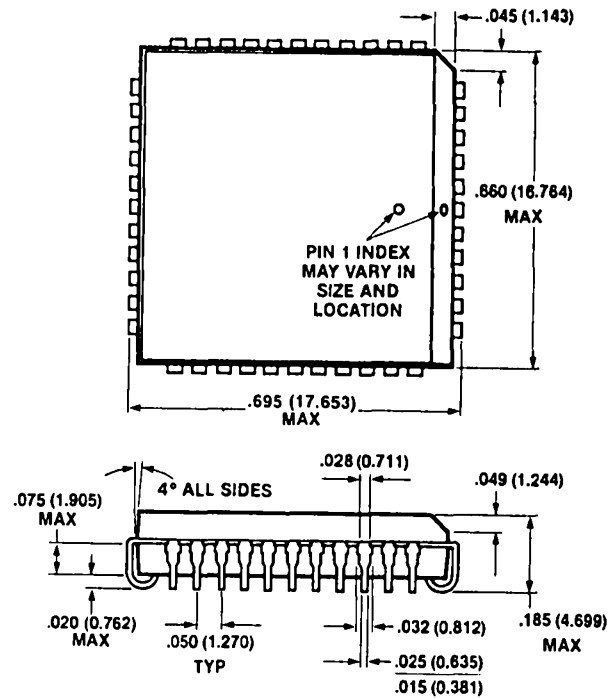
- NOTES: UNLESS OTHERWISE SPECIFIED.
1. ALL METRIC DIMENSIONS ARE IN PARENTHESES.
 2. TOLERANCE TO BE $\pm .005$ (0.127).
 3. LEAD MATERIAL: ALLOY 42 (OR EQUIVALENT).
 4. LEAD FINISH: GOLD PLATE OVER NICKEL.

40-PIN PLASTIC DUAL IN-LINE PACKAGE (DIP)


- NOTES: UNLESS OTHERWISE SPECIFIED.
1. LEAD FINISH: MATTE TIN PLATE OR LEAD/TIN SOLDER.
 2. LEAD MATERIAL: ALLOY 42 OR COPPER.
 3. PACKAGE LENGTH DOES NOT INCLUDE END FLASH BURR, WHICH IS .010 (0.254) MAX AT EACH END.
 4. TOLERANCE TO BE $\pm .005$ (0.127).
 5. ALL METRIC DIMENSIONS ARE IN PARENTHESES.
 6. PIN 1 INDEX MARK MAY VARY IN SIZE AND SHAPE.

PACKAGE OUTLINES

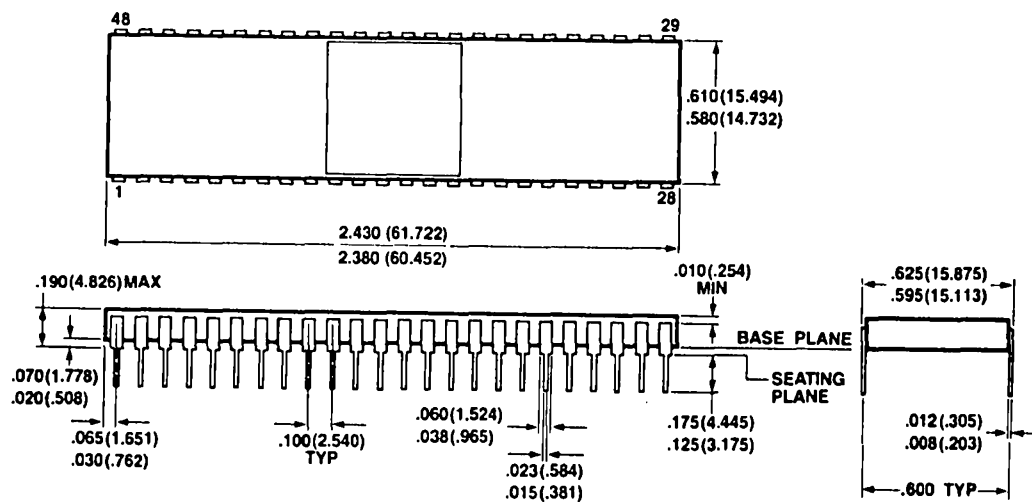
44-PIN PLASTIC LEADED CHIP CARRIER (PLCC)



NOTES: UNLESS OTHERWISE SPECIFIED.

1. TOLERANCE TO BE $\pm .005$ (0.127).
2. LEADFRAME MATERIAL: COPPER.
3. LEAD FINISH: MATTE TIN PLATE OR SOLDER DIP.
4. SPACING TO BE MAINTAINED BETWEEN FORMED LEAD AND MOLDED PLASTIC ALONG FULL LENGTH OF LEAD.
5. MOLDED PLASTIC DIMENSION DOES NOT INCLUDE SIDE FLASH BURR, WHICH IS .010 (0.254) MAX ON FOUR SIDES.
6. ALL METRIC DIMENSIONS ARE IN PARENTHESES.

48-PIN CERAMIC SIDE-BRAZED DUAL IN-LINE PACKAGE (DIP)



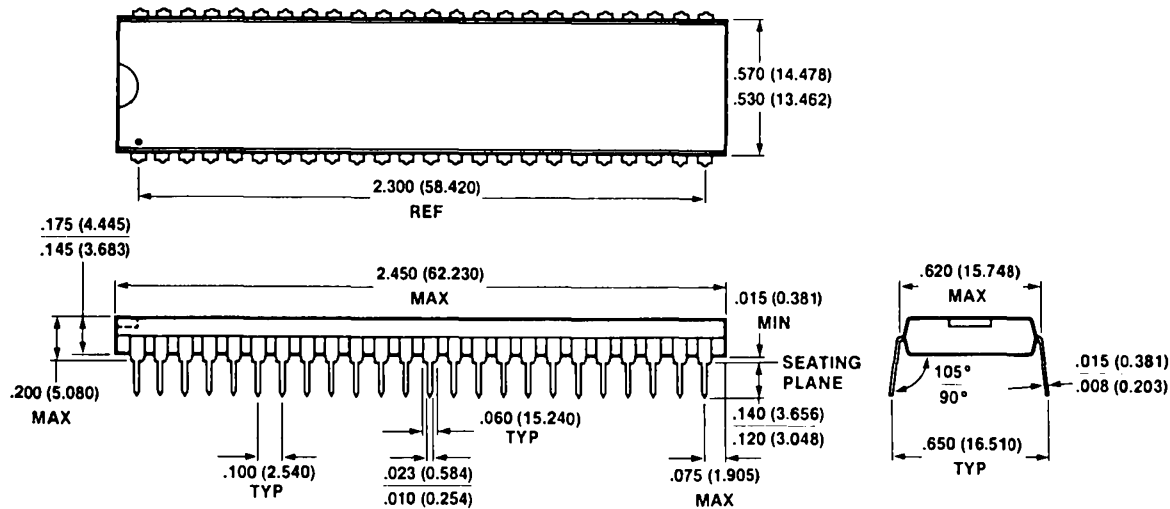
NOTES: UNLESS OTHERWISE SPECIFIED.

- NOTES: UNLESS OTHERWISE SPECIFIED:
1. ALL METRIC DIMENSIONS ARE IN PARENTHESES.
2. TOLERANCE TO BE $\pm .005$ (0.127).
3. LEAD MATERIAL: ALLOY 42 (OR EQUIVALENT).
4. LEAD FINISH: GOLD PLATE OVER NICKEL.



PACKAGE OUTLINES

48-PIN PLASTIC DUAL IN-LINE PACKAGE (DIP)



NOTES: UNLESS OTHERWISE SPECIFIED.

1. LEAD FINISH: MATTE TIN PLATE OR LEAD/TIN SOLDER.

2. LEAD MATERIAL: ALLOY 42 OR COPPER.

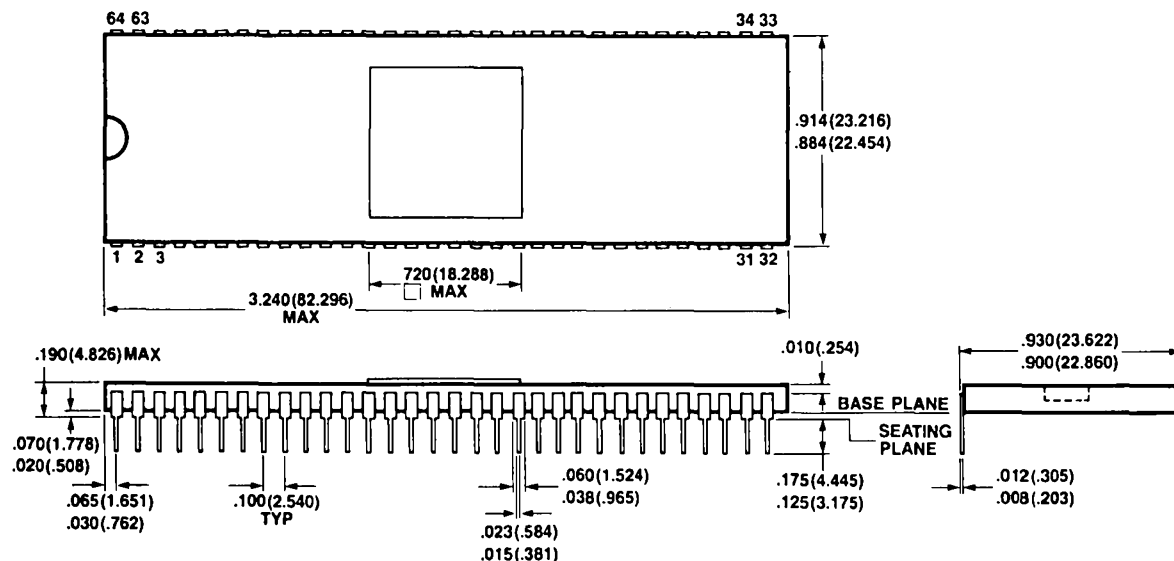
3. PACKAGE LENGTH DOES NOT INCLUDE END FLASH BURR, WHICH IS .010 (0.254) MAX AT EACH END.

4. TOLERANCE TO BE $\pm .005$ (0.127) UNLESS OTHERWISE NOTED.

5. METRIC DIMENSIONS ARE IN PARENTHESES.

6. PIN 1 INDEX MARK MAY VARY IN SIZE AND SHAPE.

64-PIN CERAMIC SIDE-BRAZED DUAL IN-LINE PACKAGE (DIP)



NOTES: UNLESS OTHERWISE SPECIFIED.

1. ALL METRIC DIMENSIONS ARE IN PARENTHESES.

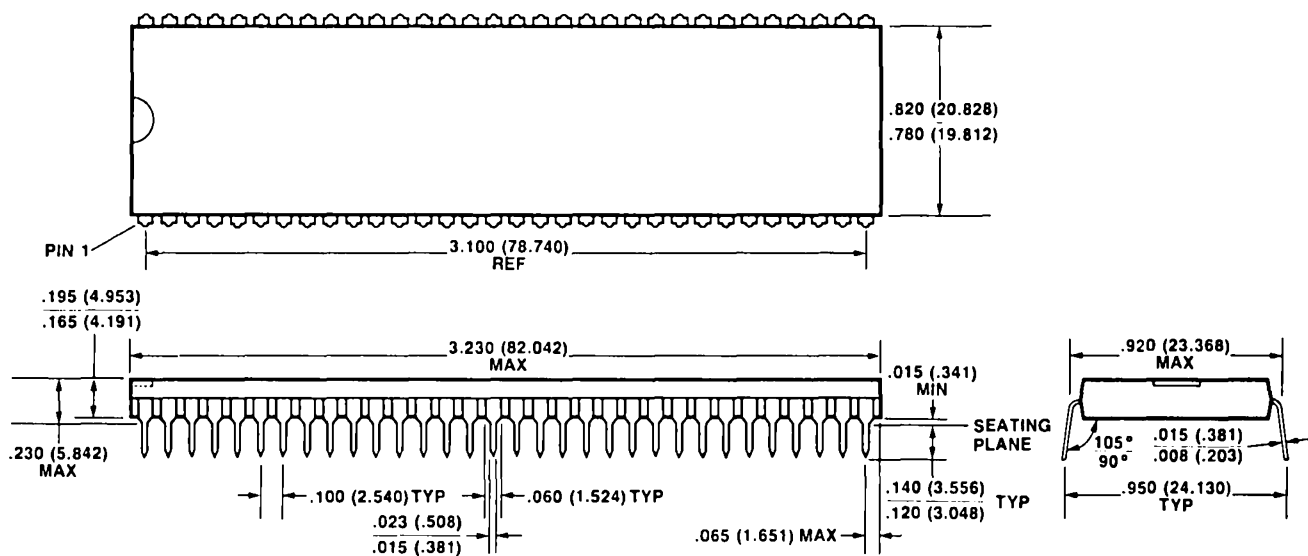
2. TOLERANCE TO BE $\pm .005$ (0.127).

3. LEAD MATERIAL: ALLOY 42 (OR EQUIVALENT).

4. LEAD FINISH: GOLD PLATE OVER NICKEL.

PACKAGE OUTLINES

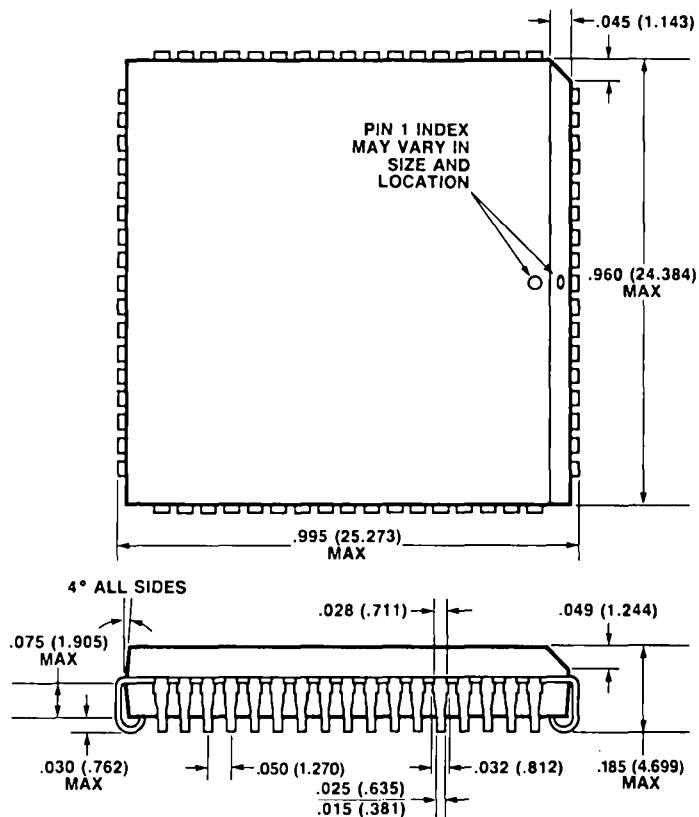
64-PIN PLASTIC DUAL IN-LINE PACKAGE (DIP)



NOTES: UNLESS OTHERWISE SPECIFIED.

1. LEAD FINISH: MATTE TIN PLATE OR LEAD/TIN SOLDER.
2. LEAD MATERIAL: ALLOY 42 OR COPPER.
3. PACKAGE LENGTH DOES NOT INCLUDE END FLASH BURR, WHICH IS .010 (0.254) MAX AT EACH END.
4. TOLERANCE TO BE $\pm .005$ (0.127).
5. METRIC DIMENSIONS ARE IN PARENTHESES.
6. PIN 1 INDEX MARK MAY VARY IN SIZE AND SHAPE.

68-PIN PLASTIC LEADED CHIP CARRIER (PLCC)

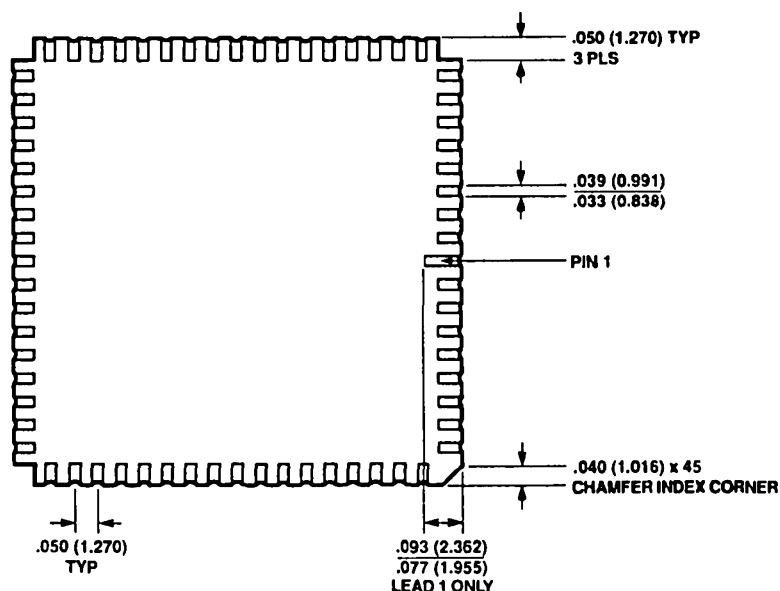
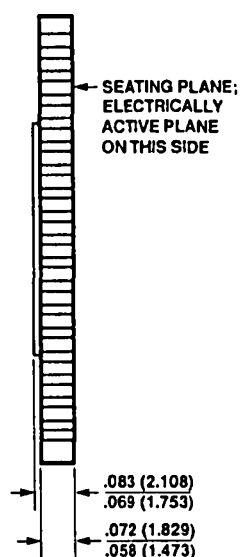


NOTES: UNLESS OTHERWISE SPECIFIED.

1. TOLERANCE TO BE $\pm .005$ (0.127).
2. LEADFRAME MATERIAL: COPPER.
3. LEAD FINISH: MATTE TIN PLATE OR SOLDER DIP.
4. SPACING TO BE MAINTAINED BETWEEN FORMED LEAD AND MOLDED PLASTIC ALONG FULL LENGTH OF LEAD.
5. MOLDED PLASTIC DIMENSION DOES NOT INCLUDE SIDE FLASH BURR, WHICH IS .010 (0.254) MAX ON FOUR SIDES.
6. ALL METRIC DIMENSIONS ARE IN PARENTHESES.

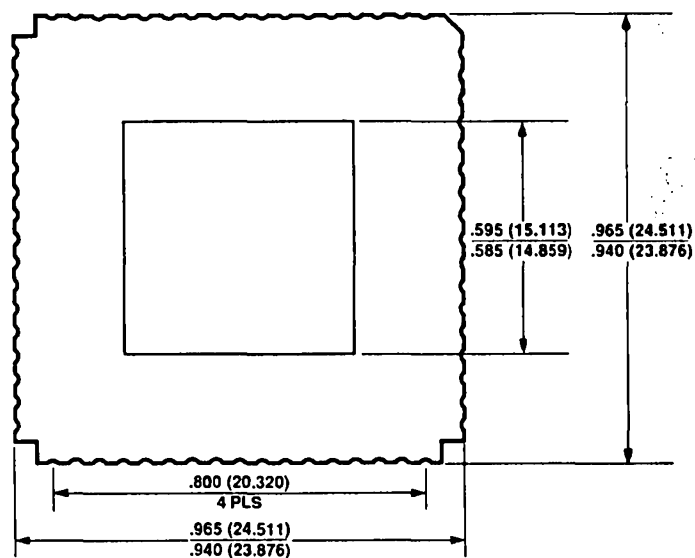
PACKAGE OUTLINES

68-PIN LEADLESS CHIP CARRIER (LCC)



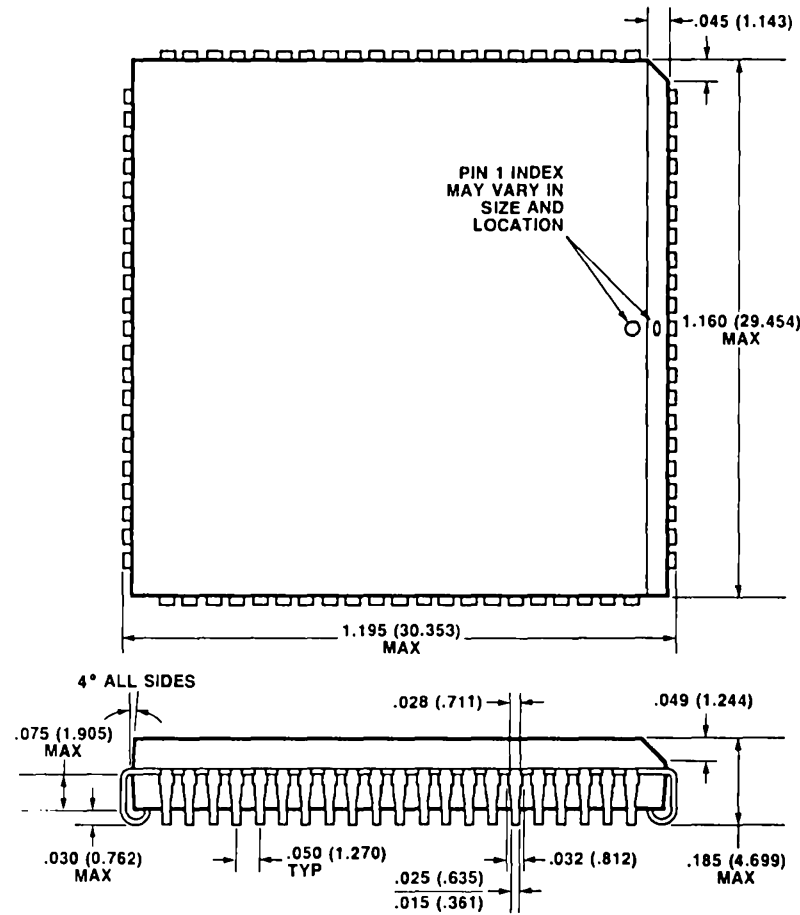
NOTES: UNLESS OTHERWISE SPECIFIED.

1. TOLERANCE: $\pm .005$ (0.127).
2. ALL EXPOSED METALLIZED AREAS: GOLD-PLATED (60 MICROINCHES MIN. THICKNESS) OVER NICKEL (50 MICROINCHES MIN., 350 MICROINCHES MAX.) OVER REFRACTORY METALLIZATION.
3. MATERIAL: Al_2O_3 .
4. LID SEAL: GOLD/TIN EUTECTIC.
5. ALL METRIC DIMENSIONS ARE IN PARENTHESES. METRIC DIMENSIONS ARE IN MILLIMETERS.
6. JEDEC TYPE B PACKAGE.



PACKAGE OUTLINES

84-PIN PLASTIC LEADED CHIP CARRIER (PLCC)

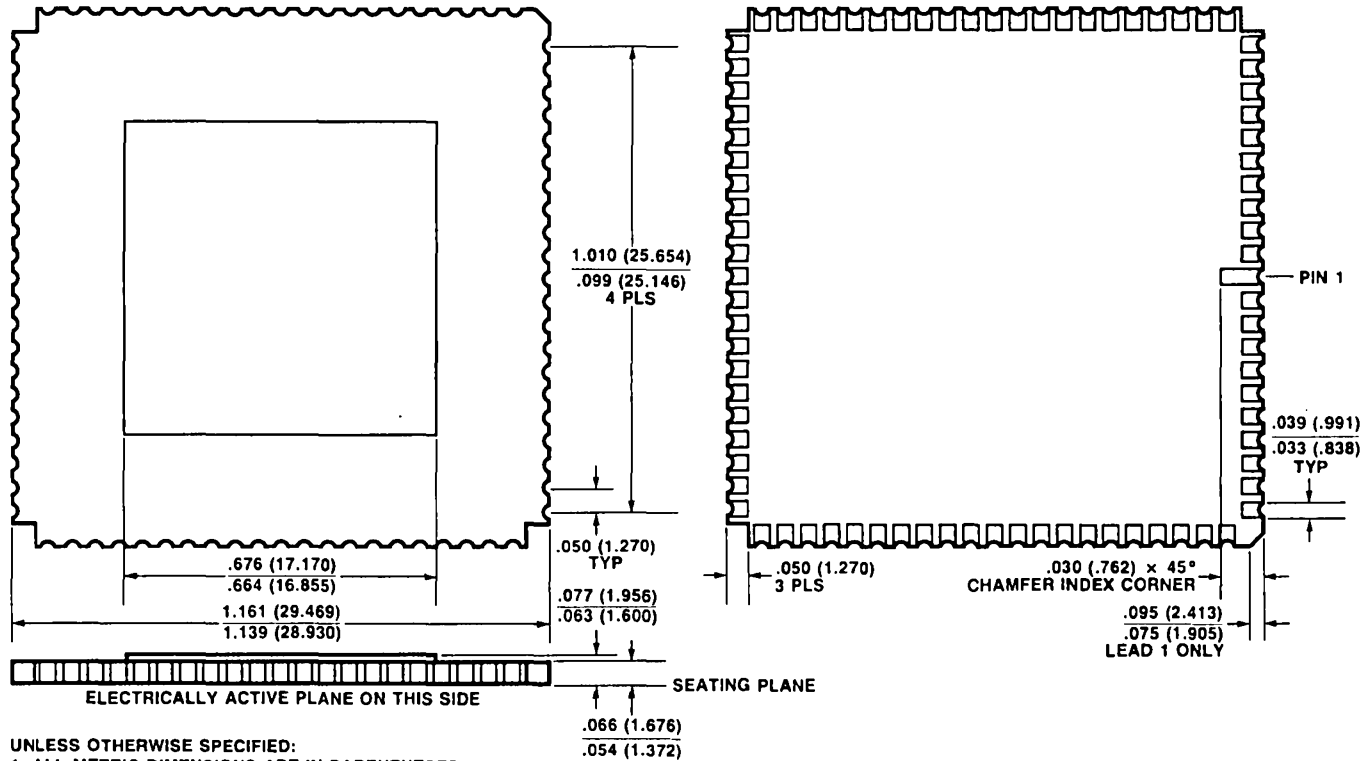


UNLESS OTHERWISE SPECIFIED:

1. ALL METRIC DIMENSIONS ARE IN PARENTHESES.
METRIC DIMENSIONS ARE IN MILLIMETERS.
2. TOLERANCE TO BE $\pm .005$ (0.127).
3. LEADFRAME MATERIAL: COPPER.
4. LEAD FINISH: MATTE TIN PLATE OR SOLDER DIP.
5. SPACING TO BE MAINTAINED BETWEEN FORMED LEAD AND MOLDED PLASTIC
ALONG FULL LENGTH OF LEAD.
6. MOLDED PLASTIC DIMENSION DOES NOT INCLUDE SIDE FLASH BURR, WHICH IS
.010 (0.254) MAX. ON FOUR SIDES.

PACKAGE OUTLINES

84-PIN LEADLESS CHIP CARRIER (LCC)



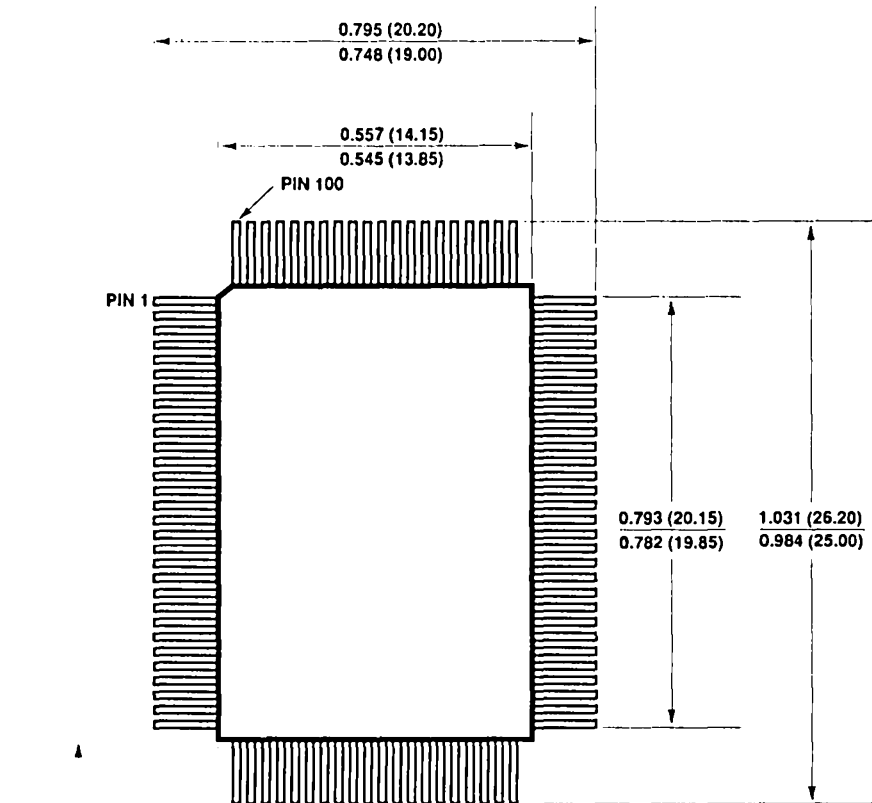
UNLESS OTHERWISE SPECIFIED:

1. ALL METRIC DIMENSIONS ARE IN PARENTHESES.
METRIC DIMENSIONS ARE IN MILLIMETERS.
2. TOLERANCE TO BE $\pm .005$ (0.127).
3. ALL EXPOSED METALLIZED AREAS SHALL BE GOLD-PLATED (60 MICROINCHES MIN. THICKNESS) OVER NICKEL (50 MICROINCHES MIN., 350 MICROINCHES MAX.) OVER REFRACTORY METALLIZATION.
4. MATERIAL: Al_2O_3 .
5. JEDEC TYPE B PACKAGE.

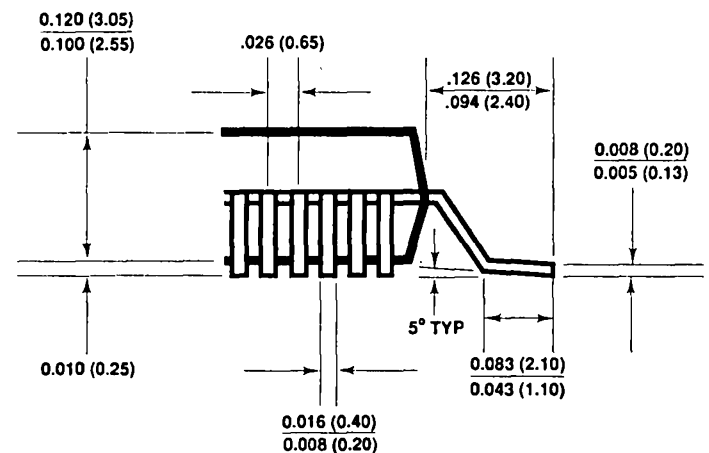
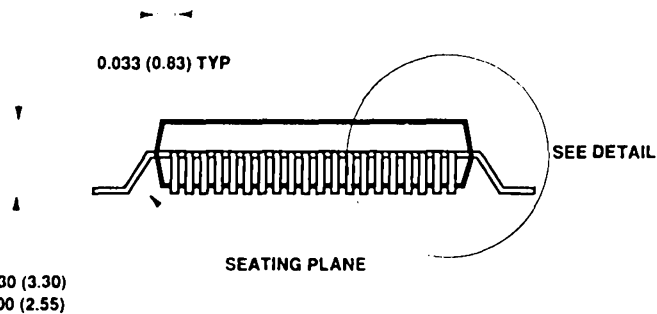


PACKAGE OUTLINES

100-PIN PLASTIC FLATPACK (CJQFP)



0.023 (0.58) TYP

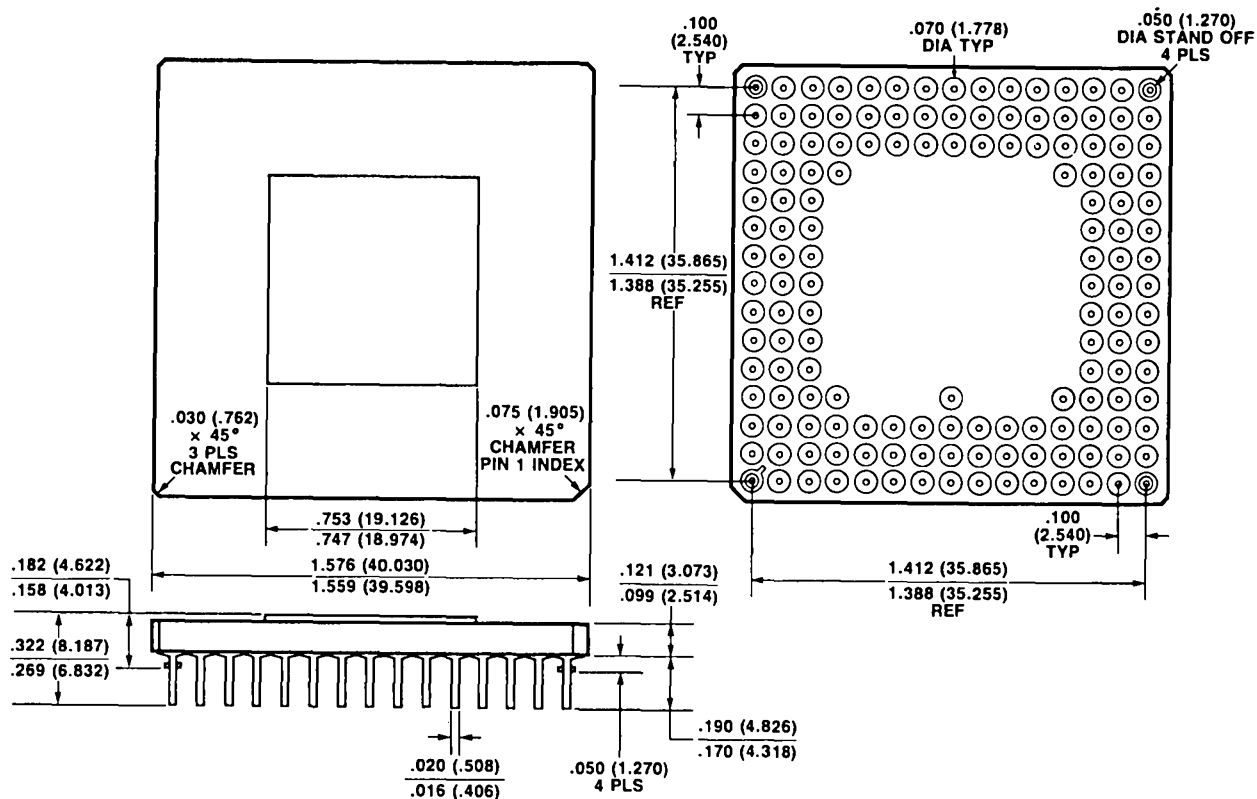


- NOTES: UNLESS OTHERWISE SPECIFIED
1. THE CJQFP ARE CURRENTLY USED ONLY FOR PROTOTYPE BUILDS.
 2. ALL METRIC DIMENSIONS ARE IN PARENTHESES.
 3. CJQFP ARE EPOXY DIE ATTACHED AND EPOXY SEALED.
 4. LEADFRAME: ALLOY 42
- DIE ATTACH MATERIAL: HITACHI CHE EN-4000, KASEI EPINAR 4110
MOLD COMPOUND: SUMITOMO 6300, KASEI CEL 4000



PACKAGE OUTLINES

149-PIN CERAMIC PIN GRID ARRAY (PGA)



UNLESS OTHERWISE SPECIFIED:

1. ALL METRIC DIMENSIONS ARE IN PARENTHESES.
METRIC DIMENSIONS ARE IN MILLIMETERS.
2. TOLERANCE TO BE $\pm .005$ (0.127).
3. MATERIAL: Al_2O_3 .
4. LEAD MATERIAL: KOVAR.
5. LEAD FINISH IS GOLD PLATING (60 MICROINCHES MIN. THICKNESS) OVER NICKEL (100 MICROINCHES NOMINAL THICKNESS).

RASTER OP ALU

FEATURES

- Provides hardware assist for bit-mapped graphics operations. Includes 32-bit barrel shifter
- Performance increase over software implementations:
 - Monochrome = 4 x Software
 - Color = 4 x (Planes) x Software
- Supports both CRT displays and such hardcopy devices as laser printers
- Compatible with both monochrome and color displays
- Implements all 256 possible raster operations on source, destination, and pattern data
- 28-pin package; 5 V supply

DESCRIPTION

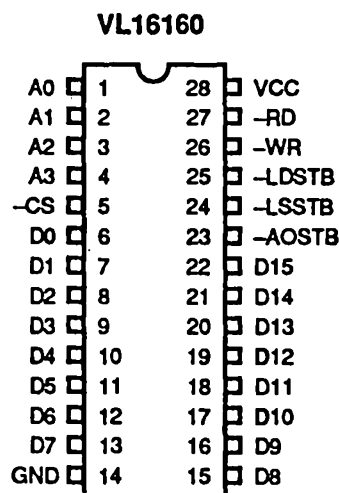
The VL16160 Raster Op ALU (RALU) provides hardware-assisted performance enhancements for bit manipulation operations used in bit-mapped graphics displays. These operations, called bit block translation (BITBLT), allow bit-mapped images to be combined and manipulated by logical operators. These operators include AND, OR, and XOR, and can be used on source, destination, and pattern data. Additionally, support for masking with multiple mask registers for clipping is included.

The BITBLT operation is general purpose enough to be used in a wide range of graphics operations, including text display using arbitrary fonts,

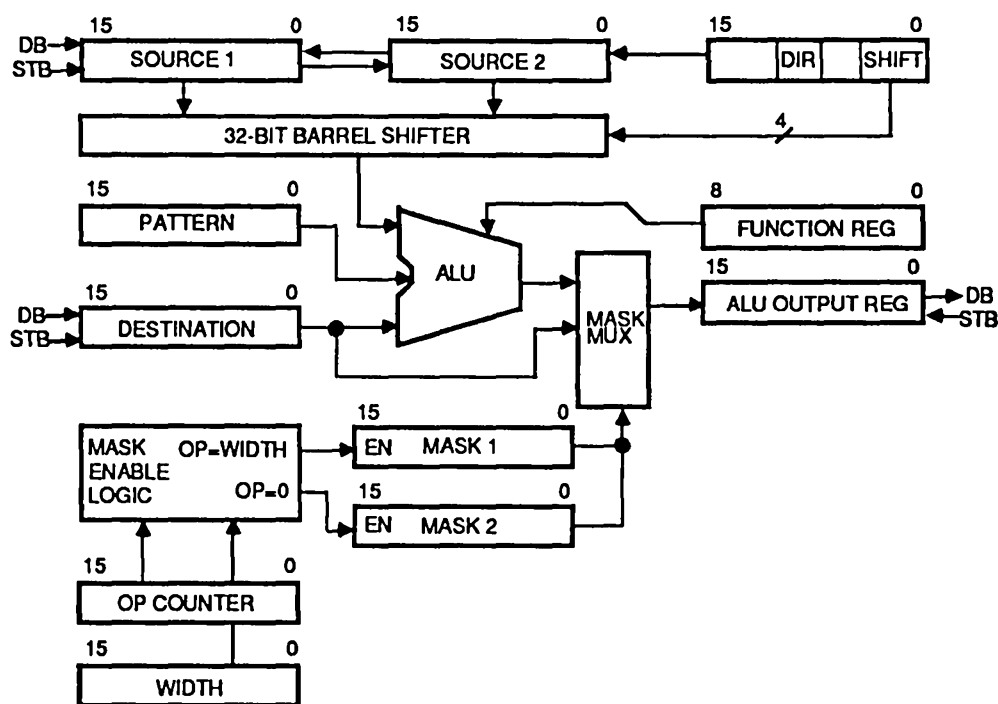
attributes, and enhancements. Successive applications of BITBLT can perform such operations as scaling, filling, rotations, and texturing.

In a typical application, the RALU operates on display data in 16-bit words that are latched into its input buffers by external hardware. Once source, destination, pattern, shift, and masking data are loaded into the RALU, the source data is bit-aligned with the destination data, and the logical operation specified in the function register takes place. The results are stored in the ALU Output Register, which can be output onto the bus by a single strobe signal.

PIN DIAGRAM



BLOCK DIAGRAM

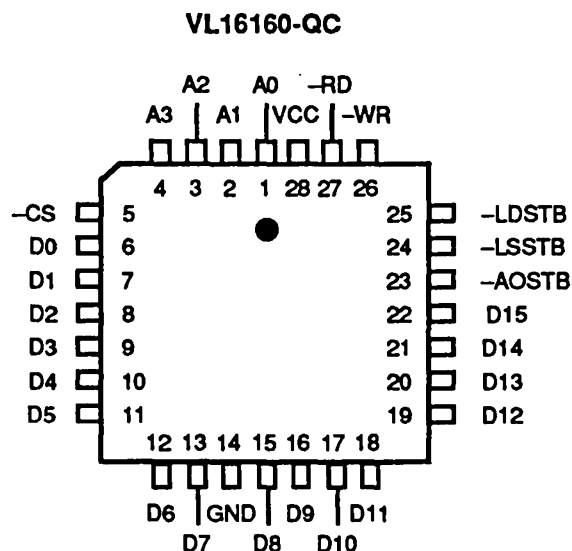


ORDER INFORMATION

Part Number	Package
VL16160PC	Plastic DIP
VL16160CC	Ceramic DIP
VL16160QC	Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range is 0°C to +70°C.

PIN DIAGRAM



SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Description
D0-D15	6-15	Bidirectional data lines; input enabled by -CS and -WR. Input data to Destination Register must be stable relative to the trailing edge of -LDSTB. Output enabled by -CS, -RD, and A0-A3 or -AOSTB.
-CS	5	Chip Select; Must be active to write to or read from internal registers.
-RD	27	Read Enable; Input used to strobe any internal register data to the data bus pins. Must be active in conjunction with -CS.
-WR	26	Write Enable; Input used to strobe data on data bus pins into the selected register. Must be active in conjunction with -CS.
A0-A3	1-4	Register Address; Address inputs that specify the internal chip register to be accessed for a read or write operation.
-AOSTB	24	ALU Output Strobe; Input used to enable the output of the function decoder onto the data bus pins. Cannot be active when -CS and -RD or -WR are active.
-LDSTB	25	Load Destination Register Strobe; Input used to strobe the value (address) on the data bus pins into the Destination Register. Value on A0-A3 need not be valid when -LDSTB is used to load the Destination Register. The -LDSTB pin also decrements the op counter each time it is pulsed.
-LSSTB	24	Load Source Register Strobe; Input used to strobe the value on the data bus into the Source Register specified by the Direction Bit. The other Source Register is loaded with the previous contents of the Source Register being loaded.
GND	14	Ground
VCC	28	+5 V \pm 5%



FUNCTIONAL DESCRIPTION

The VL16160 consists of four basic blocks: Source Shifter, Function Decoder, Op Counter, and the Register set. The internal data bus is 16 bits wide, enabling all internal registers to be accessed easily from the I/O bus for context saving and restoring. In operation, the Source Shifter extracts data from the Source Registers and shifts the data to be aligned with the data in the Destination and Pattern Registers. The Function Decoder then performs a 16-bit Boolean operation as specified by the Function Register with the data extracted from the Source Registers and the data in the Destination and Pattern Registers. The result of the Boolean operation is available on the external I/O bus when the -AOSTB signal is strobed and can easily be written back into display memory. The Op counter and associated registers provide the support for clipping operations as required by the application.

SOURCE SHIFTER

The Source Shifter performs bit alignment on the concatenated 32 bits of data in the Source 1 and Source 2 Registers. The amount of bit alignment performed is based upon the value in the Shift Value Register. When -LSSTB is strobed, the Source Shifter extracts 16 contiguous bits from the 32 bits of data in the Source 1 and Source 2 registers as follows:

1. If the low order four bits of the Shift Value Register have a non-zero value, that value specifies the shift count by which the 16-bit field to be extracted is offset from bit 0 of the concatenated source registers, as shown in Figure 1. The result is passed on to the Function Decoder.
2. If the low-order four bits of the Shift Value Register is 0, the contents of either Source 1 or Source 2 are passed directly to the Function Decoder and no shifting occurs. The direction bit indicates which source register is used in the operation, as shown in Figure 1.

FUNCTION DECODER

The Function Decoder performs a Boolean operation on the contents of the Destination Register, Pattern Register, and the output of Source Shifter. The Boolean operation is specified by the Function Register. With the three operands, 256 different Boolean operations are possible. The result of the operation is available on the I/O bus when the -AOSTB control signal is active. -AOSTB signal cannot be active at the same time that -CS and -RD or -WR are active. The result of the Boolean operation is also available by reading the ALU Output Register.

To understand how the Function Decoder performs the desired Boolean operation, note again that with three operands, (data in the Source, Pattern and Destination Registers), a total of 256 different boolean operations is possible. Out of these 256 possible operations, the application defines which are needed to perform the desired task.

For example (see Figure 2), to "paint" a new image over an existing image requires the source data (image) to be ORed with the destination data (image). This means "Source Register OR the Destination Register". For each bit, there are four possible results of this operation between these two registers. However, since the Pattern Register is always included, even when it is a "don't care," a total of eight different possible results of this one Boolean operation is possible. These eight combinations define the "function code" for the overlay operation. Thus, the function code is really defined as the result (and the only result possible) of a Boolean combination of the Source, Destination, and Pattern Registers. In using the VL16160, the application defines which of the 256 possible Boolean combinations of the Source, Destination and Pattern Registers define those "functions" required of the application, and when that "function" is required, the corresponding function code is loaded into the Function Register.

In principal, the Function Decoder operates on a bit-by-bit basis as a 1-of-8 data selector with each data bit in the

Source, Destination, and Pattern Registers selecting one of eight bits of data from the Function Register.

The function codes required of an application are determined ahead of time by the user and stored in memory to be used as needed. The determination of the correct function code is a matter of simply applying the definitions stated above (see Figure 2), in a simple method. The truth table for Pattern, Source, and Destination bits is written, with the desired output. This desired output is read as the desired value of the Function Register, with the least significant bit as shown in Figure 2. Using this method, the software engineer can easily define a pattern to suit each specific need.

OP COUNTER

The Op Counter, in conjunction with the Width and Mask Registers, provides for masking of selected bits in the Destination Register. This masking prevents the VL16160 from modifying selected areas of display memory when performing BITBLTs. For example, clipping may be required at the edges of a window. The function of the Op Counter is to keep track of the beginning and end of each row, so that the mask registers can handle this clipping automatically, without additional processor intervention.

The Op Counter must be correctly initialized prior to the beginning of a raster operation. The enabling of masking is internally clocked by the -LDSTB signal. For this reason, after loading the Op counter with an initial value, -LDSTB must be pulsed before the -LSSTB of the first operation. Since this -LDSTB will decrement the Op Counter, it is necessary to increment the Op Counter to be one more than the intended value, so that this "dummy" -LDSTB starts out the BITBLT with the correct Op Counter value. This "dummy" -LDSTB does have to be repeated between scanlines, as the masking remains enabled. If context switching is utilized, however, reinitialization (with the loading of Op Counter and subsequent -LDSTB) is necessary before leaving a context, or upon re-entering one, in the middle of a BITBLT.



REGISTER DESCRIPTION

As shown in the block diagram, the RALU consists of a number of registers, each connected to the internal 16-bit data path. Of these registers, three are used very often and are directly accessible from the data bus by the assertion of strobe signals.

SOURCE

The Source Register holds a 16-bit word of data to be modified by a raster operation. It is loaded from the data bus by the assertion of the –LSSTB signal.

DESTINATION

The Destination Register holds a word of data from the bit-mapped display that is modified by the source data and raster operation. It is loaded from the data bus when –LDSTB is asserted.

ALU OUTPUT

The ALU Output Register holds the result of the raster operation to be written back to memory. The contents may be put onto the data bus by the assertion of the –AOSTB signal.

The remainder of the registers are typically set up for a series of operations and are not changed until the end of a scan line.

DIR / SHIFT

This register controls the direction of the raster operation (left-to-right or right-to-left). In addition, it specifies the number of bits to shift to align the source with the destination fields.

MASK 1 and 2

These registers are used to define the left and right boundaries of the area on the screen that is manipulated. (The direction bit affects which register corresponds to left vs. right). A bit set in these registers allows the corresponding bit in the Destination Register to pass through unaltered. When the Op Counter is equal to the Width Register (usually for the first raster operation on each scan line), the Mask 1 Register selects bits to be included in the operation. Masking is disabled until the Op Counter is zero (usually for the last operation on a scan line); at that time, the Mask 2 register is used.

PATTERN

This register contains data to be combined with the output of the bit-shifted source register. This is commonly used for enhancing an image with a background pattern.

FUNCTION

This register contains the operator that is used to combine the source, destination, and pattern data.

OP COUNTER

The Op Counter Register specifies the current count of the operation in progress. The Op Counter is decremented each time –LDSTB is brought active. After the Op counter goes to zero, the next –LDSTB causes the Op counter to be reloaded with the value of the Width register prior to the next operation. The Op counter can be set to the value of the Width Register at the start of a raster operation by beginning an operation with a "dummy" –LDSTB. This loads the Op counter in preparation for the first scan line.

WIDTH

The Width Register specifies the width of the line (in 16-bit words) on which raster operations will take place.

FLAG REGISTER

The Flag Register is uncommitted and can be used to temporarily store context information for multi-tasking implementations.

FIGURE 1. SHIFTING AND DIRECTION

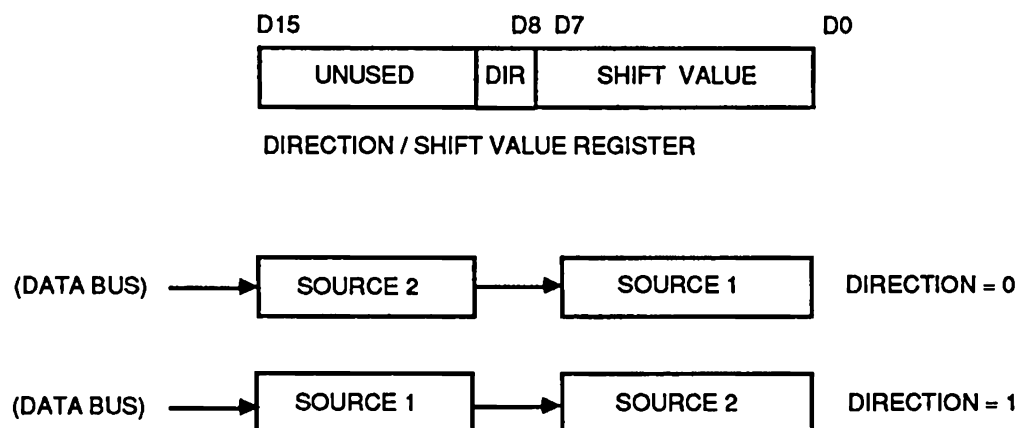


TABLE 1. REGISTER MAP

0	Destination Register
1	Source 1 Register
2	Source 2 Register
3	Pattern Register
4	Mask 1 Register
5	Mask 2 Register
6	Shift Value Register
7	Function Register
8	Width Register
9	Operation Count Register
10	ALU Output Register
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	Flag Register

FIGURE 2. RASTER OPERATIONS EXAMPLE

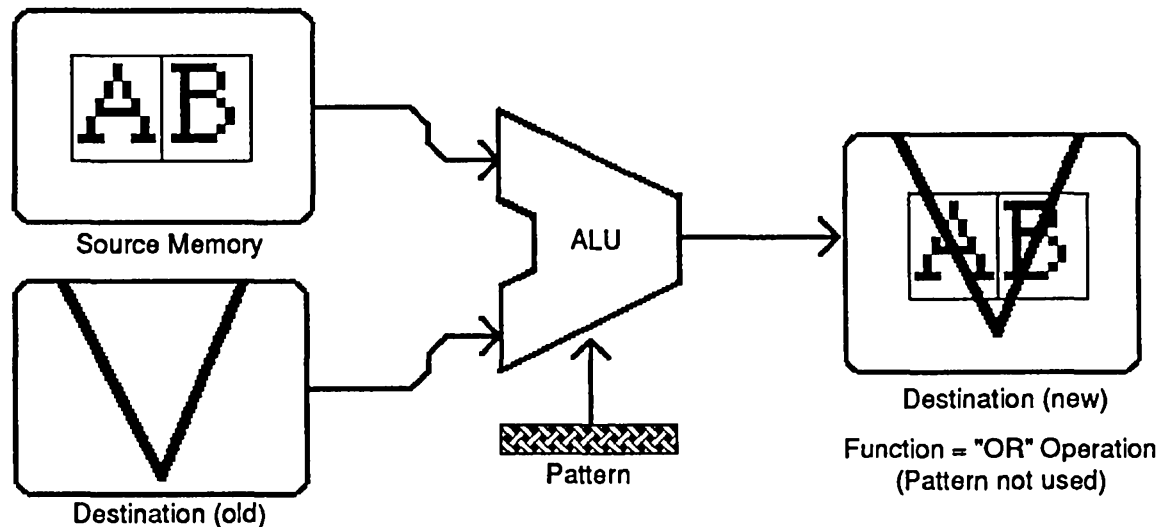


FIGURE 2a. SOURCE XOR DESTINATION (66_{16})

Pattern	Source	Dest.	Funct.
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

MSB

Example

LSB

FIGURE 2d. SOURCE XOR DESTINATION OR PAT. ($6F_{16}$)

Pattern	Source	Dest.	Funct.
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

MSB

Example

LSB

▨ = Pattern

FIGURE 2b. SOURCE OR DESTINATION (77_{16})

Pattern	Source	Dest.	Funct.
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

MSB

Example

LSB

FIGURE 2e. SOURCE OR DESTINATION OR PAT. ($7F_{16}$)

Pattern	Source	Dest.	Funct.
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

MSB

Example

LSB

▨ = Pattern

FIGURE 2c. SOURCE OVERLAY DESTINATION (33_{16})

Pattern	Source	Dest.	Funct.
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

MSB

Example

LSB

FIGURE 2f. SOURCE OVERLAY DEST. OR PAT. ($1F_{16}$)

Pattern	Source	Dest.	Funct.
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

MSB

Example

LSB

▨ = Pattern

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	-0.5 V to +7.0 V
Input Voltage	-0.5 V to +7.0 V
Output Voltage	-0.5 V to +7.0 V
Operating Temperature	0°C to +70°C
Storage Temperature	-65°C to +150°C
Lead Temperature (10 s.)	300°C
Junction Temperature	175°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device

under these or any other conditions above those listed in this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device

DC CHARACTERISTICS $T_A = 0^\circ\text{C to } +70^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 0.25\text{ V}$

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V_{IH}	High-Level Input Voltage	2.4			V	
V_{IL}	Low-Level Input Voltage		0.6		V	
V_{OH}	High-Level Output Voltage	2.4			V	$V_{CC} = \text{Min}$; $I_{OH} = -400\text{ }\mu\text{A}$
V_{OL}	Low-Level Output Voltage		0.3	0.45	V	$V_{CC} = \text{Min}$; $I_{OL} = 4.4\text{ mA}$
I_{OH}	High-Level Output Current	-400			μA	
I_{OL}	Low-Level Output Current	4.4			mA	
I_{IL}	Input Leakage Current			10	μA	$V_I = 0.45\text{ V}$
$I_{I/O}$	I/O Leakage Current	$0.7\text{ V} < V_O < V_{CC}$		20	μA	
		$0.4\text{ V} < V_O < V_{CC}$	100			
I_{CC}	Power Supply Current at DC			120	mA	$V_{CC} = \text{Max}$

CAPACITANCE $T_A = 0^\circ\text{C to } +70^\circ\text{C}$

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
$C_{I/O}$	I/O Capacitance			15	pF	
C_I	Input Capacitance		6	15	pF	

AC TIMING CHARACTERISTICS $T_A = 0^{\circ}\text{C to } +70^{\circ}\text{C}$, $V_{CC} = 5\text{ V} \pm 0.25\text{ V}$

Symbol	Parameter	Min	Max	Unit	Conditions
tCSH	–CS, A0-A3 Hold After –WR Active	20		ns	
tRWW	–WR, –RD Signal Width	60		ns	
tCSS	–CS, A0-A3 Setup to –WR Inactive	0		ns	
CSV	Data Valid After –CS Active		120	ns	
tRDV	Data Valid After –RD Active		120	ns	
tRDH	Data Valid After –RD, –CS Inactive	5		ns	
tWRS	Data Setup to –WR Inactive	50		ns	
tWRH	Data Hold After –WR Inactive	30		ns	
tLSW	–LSSTB Pulse Width	60		ns	
tNLS	Time Between –LSSTB Pulses	0		ns	
tSDV	–LSSTB Inactive to Valid Data		120	ns	
LSF	–LSSTB Inactive to AOSTB Active	30		ns	
tLDV	–LSSTB Active to Valid Data		170	ns	
tLDW	–LDSTB Pulse Width	60		ns	
tNLD	Time Between –LDSTB Pulses	150		ns	
tLDF	–LDSTB Inactive to –AOSTB Active	20		ns	
tLSS	Data Setup to –LSSTB Inactive	20		ns	
tLSH	Data Hold after –LSSTB Inactive	25		ns	
tLDS	Data Setup to –LDSTB Inactive	30		ns	
tLDH	Data Hold After –LDSTB Inactive			ns	
tFOV	Data Valid After –AOSTB Active		90	ns	
tDDV	Data Valid After Valid –LDSTB Data		140	ns	
tFDV	Bus High-Impedance After –AOSTB Inactive		40	ns	

FIGURE 3. REGISTER READ/WRITE TIMING

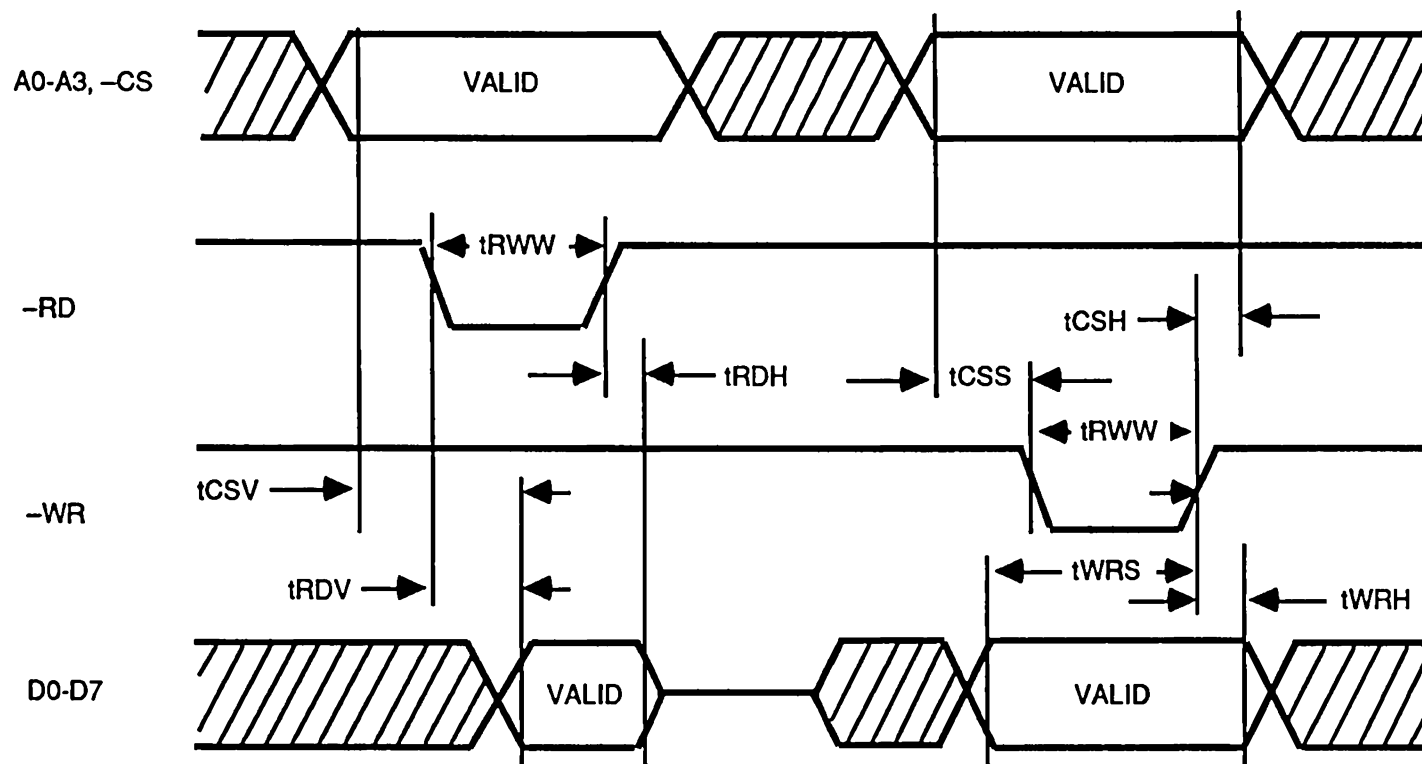


FIGURE 4. SOURCE REGISTER AND ALU OUTPUT CONTROL SIGNAL TIMING

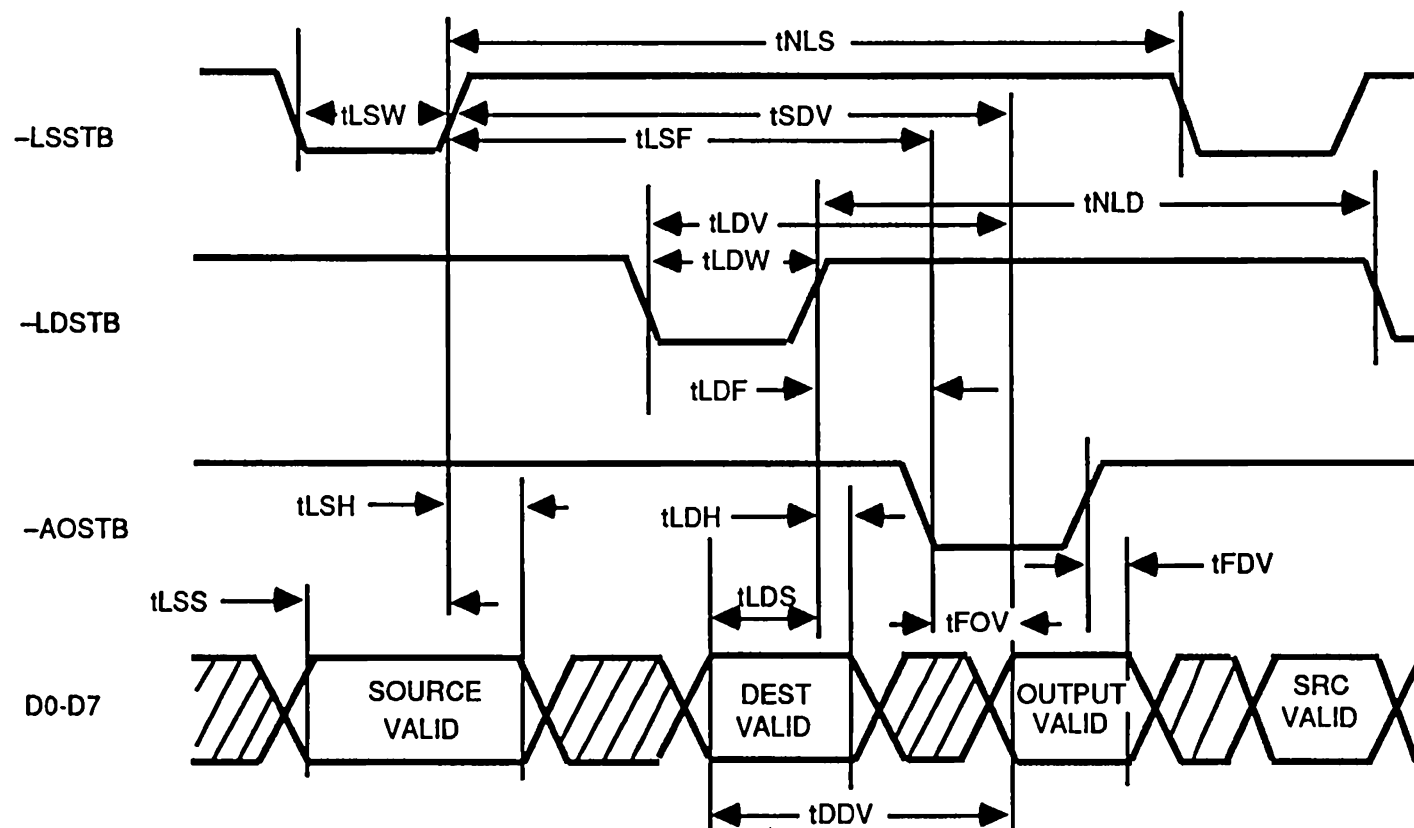
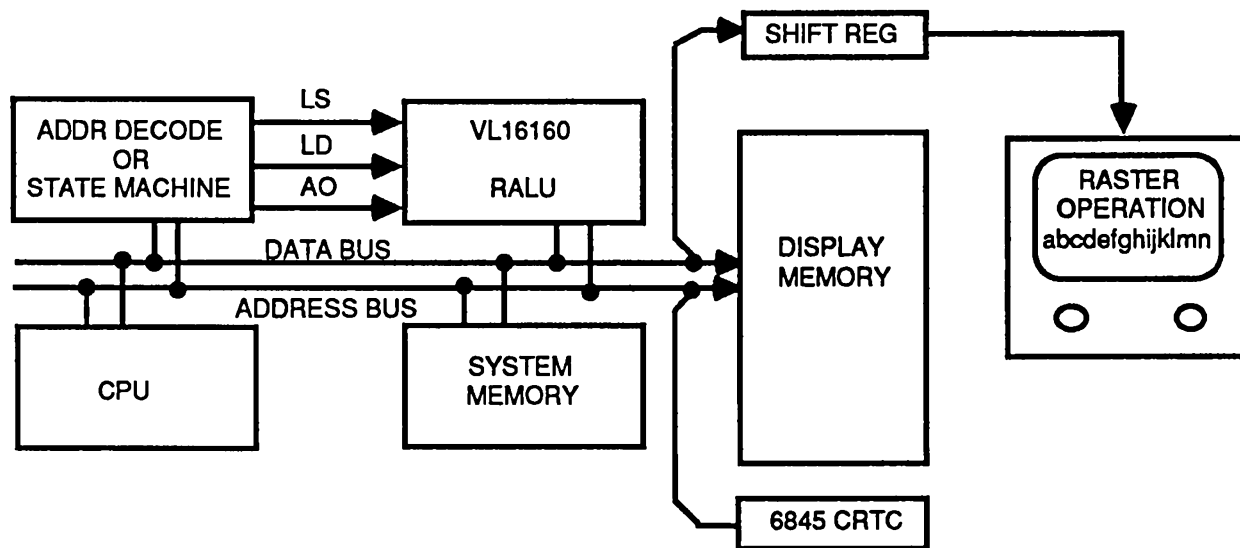


FIGURE 5. TYPICAL APPLICATION



ASYNCHRONOUS COMMUNICATIONS ELEMENT

FEATURES

- Full double buffering
- Independent control of transmit, receive, line status and data set interrupts
- Modem control signals include -CTS, -RTS, -DSR, -DTR, -RI and -DCD
- Programmable serial interface characteristics:
 - 5-, 6-, 7- or 8-bit characters
 - Even-, odd-, or no-parity bit generation and detection
 - 1-, 1 1/2- or 2-stop bit generation
 - Baud rate generation (dc to 56K baud)
- Full status reporting capabilities
- Three-state TTL drive capabilities for bidirectional data bus and control bus

DESCRIPTIONS

The VL16C450 is an asynchronous communications element (ACE) that is functionally equivalent to the VL82C50A, but is an improved specification version of that part. The improved specifications provide ensured compatibility with state-of-the-art CPUs.

The VL16C450, VL82C50A, and VL82C50 ACEs serve as serial data input/output interface in microcomputer systems. They perform serial-to-parallel conversion on data characters received from peripheral devices or modems, and parallel-to-serial conversion on data characters transmitted by

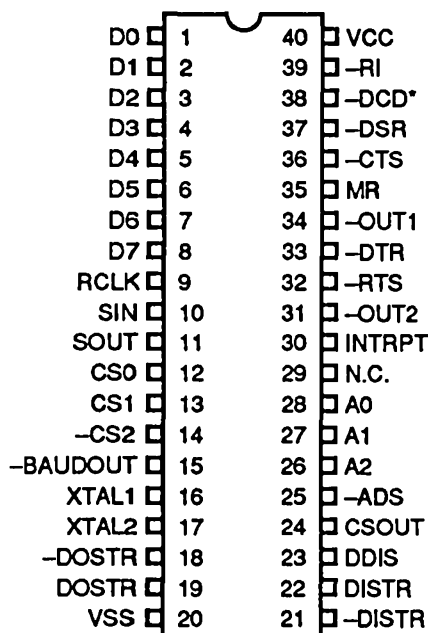
the CPU. The complete status of the ACE can be read at any time during functional operation by the CPU. The information obtained includes the type and condition of the transfer operations being performed, and error conditions involving parity, overrun, framing, or break interrupt.

A programmable baud rate generation is included that can divide the timing reference clock input by a divisor between 1 and $(2^{16}-1)$.

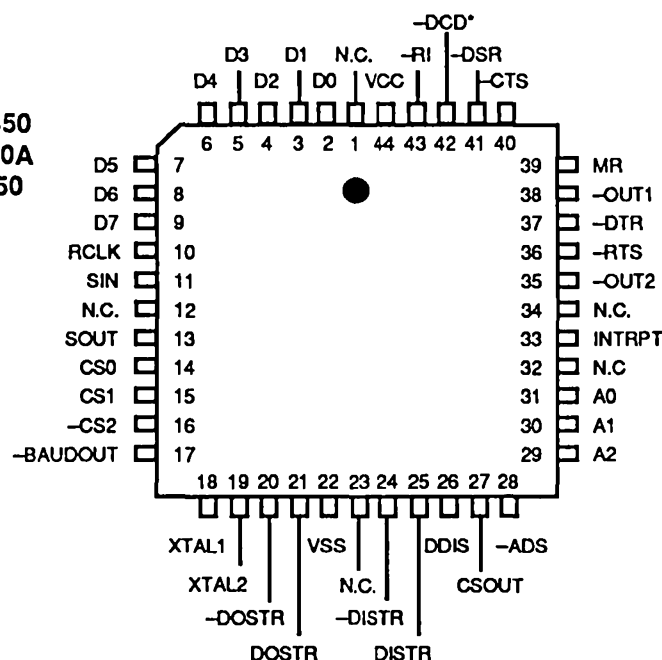
The VLSI family of ACEs is available packaged in plastic leaded chip carrier as well as a plastic and ceramic DIP.

PIN DIAGRAMS

**VL16C450
VL82C50A
VL82C50**



**VL16C450
VL82C50A
VL82C50**



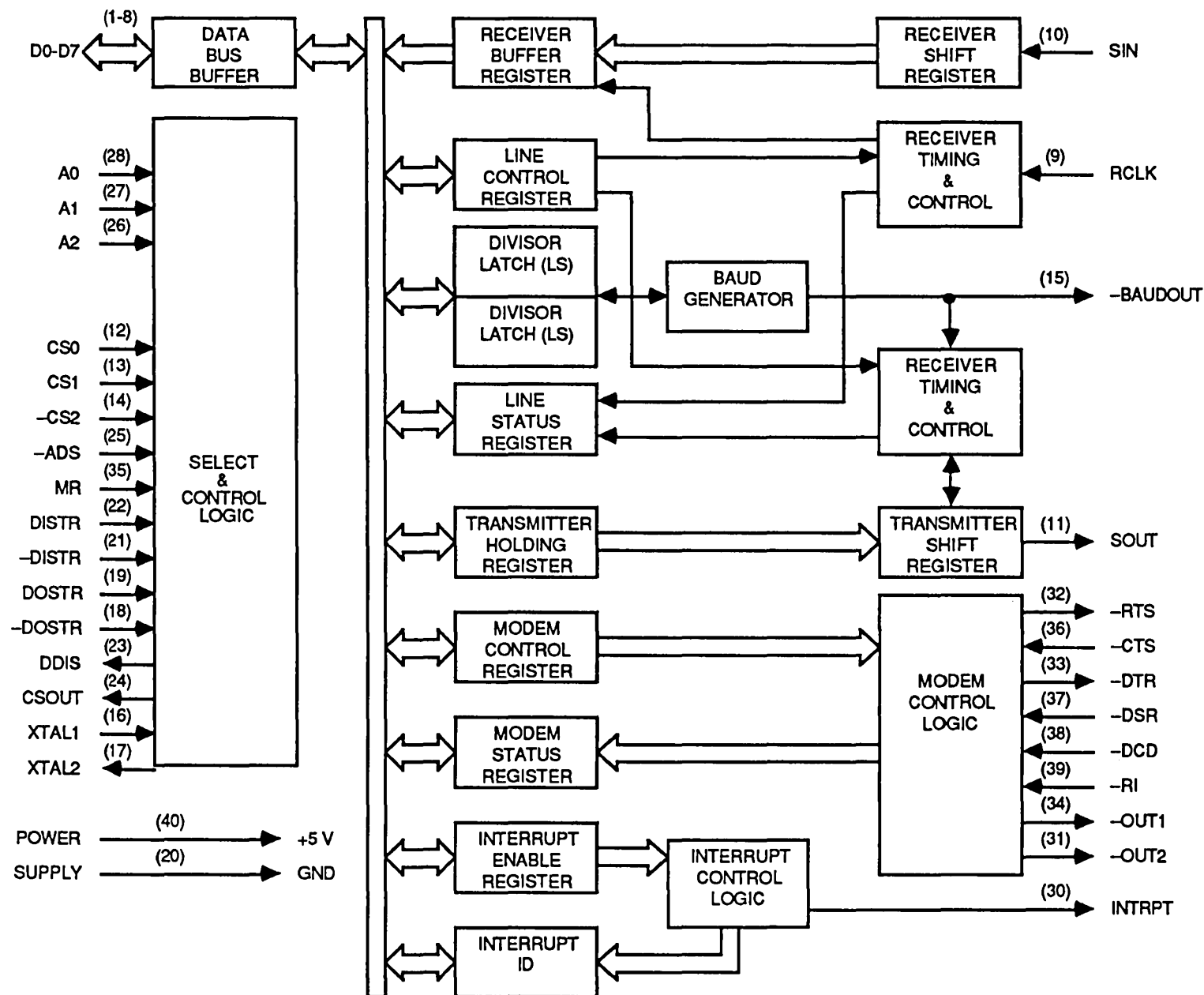
*On the VL82C50, Pin 38 (Pin 42 on the PLCC package) is also called -RLSD.

ORDER INFORMATION

Part Number	Clock Frequency	Package
VL16C450-PC VL16C450-CC VL16C450-QC	3.1 MHz	Plastic DIP Ceramic DIP Plastic Leaded Chip Carrier (PLCC)
VL82C50A-PC VL82C50A-CC VL82C50A-QC	3.1 MHz	Plastic DIP Ceramic DIP Plastic Leaded Chip Carrier (PLCC)
VL82C50-PC VL82C50-CC VL82C50-QC	3.1 MHz	Plastic DIP Ceramic DIP Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range is 0°C to + 70°C.

BLOCK DIAGRAM



Note: Applicable pin numbers (DIP) are included within parentheses.

SIGNAL DESCRIPTIONS

Signal Name	Pin Number (DIP)	Signal Type	Signal Description
D0-D7	1-8	I/O	Data Bits 0 through 7 - The Data Bus provides eight, three-state I/O lines for the transfer of data, control and status information between the ACE and the CPU. These lines are normally in a high-impedance state except during read operations. D0 is the least significant bit (LSB) and is the first serial data bit to be received or transmitted.
RCLK	9	I	Receive Clock Input - The external clock input to the UART baud rate divisor.
SIN	10	I	Serial Data Input - The serial data input moves information from the communication line or modem to the ACE receiver circuits. A mark (1) is high, and a space (0) is low. Data on serial data input is disabled when operating in the Loop Mode.
SOUT	11	O	Serial Data Output - This line is the serial data output from the UART's transmitter circuitry. A mark (1) is a logic "one" (high) and space (0) is a logic "zero" (low). SOUT is held in the mark condition when the transmitter is disabled, Reset is true, the Transmitter Register is empty, or when in the Loop Mode.
CS0, CS1, CS2	12-14	I	Chip Selects - The Chip Select inputs act as an enable for the device. When $\overline{\text{CS2}}$ is low and CS0 and CS1 are both high, the chip is selected.
$\overline{\text{BAUDOUT}}$	15	O	Baud Rate Output - This output signal for the transmitter section is equal to the internal reference frequency, divided by the selected divisor.
XTAL1	16	I	Crystal Input Pin 1 - Input for external timing reference input or pin of crystal (See Basic Configuration).
XTAL2	17	I	Crystal Input Pin 2 - Input for pin of crystal (See Basic Configuration).
$\overline{\text{DOSTR}}$	18	I	Input/Output Write Strobe - This is an active low input which causes data from the data bus (D0-D7) to be input to the UART.
DOSTR	19	I	Input/Output Write Strobe - Same as $\overline{\text{DOSTR}}$, but uses an active high input.
VSS	20		Ground (0 V).
$\overline{\text{DISTR}}$	21	I	Input/Output Read Strobe - This is an active low input which causes the serial channel to output data to the data bus (DB0-DB7).
DISTR	22	I	Input/Output Read Strobe - Same as $\overline{\text{DISTR}}$, but uses an active high input.
DDIS	23	O	Driver Disable - This pin goes low whenever the microprocessor is reading data from the ACE. This signal may be used to disable an external transceiver.
CSOUT	24	O	Chip Select Out - A high on this pin indicates that the chip has been selected by the chip select input pins.
$\overline{\text{ADS}}$	25	I	Address Strobe Input - When this pin is low, the state of the Register Select and Chip Select pins is latched internally.
A0-A2	28-26	I	Address Lines A0-A2 - The address lines select the internal registers during CPU bus operations.
NC	29		No Connection.
INTRPT	30	O	Interrupt Output - This pin goes high (when enabled by the Interrupt Enable Register) whenever a Receiver Error Flag, Received Data Available, Transmitter Holding Register Empty, or Modem Status condition is detected.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number (DIP)	Signal Type	Signal Description
–OUT2	31	O	Output 2 - User defined output that can be set to an active low by programming bit 3 of the Modem Control Register to a high level.
–RTS	32	O	Request to Send - The –RTS signal is an output on the UART used to enable the modem. The –RTS pin is set low by writing a logic 1 to MCR bit 1 of the UART's Modem Control Register. The –RTS pin is reset high by Reset. A low on the –RTS pin indicates to the ACE that the UART has data ready to transmit.
–DTR	33	O	Data Terminal Ready - The DTR pin can be set (low) by writing a logic 1 to MCR, Modem Control Register bit 0 of the UART. This signal is cleared (high) by writing a logic 0 to the DTR bit (MCR) or whenever a reset occurs. When active (low), the DTR pin indicates to the ACE that the UART is ready to receive data.
–OUT1	34	O	Output 1 - User defined output that can be set to an active low by programming bit 2 of the Modem Control Register to a high level.
MR	35	I	Master Reset - When high, the reset input forces the ACE into an idle mode in which all data activities are suspended. The Modem Control Register (MCR) along with its output, is cleared. The Line Status Register (LSR) is cleared except for the THRE and TEMT bits, which are set. All functions of the device remain in an idle state until programmed to resume activities.
–CTS	36	I	Clear to Send - The logical state of the –CTS pin is reflected in the CTS bit of the (MSR) Modem Status Register [CTS is bit 4 of the MSR, written MSR(4)] of the UART. A change of state of the –CTS pin, since the previous reading of the MSR causes the setting of DCTS in the Modem Status Register. When the –CTS pin is low, the modem is indicating that data on SOUT can be transmitted.
–DSR	37	I	Data Set Ready - The logical state of the –DSR pin is reflected in MSR(5) of the Modem Status Register. DDSR MSR(1) indicates whether the –DSR pin has changed state since the previous reading of the MSR. When the –DSR pin is low, the modem is indicating that it is ready to exchange data with the UART.
–DCD (–RLSD)	38	I	Data Carrier Detect (Receive Line Signal Detect) - When low, the –DCD (–RLSD) indicates that the data carrier has been detected by the modem or data set. –DCD (–RLSD) is a modem input whose condition can be tested by the CPU by reading MSR(7) (DCD or RLSD) of the Modem Status Register. MSR(3) (DDCD or DRLSD) of the Modem Status Register indicates whether the –DCD (–RLSD) input has changed since the previous reading of the MSR. –DCD (–RLSD) has no effect on the receiver. If the –DCD (–RLSD) changes state with the modem status interrupt enabled, an interrupt occurs.
–RI	39	I	Ring Indicator Input - When low, –RI indicates that a telephone ringing signal has been received by the modem or data set. The –RI signal is a modem control input whose condition is tested by reading MSR(6) (RI) of the UART. The Modem Status Register output TERI MSR(2) indicates whether the RI input has changed from high to low since the previous reading of the MSR. If the interrupt is enabled IER(3) = 1 and –RI changes from a high to low, an interrupt is generated.
VCC	40		Power Supply - The power supply requirement is 5 V \pm 5%.

REGISTERS

Three types of internal registers are used in the serial channel of each ACE. They are used in the operation of the device, and are the control, status, and data registers. The control registers are the Bit Rate Select Register DLL (Divisor Latch LSB) and DLM (Divisor Latch MSB), Line Control Register, Interrupt Enable Register, and the Modem Control registers, while the status registers are the Line Status Registers and the Modem Status Register. The data registers are the Receiver Buffer Register and the Transmitter Holding Register. The Address, Read, and Write inputs are used in conjunction with the Divisor Latch Access Bit in the Line Control Register [LCR(7)] to select the register to be written or read (see Table 1). Individual bits within these registers are referred to by the register mnemonic and the bit number in parenthesis. As an example, LCR(7) refers to Line Control Register Bit 7.

The Transmitter Buffer Register and Receiver Buffer Register are data registers that hold from five to eight bits of data. If less than eight data bits are transmitted, data is right justified to the

LSB. Bit 0 of a data word is always the first serial data bit received and transmitted. The ACE data registers are double-buffered so that read and write operations may be performed when the UART is performing the parallel-to-serial or serial-to-parallel conversion.

The format of the data character is controlled by the Line Control Register. The contents of the LCR may be read, eliminating the need for separate storage of the line characteristics in system memory. The contents of the LCR are described below:

- LCR (0) Word Length Select Bit 0 (WLS0)
- LCR (1) Word Length Select Bit 1 (WLS1)
- LCR (2) Stop Bit Select (STB)
- LCR (3) Parity Enable (PEN)
- LCR (4) Even Parity Select (EPS)
- LCR (5) Stick Parity
- LCR (6) Set Break
- LCR (7) Divisor Latch Access Bit (DLAB)

LCR(0) and LCR(1) word length select bit 1: The number of bits in each serial character is programmed as shown in Table 2.

TABLE 2. WORD LENGTH SELECT

LCR(1)	LCR(0)	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

LCR(2) Stop Bit Select: LCR(2) specifies the number of stop bits in each transmitted character. If LCR(2) is a logic 1 when a 5-bit word length is selected, 1.5 stop bits are generated. If LCR(2) is a logic 1 when either a 6-, 7-, or 8-bit word length is selected, two stop bits are generated. The receiver checks for two stop bits if programmed to do so.

LCR(3) Parity Enable: When LCR(3) is high, a parity bit between the last data word bit and stop bit is generated and checked.

LCR(4) Even Parity Select: When parity is enabled [LCR(3) = 1], LCR(4) = 0 selects odd parity, and LCR(4) = 1 selects even parity.

LCR(5) Stick Parity: When parity is enabled [LCR(3) = 1], CLR(5) = 1 causes the transmission and reception of a parity bit to be in the opposite state from that indicated by LCR(4). This allows forced parity to a known state and the receiver to check the parity bit in a known state.

LCR(6) Break Control: When LCR(6) is set to a logic "1", the serial output (SOUT) is forced to the spacing (logic 0) state. The break is disabled by setting LCR(6) to a logic "0". The Break Control bit acts only on SOUT and does not effect on the transmitter logic. Break Control enables the CPU to alert a terminal in a computer communications system. If the following sequence is used, no invalid characters will be transmitted because of the break.

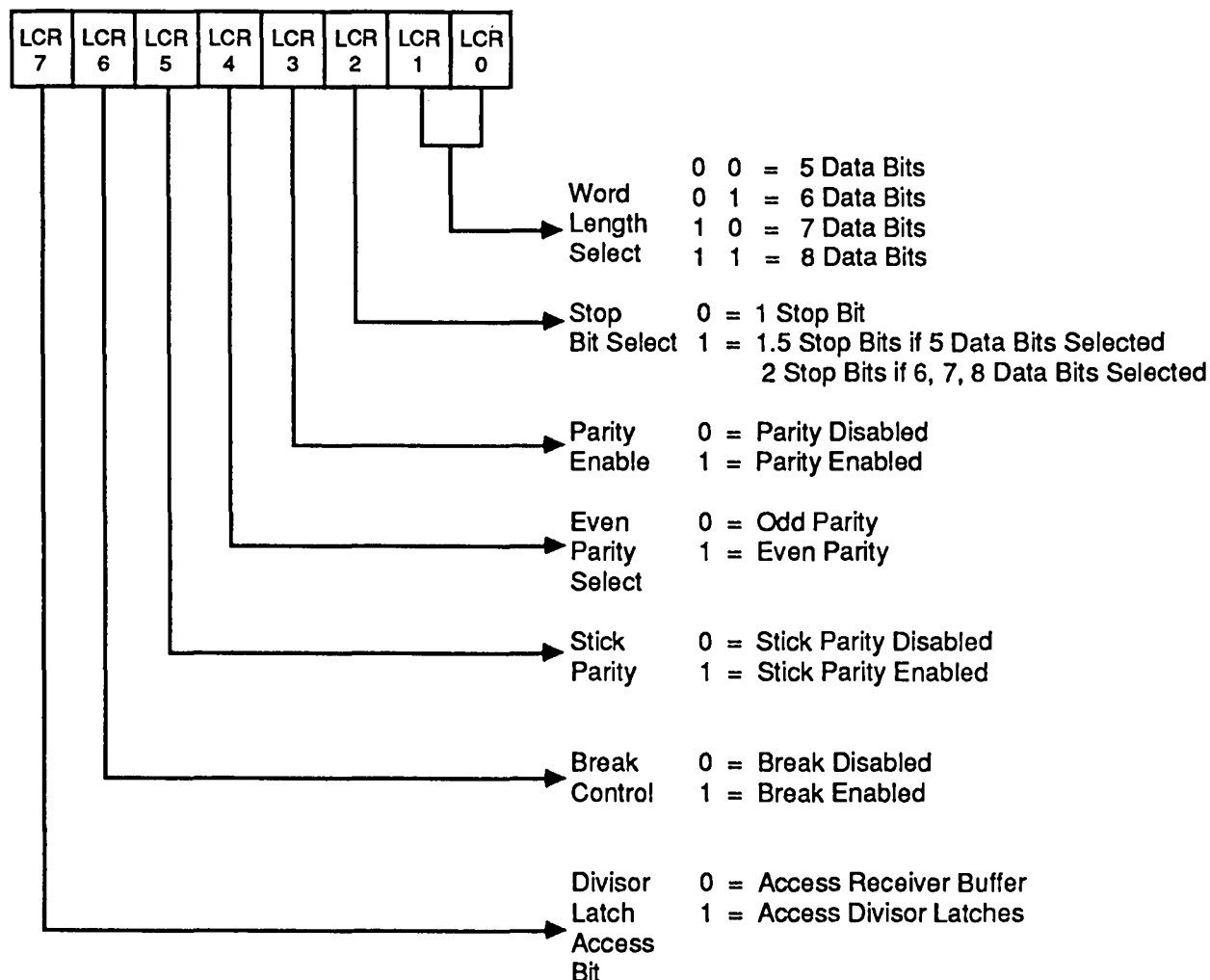
1. Load all "0"s pad character in response to THRE.
2. Set the break in response to the next THRE.
3. Wait for the transmitter to be idle (TEMT = 1), then clear the break when the normal transmission has to be restored.

TABLE 1. SERIAL CHANNEL INTERNAL REGISTERS

DLAB	A2	A1	A0	Mnemonic	Register
0	0	0	0	RBR	Receiver Buffer Register (read only)
0	0	0	0	THR	Transmitter Holding Register (write only)
0	0	0	1	IER	Interrupt Enable Register
X	0	1	0	IIR	Interrupt Identification Register (read only)
X	0	1	1	LCR	Line Control Register
X	1	0	0	MCR	Modem Control Register
X	1	0	1	LSR	Line Status Register
X	1	1	0	MSR	Modem Status Register
X	1	1	1	SCR	Scratch Register
1	0	0	0	DLL	Divisor Latch (LSB)
1	0	0	1	DLM	Divisor Latch (MSB)

X = "Don't Care" 0 = Logic Low 1 = Logic High

Note: The serial channel is accessed when CS0 is low.

FIGURE 1. LINE CONTROL REGISTER


LCR(7) Divisor Latch Access Bit (DLAB); LCR(7) must be set high (logic "1") to access the Divisor Latches DLL and DLM of the Baud Rate Generator during a read or write operation. LCR(7) must be input low to access the Receiver Buffer, the Transmitter Holding, or the Interrupt Enable Registers.

The Line Status Register (LSR) is a single register that provides status indications. The LSR is usually the first register read by the CPU to determine the cause of an interrupt or to poll the status the serial channel of the ACE.

Three error flags OE, FE, and PE provide the status of any error conditions detected in the receiver circuitry. During reception of the stop bits, the error flags are set high by an error condition. The error flags are not reset by the absence of an error condition in the next received character. The flags reflect the last character only if no overrun occurred. The Overrun Error character in the

Receiver Buffer Register has been overwritten by a character from the Receiver Shift Register before being read by the CPU. The character is thereby lost. Framing Error (FE) indicates that the last character received contained incorrect (low) stop bits. This is caused by the absence of the required stop bit or by a stop bit too short to be detected. Parity Error (PE) indicates that the last character received had a parity error based on the programmed and calculated parity of the received character.

The Break Interrupt (BI) status bit indicates that the last character received was a break character. A break character is an invalid data character. However, it is an entire character, including parity and stop bits.

The Transmitter Holding Register Empty (THRE) bit indicates that the THR register is empty and may receive another character. The Transmission

Shift Register Empty (TEMT) bit indicates that the Transmitter Shift Register is empty, and the serial channel has completed transmission of the last character to be sent. If the interrupt is enabled [IER(1)], an active THRE causes an interrupt (INTRPT).

The Data Ready (DR) bit indicates that the RBR has been loaded with a received character (including Break) and that the CPU may access this data.

Reading the LSR clears LSR(1)-LSR(4). (OE, PE, FE, and BI.)

The Line Status Register shown in Table 3 is described below:

LSR(0) Data Ready (DR): Data Ready is set high when an incoming character has been received and transferred into the Receiver Buffer Register. LSR(0) is reset low by a CPU read of the data in the Receiver Buffer Register.

LSR(1) Overrun Error (OE): Overrun Error indicates that data in the Receiver

TABLE 3. LINE STATUS REGISTER BITS

LSR BITS	Logic 1	Logic 0
LSR(0) Data Ready (DR)	Ready	Not Ready
LSR(1) Overrun Error (OE)	Error	No Error
LSR(2) Parity Error (PE)	Error	No Error
LSR(3) Framing Error (FE)	Error	No Error
LSR(4) Break Interrupt (BI)	Break	No Break
LSR(5) Transmitter Holding Register Empty (THRE)	Empty	Not Empty
LSR(6) Transmitter Empty (TEMT)	Empty	Not Empty
LSR(7) Not Used		

Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, overwriting the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.

LSR(2) Parity Error (PE): Parity Error indicates that the received data character does not have the correct even or odd parity, as selected by the Even Parity Select bit LCR(4). The PE bit is set high upon detection of a parity error, and is reset low when the CPU reads the contents of the LSR.

LSR(3) Framing Error (FE): Framing Error indicates that the received character did not have a valid stop bit. LSR(3) is set high when the stop bit following the last data bit or parity bit is detected as a zero bit (spacing level). The FE indicator is reset low when the CPU reads the contents of the LSR.

LSR(4) Break Interrupt (BI): Break Interrupt is set high when the received data input is held in the spacing (logic 0) state for longer than a full word transmission time (start bit + data bits + parity + stop bits). The BI indicator is reset when the CPU reads the contents of the Line Status Register.

LSR(1) - LSR(4) are the error conditions that produce a Receiver Line Status interrupt (priority 1 interrupt in the Interrupt Identification Register (IIR)) when any of the conditions are detected. This interrupt is enabled by setting IER(2) = 1 in the Interrupt Enable Register.

LSR(5) Transmitter Holding Register Empty (THRE): THRE indicates that the ACE is ready to accept a new character for transmission. The THRE bit is set high when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. LSR(5) is reset low by the loading the Transmitter Holding Register by the CPU. LSR(5) is reset low by the loading of the Transmitter Holding Register by the CPU. LSR(5) is not reset by a CPU read of the LSR.

When the THRE interrupt is enabled IER(1). THRE causes a priority 3 interrupt in the IIR. If THRE is the interrupt source indicated in IIR, INTRPT is cleared by a read of the IIR.

LSR(6) Transmitter Empty (TEMT): TEMT is set high when the Transmitter Holding Register (THR) and the Transmitter Shift Register (TSR) are both empty. LSR(6) is reset low when a character is loaded into the THR and remains low until the character is transferred out of SOUT. TEMT is not

reset low by a CPU read of the LSR.

LSR(7): This bit is always 0.

The Modem Control Register (MCR) controls the interface with the modem or data set as described in Table 4 and Figure 2. MCR can be written and read. The -RTS and -DTR outputs are directly controlled by their control bits in this register. A high input asserts a low (true) at the output pins. MCR Bits 0, 1, 3, and 4 are shown below:

MCR(0): When MCR(0) is set high, the -DTR output is forced low. When MCR(0) is reset low, the -DTR output is forced high. The -DTR output of the serial channel may be input into an inverting line driver in order to obtain the proper polarity input at the modem or data set.

MCR(1): When MCR(1) is set high, the RTS output is forced low. When MCR(1) is reset low, the -RTS output is forced high.

MCR(2): The -RTS output of the serial channel may be input into an inverting line driver in order to obtain the proper polarity input at the modem or data set.

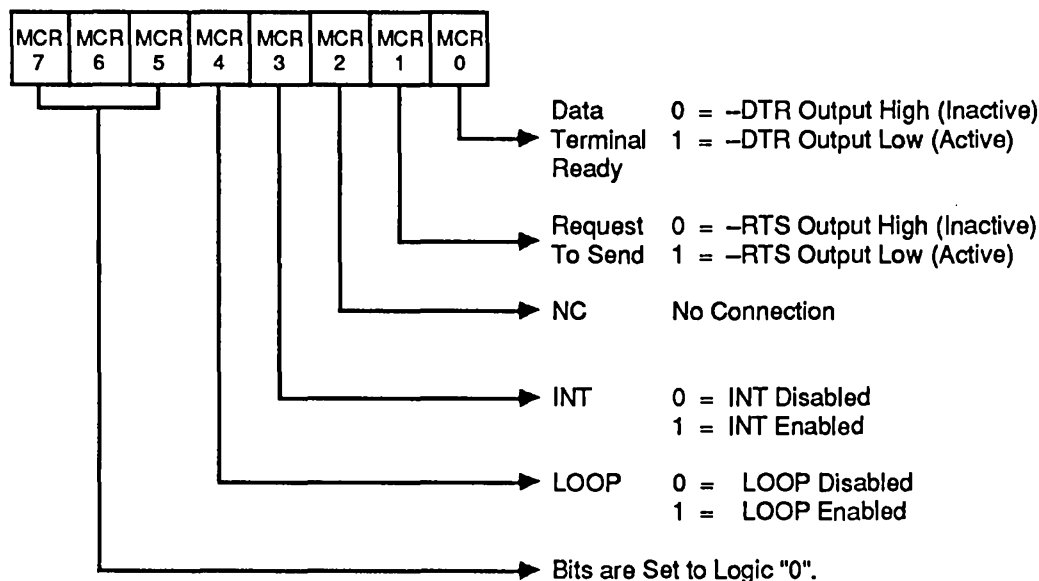
MCR(3): When MCR(3) is set high, the -OUT1 or -OUT2 output is forced high.

MCR(4): MCR(4) provides a local loopback feature for diagnostic testing of the channel. When MCR(4) is set high, Serial Output (SOUT) is set to the marking (logic "1") state, and the receiver data input Serial Input (SIN) is disconnected. The output of the Transmitter Shift Register is looped back into the Receiver Shift Register input. The three

TABLE 4. MODEM CONTROL REGISTER BITS

MCR Bits	Logic 1	Logic 0
MCR(0) Data Terminal Ready (DTR)	-DTR Output Low	-DTR Output High
MCR(1) Request to Send (RTS)	-RTS Output Low	-RTS Output High
MCR(2) OUT1	-OUT1 Output Low	-OUT1 Output High
MCR(3) OUT2	-OUT2 Output Low	-OUT2 Output High
MCR(4) LOOP	Loop Enabled	Loop Disabled
MCR(5) 0		
MCR(6) 0		
MCR(7) 0		

FIGURE 2. MODEM CONTROL REGISTER



modem control inputs (-CTS, -DSR, and -RI) are disconnected. The modem control outputs (-DTR and -RTS) are internally connected to the four modem control inputs. The modem control output pins are forced to their inactive state (high).

In the diagnostic mode, data transmitted is immediately received. This allows the processor to verify the transmit and receive data paths of the selected serial channel. Bits MCR(5) - MCR(7) are permanently set to logic 0.

The MSR provides the CPU with status of the modem input lines from the modem or peripheral devices. The MSR allows the CPU to read the serial channel modem signal inputs by accessing the data bus interface of the ACE in addition to the current status information, four bits of the MSR indicate whether the modem inputs have changed since the last reading of the MSR. The delta status bits are set high when a control input from the modem changes state, and reset low when the CPU reads the MSR.

The modem input lines for the channel are -CTS, -DSR, -RI, and -RLSD. MSR(4) - MSR(7) are status indications of these lines. The status indications follow the status of the input lines. If the modem status interrupt in the Interrupt Enable Register is enabled [IER(3)], a change of state in a modem input signals will be reflected by the modem status

bits in the IIR register, and an interrupt (INTRPT) is generated. The MSR is a priority 4 interrupt. The contents of the Modem Status Register are described in Table 5. Note that the state (high or low) of the status bits are inverted versions of the actual input pins.

MSR(0) Delta Clear to Send (DCTS): DCTS displays that the -CTS input to the serial channel has changed state since it was read last by the CPU.

MSR(1) Delta Data Set Ready (DDSR): DDSR indicates that the -DSR input to the serial channel has changed state since the last time it was read by the CPU.

MSR(2) Trailing Edge of Ring Indicator (TERI): TERI indicates that the -RI input to the serial channel has changed state from high to low since the last time it was read by the CPU. Low to high transitions on -RI do not activate TERI.

MSR(3) Delta Data Carrier Detect (DRSLD): DRSLD indicates that the -RSLD input to the serial channel has changed state since the last time it was read by the CPU.

MSR(4) Clear to Send (CTS): Clear to Send (CTS) is the status of the -CTS input from the modem indicating to the serial channel that the modem is ready to receive data from the serial channel's transmitter output (SOUT). If the serial channel is in loop mode [MSR(4) = 1], MSR(4) is equivalent to -RTS in the MCR.

MSR(5) Data Set Ready (DSR): Data Set Ready (DSR) is a status of the -DSR input from the modem to the serial channel which indicates that the modem is ready to provide received data to the serial channel receiver circuitry. If the channel is in the loop mode [MCR(4) = 1], MSR(5) is equivalent to the DTR in the MCR.

TABLE 5. MODEM STATUS REGISTER BITS

MSR Bit	Mnemonic	Description
MSR(0)	DCTS	Delta Clear To Send
MSR(1)	DDSR	Delta Data Set Ready
MSR(2)	TERI	Trailing Edge of Ring Indicator
MSR(3)	DRLSD	Delta Data Carrier Detect
MSR(4)	-CTS	Clear To Send
MSR(5)	-DSR	Data Set Ready
MSR(6)	-RI	Ring Indicator
MSR(7)	-RLSD	Receiver Line Signal Detect

MSR(6) Ring Indicator (RI): Indicates the status of the RI input (pin 39). If the channel is in the loop mode (MCR(4) = 1), (6) is not connected in the MCR.

MSR(7) Receive Line Signal Detect (RLSD): Receive Line Signal Detect indicates the status of the Receive Line Signal Detect (–RLSD) input. If the channel is in the loop mode (MCR(4)–1), MSR(4) is equivalent to OUT2 of the MCR.

The modem status inputs (–RI, –RLSD, –DSR, and –CTS) reflect the modem input lines with any change of status. Reading the MSR register will clear the delta modem status indications but has no effect on the status bits. The status bits reflect the state of the input pins regardless of the mask control signals. If a DCTS, DDSR, TERI, or DRLSD are true, and a state change occurs during a read operation (–DISTR), the state change is not indicated in the MSR. If DCTS, DDSR, TERI, or DRLSD are false, and a state change occurs during a read operation, the state change is indicated after the read operation.

For LSR and MSR, the setting of status bits is inhibited during status register read –DISTR operations. If a status condition is generated during a read –DISTR operation, the status bit is not set until the trailing edge of the read –DISTR.

If a status bit is set during a read –DISTR operation, and the same status condition occurs, that status bit will be cleared at the trailing edge of the read –DISTR instead of being set again.

The ACE serial channel contains a programmable Baud Rate Generator (BRG) that divides the clock (DC to 3.1 MHz) by any divisor from 1 to 2^{16-1} (see also BRG description). The output frequency of the Baud Generator is 16X the data rate [divisor # = clock ÷ (baud rate × 16)]. Two 8-bit divisor latch registers store the divisor in a 16-bit binary format. These Divisor Latch registers must be loaded during initialization. Upon loading either of the Divisor Latches, a 16-bit baud counter is immediately loaded. This prevents long counts on initial load.

The receiver circuitry in the serial channel of the ACE is programmable for 5, 6, 7, or 8 data bits per character. For

words of less than 8 bits, the data is right justified to the least significant bit LSB = Data Bit 0 [RBR(0)]. Data Bit 0 of a data word [RBR(0)] is the first data bit received. The unused bits in a character less than 8 bits are output low to the parallel output by the serial channel.

Received data at the SIN input pin is shifted into the Receiver Shift Register by the 16X clock provided at the CLK input. This clock is synchronized to the incoming data based on the position of the start bit. When a complete character is shifted into the Receiver Shift Register, the assembled data bits are parallel loaded into the Receiver Buffer Register. The DR flag in the LSR register is set.

Double buffering of the received data permits continuous reception of data without losing received data. While the Receiver Shift Register is shifting a new character into the serial channel, the Receiver Buffer Register is holding a previously received character for the CPU to read. Failure to read the data in the RBR before complete reception of the next character result in the low of the data in the Receiver Register. The OE flag in the LSR register indicates the overrun condition.

RBR Bits 0 through 7:

RBR(0)	Data Bit 0
RBR(1)	Data Bit 1
RBR(2)	Data Bit 2
RBR(3)	Data Bit 3
RBR(4)	Data Bit 4
RBR(5)	Data Bit 5
RBR(6)	Data Bit 6
RBR(7)	Data Bit 7

The Transmitter Holding Register (THR) holds parallel data from the data bus (D0–D7) until the Transmitter Shift Register is empty and ready to accept a new character for transmission. The transmitter and receiver word length and number of stop bits are the same. If the character is less than eight bits, unused bits at the microprocessor data bus are ignored by the transmitter.

Data Bit 0 (THR(0)) is the first serial data bit transmitted. The THRE flag (LSR(5)) reflect the status of the THR. The TEMT flag (LSR(5)) indicates if both the THR and TSR are empty.

THR Bits 0 through 7:

THR(0)	Data Bit 0
THR(1)	Data Bit 1
THR(2)	Data Bit 2
THR(3)	Data Bit 3
THR(4)	Data Bit 4
THR(5)	Data Bit 5
THR(6)	Data Bit 6
THR(7)	Data Bit 7

Scratchpad Register is an 8-bit Read/Write register that has no effect on either channel in the ACE. It is intended to be used by the programmer to hold data temporarily.

SCR Bits 0 through 7:

SCR(0)	Data Bit 0
SCR(1)	Data Bit 1
SCR(2)	Data Bit 2
SCR(3)	Data Bit 3
SCR(4)	Data Bit 4
SCR(5)	Data Bit 5
SCR(6)	Data Bit 6
SCR(7)	Data Bit 7

INTERRUPTS

The Interrupt Identification Register (IIR) in the serial channel of the ACE has interrupt capability of interfacing to current microprocessors. In order to minimize software overhead during data character transfers, the serial channel prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows:

1. Receiver Line Status (priority 1)
2. Received Data Ready (priority 2)
3. Transmitter Holding Register Empty (priority 3)
4. Modem Status (priority 4)

Information indicating that a prioritized interrupt is pending and the type of interrupt is stored in the Interrupt Identification Register (IIR). When addressed during chip select time, the IIR indicates the highest priority interrupt pending. No other interrupts are acknowledged until the interrupt is serviced by the CPU. The contents of the IIR are indicated in Table 6 and are described below:

IIR(0): IIR(0) can be used in either a hard-wired prioritized or polled environment to indicate whether an interrupt is pending. When IIR(0) is low, an interrupt is pending, and IIR contents may be used as a pointer to the appropriate



TABLE 6. INTERRUPT IDENTIFICATION REGISTER

Interrupt Identification				Interrupt Set And Reset Functions		
Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Flag	Interrupt Source	Interrupt Reset Control
X	X	1		None	None	
1	1	0	First	Receiver Line Status	OE, PE FE, or BI	LSR Read
1	0	0	Second	Received Data Available	Received Data Available	RBR Read
0	1	0	Third	THRE	THRE	IIR Read if THRE is the Interrupt Source or THR Write
0	0	0	Fourth	Modem Status	-CTS, -DSR -RI, -RSLD	MSR Read

X = Not Defined.

TABLE 7. SERIAL CHANNEL ACCESSIBLE REGISTERS

Register Mnemonic	Register Bit Number							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RBR (Read Only)	Data Bit 7 (MSB)	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0 (LSB)*
THR (Write Only)	Data Bit 7	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0
DLL	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DLM	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
IER	0	0	0	0	(EDSSI) Enable Modem Status Interrupt	(ELSI) Enable Receiver Line Status Interrupt	(ETBEI) Enable Transmitter Holding Register Empty Interrupt	(ERBFI) Enable Received Data Available Interrupt
IIR (Read Only)	0	0	0	0	0	Interrupt ID Bit (1)	Interrupt ID Bit (0)	"0" 1F Interrupt Pending
LCR	(DLAB) Divisor Latch Access Bit	Set Break	Stick Parity	(EPS) Even Parity Select	(PEN) Parity Enable	(STB) Number of Stop Bits	(WLSB1) Word Length Select Bit 1	(WLSB0) Word Length Select Bit 0
MCR	0	0	0	Loop	Out 2	Out 1	(RTS) Request To Send	(DTR) Data Terminal Ready
LSR	0	(TEMT) Transmitter Empty	(THRE) Transmitter Holding Register Empty	(BI) Break Interrupt	(FE) Framing Error	(PE) Parity Error	(OE) Overrun Error	(DR) Data Ready
MSR	(DCD) Data Carrier Detect	(RI) Ring Indicator	(DSR) Data Ready Set	(CTS) Clear to Send	(DRSLD) Delta Receive Line Signal Detect	(TERI) Trailing Edge Ring Indicator	(DDSR) Delta Data Set Ready	(DCTS) Delta Clear to Send
SCR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

*LSB Data Bit 0 is the first bit transmitted or received.

interrupt service routine. When IIR(0) is high, no interrupt is pending.

IIR(1) and IIR(2) are used to identify the highest priority interrupt pending as indicated in Table 6.

IIR(3) - IIR(7): These five bits of the IIR are logic 0.

The Interrupt Enable Register (IER) is a Write register used to independently enable the four serial channel interrupts which activate the interrupt (INTRPT) output. All interrupts are disabled by resetting IER(0) - IER(3) of the Interrupt Enable Register. Interrupts are enabled by setting the appropriate bits of the IER high. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INTRPT output. All other system functions operate in their normal manner, including the setting of the Line Status and Modem Status Registers. The contents of the Interrupt Enable Register is described in Table 7 and below:

IER(0): When programmed high (IER(0) = Logic 1), IER(1) enables the Received Data Available interrupt.

IER(1): When programmed high (IER(1) = Logic 1), IER(1) enables the Transmitter Holding Register Empty interrupt.

IER(2): When programmed high (IER(2) = Logic 1), IER(2) enables the Receiver Line Status interrupt.

IER(3): When programmed high (IER(3) = Logic 1), IER(3) enables the Modem Status Interrupt.

IER(4) - IER(7): These four bits of the IER are logic 0.

TRANSMITTER

The serial transmitter section consists of a Transmitter Holding Register (THR), Transmitter Shift Register (TSR), and associated control logic. The Transmitter Holding Register Empty (THRE) and Transmitter Shift Register Empty (TEMT) are two bits in the Line Status Register which indicate the status of THR and TSR. To transmit a 5- to 8-bit word, the word is written through D0-D7 to the THR. The microprocessor should perform a write operation only if THRE is high. The THRE is set high when the word is automatically transferred from the THR to the TSR during the transmission of the start bit.

When the transmitter is idle, THRE and TEMT are high. The first word written causes THRE to be reset to 0. After the transfer, THRE returns high. TEMT remains low for at least the duration of the transmission of the data word. If a second character is transmitted to the THR, the THRE is reset low. Since the data word cannot be transferred from the THR to the TSR until the TSR is empty, THRE remains low until the TSR has completed sending the word. When the last word has been transmitted out of the TSR, TEMT is set high. THRE is set high one THR to TSR transfer time later.

RECEIVER

Serial asynchronous data is input into the SIN pin. The idle state of the line providing the input into SIN is high. A start bit detect circuit continually searches for a high to low transition from the idle state. When the transition is detected, a counter is reset, and counts the 16X clock to 7 1/2, which is the center of the start bit. The start bit is valid if the SIN is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the SIN input.

The Line Control Register determines the number of data bits in a character (LCR(0), LCR(1)), number of stop bits LCR(2), if parity is used LCR(3), and the polarity of parity LCR(4). Status for the receiver is provided in the Line Status Register to the Receiver Buffer Register, the Data Received indication in LSR(0) is set high. The CPU reads the Receiver Buffer Register through D0-D7. This read resets LSR(0). If D0-D7 are not read prior to a new character transfer from the RSR to the RBR, the overrun error status indication is set in LSR(1). The parity check tests for even or odd parity on the parity bit, which precedes the first stop bit. If there is a parity error, the parity error is set in LSR(2). There is circuitry which tests whether the stop bit is high. If it is not, a framing error indication is generated in LSR(3).

The center of the start bit is defined as clock count 7 1/2. If the data into SIN is symmetrical square wave, the center of the data cells will occur within $\pm 3.125\%$ of the actual center, providing an error margin of 46.875%. The start bit can

begin as much as one 16X clock cycle prior to being detected.

BAUD RATE GENERATOR (BRG)

The BRG generates the clocking for the UART function, providing standard ANSI/CCITT bit rates. The oscillator driving the BRG is provided by an external clock into CLK.

The data rate is determined by the Divisor Latch registers DLL and DLM and the external frequency. The bit rate is selected by programming the two divisor latches, Divisor Latch Most Significant Byte and Divisor Latch Least Significant Byte. Setting DLL = 1 and DLM = 0 selects the divisor to divide by 1 (divide by 1 gives maximum baud rate for a given input frequency at the CLK input).

The BRG can use any of three different popular frequencies to provide standard baud rates. These frequencies are 1.8432 MHz, 2.4576 MHz, and 3.072 MHz. With these frequencies, standard bit rates from 50 to 38.5k bps are available. Tables 8, 9, and 10 illustrate the divisors needed to obtain standard rates using these three crystal frequencies.

MASTER RESET

After power up, the ACE MR input should be held high for one microsecond to reset the ACE circuits to an idle mode until initialization. A high on MR causes the following:

1. Initializes the transmitter and receiver internal clock counters.
2. Clears the Line Status Register (LSR), except for Transmitter Shift Register Empty (TEMT) and Transmit Holding Register Empty (THRE), which are set. The Modem Control Register (MCR) is also cleared. All of the discrete lines, memory elements and miscellaneous logic associated with these register bits are also cleared or turned off. The Line Control Register (LCR), Divisor Latches, Receiver Buffer Register, Transmitter Buffer Register are not effected.

Following removal of the reset condition (Reset low), the ACE remains in the idle mode until programmed.



A hardware reset of the ACE sets the THRE and TEMT status bit in the LSR. When interrupts are subsequently enabled, and interrupt occurs due to THRE.

A summary of the effect of a reset on the ACE is given in Table 11.

PROGRAMMING

The serial channel of the ACE is programmed by the control register LCR, IER, DLL and DLM, and MCR. These control words define the character length, number of stop bits, parity, baud rate, and modem interface.

While the control register can be written in any order, the IER should be written to last because it controls the interrupt enables. Once the serial channel is programmed and operational, these registers can be updated any time the ACE serial channel is not transmitting or receiving data.

The control signals required to access each serial channel's internal registers are shown below.

SOFTWARE RESET

A software reset of the serial channel is a useful method for returning to a

completely known state without a system reset. Such a reset consists of writing to the LCR, Divisor Latches, and MCR registers. The LSR and RBR registers should be read prior to enabling interrupts in order to clear out any residual data or status bits which may be invalid for subsequent operation.

TABLE 8. BAUD RATES (1.8432 MHz CLOCK)

Desired Baud Rate	Divisor Used	Percent Error Difference Between Desired and Actual
50	2304	—
75	1536	—
110	1047	0.026
134.5	857	0.058
150	768	—
300	384	—
600	192	—
1200	96	—
1800	64	—
2000	58	0.69
2400	48	—
3600	32	—
4800	24	—
7200	16	—
9600	12	—
19200	6	—
38400	3	—
56000	2	2.86



TABLE 9. BAUD RATES (2.4576 MHz CLOCK)

Desired Baud Rate	Divisor Used	Percent Error Difference Between Desired and Actual
50	3072	—
75	2048	—
110	1396	0.026
134.5	1142	0.0007
150	1024	—
300	512	—
600	256	—
1200	128	—
1800	85	0.392
2000	77	0.260
2400	64	—
3600	43	0.775
4800	32	—
7200	21	1.587
9600	16	—
19200	8	—
38400	4	—

TABLE 10. BAUD RATES (3.072 MHz CLOCK)

Desired Baud Rate	Divisor Used	Percent Error Difference Between Desired and Actual
50	3840	—
75	2560	—
110	1745	0.026
134.5	1428	0.034
150	1280	—
300	640	—
600	320	—
1200	160	—
1800	107	0.312
2000	96	—
2400	80	—
3600	53	0.628
4800	40	—
7200	27	1.23
9600	20	—
19200	10	—
38400	5	—



TABLE 11. MASTER RESET

Register/Signal	Reset Control	Reset
Interrupt Enable Register	Reset	All Bits Low (0–3 forced and 4–7 permanent)
Interrupt Identification Register	Reset	Bit 0 is High, Bits 1 and 2 Low Bits 3–7 are Permanently Low
Line Control Register	Reset	All Bits Low
MODEM Control Register	Reset	All Bits Low
Line Status Register	Reset	All Bits Low, Except Bits 5 and 6 are High
MODEM Status Register	Reset	Bits 0–3 Low Bits 4–7 Input Signal
SOUT	Reset	High
Intrpt (RCVR Errs)	Read LSR/Reset	Low
Intrpt (RCVR Data Ready)	Read RBR/Reset	Low
Intrpt (THRE)	Read IIR/Write THR/Reset	Low
Intrpt (Modem Status Changes)	Read MSR/Reset	Low
–Out2	Reset	High
–RTS	Reset	High
–DTR	Reset	High
–Out1	Reset	High

**AC CHARACTERISTICS:** TA = 0°C to +70°C, VCC = 5 V ±5% (Note 1)

Symbol	Parameter	VL16C450		VL82C50A		VL82C50		Units	Conditions
		Min	Max	Min	Max	Min	Max		
tAW	Address Strobe Width	60		90		90		ns	
tAS	Address Setup Time	60		90		90		ns	
tAH	Address Hold Time	0		0		0		ns	
tCS	Chip Select Setup Time	60		90		90		ns	
tCH	Chip Select Hold Time	0		0		0		ns	
tDIW	–DISTR/DISTR Strobe Width	125		175		175		ns	
tRC	Read Cycle Delay	175		500		500		ns	
RC	Read Cycle = tAR(1) + tDIW + tRC	360		755		755		ns	
tDD	–DISTR/DISTR to Drive Disable Delay		60		75		75	ns	100 pF Load Note 3
tDDD	Delay from –DISTR/DISTR to Data		125		175		175	ns	100 pF Load
tHz	–DISTR/DISTR to Floating Data Delay	0	100	100		100		ns	100 pF Load Note 3
tDOW	–DOSTR/DOSTR Strobe Width	100		175		175		ns	
tWC	Write Cycle Delay	200		500		500		ns	
WC	Write Cycle = tAW* + tDOW + tWC	360		755		755		ns	
tDS	Data Setup Time	40		90		90		ns	
tDH	Data Hold Time	40		60		60		ns	
tCSC*	Chip Select Output Delay from Select		100		125		125	ns	100 pF Load
tRA*	Address Hold Time from –DISTR/DISTR	20		20		20		ns	Note 2
tRCS*	Chip Select Hold Time from –DISTR/DISTR	20		20		20		ns	Note 2
tAR*	–DISTR/DISTR Delay from Address	60		80		80		ns	Note 2
tCSR*	–DISTR/DISTR Delay from Chip Select	50		80		80		ns	Note 2
tWA*	Address Hold Time from –DOSTR/DOSTR	20		20		20		ns	Note 2
tWCS*	Chip Select Hold Time from –DOSTR/DOSTR	20		20		20		ns	Note 2
tAW*	–DOSTR/DOSTR Delay from Address	60		80		80		ns	Note 2
tCSW*	–DOSTR/DOSTR Delay from Select	50		80		80		ns	Note 2
tMRW	Master Reset Pulse Width	1		1		1		μs	
tXH	Duration of Clock High Pulse	140		140		140			
tXL	Duration of Clock Low Pulse	140		140		140			External Clock (3.1 MHz Max)

- Notes:** 1. All timings are referenced to valid 0 and valid 1. (See AC TEST POINTS.)
2. Applicable only when ADS is tied Low.
3. Charge and discharge time is determined by VOL, VOH and the external loading.

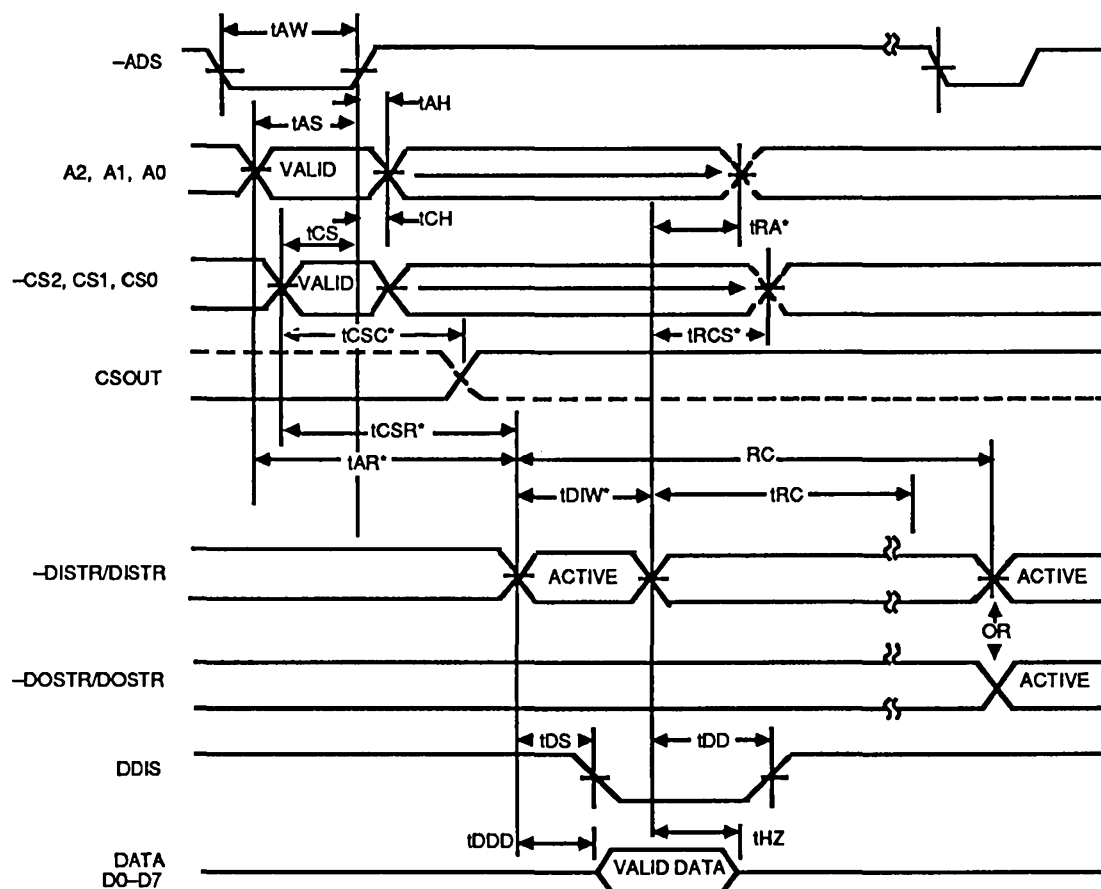
AC CHARACTERISTICS (Cont.): TA = 0°C to + 70°C, VCC = 5 V ±5% (Note 1)

Symbol	Parameter	VL16C450		VL82C50A		VL82C50		Units	Conditions
		Min	Max	Min	Max	Min	Max		
Transmitter									
tHR1	Delay from Rising Edge of –DOSTR/DOSTR (WR THR) to Reset Interrupt		175		1000		N/A	ns	100 pF Load
tHR2	Delay from Falling Edge of –DOSTR/DOSTR (WR THR) to Reset Interrupt		N/A		N/A		1000	ns	100 pF Load
tIRS	Delay from Initial INTR Reset Interrupt		16		16		16	–BAUDOUT CYCLES	
tSI	Delay from Initial Write to Interrupt	8	24	8	24	8	24	–BAUDOUT CYCLES	
tSS	Delay from Stop to Next Start		100		100		100	ns	
tSTI	Delay from Start Bit Low to Interrupt (THRE) High		8		8		8	–BAUDOUT CYCLES	
tIR	Delay from –DISTR/DISTR (RD IIR) to Reset Interrupt (THRE)		250		1000		1000	ns	100 pF Load
Modem Control									
tMDO	Delay from –DOSTR/DOSTR (WR MCR) to Output		250		1000		1000	ns	100 pF Load
tSIM	Delay to Set Interrupt from MODEM Input		250		1000		1000	ns	100 pF Load
tRIM	Delay to Reset Interrupt from –DISTR/DISTR (RS MSR)		250		1000		1000	ns	100 pF Load
Baud Generator									
N	Baud Divisor	1	2 ¹⁶ –1	1	2 ¹⁶ –1	1	2 ¹⁶ –1		
tBLD	Baud Output Negative Edge Delay		125		250		250	ns	100 pF Load
tBHD	Baud Output Positive Edge Delay		125		250		250	ns	100 pF Load
tLW	Baud Output Down Time	425		425		425		ns	fX = 2 MHz, +2, 100 pF Load
tHW	Baud Output Up Time	330		330		330		ns	fX = 2 MHz, +2, 100 pF Load
Receiver									
tSCD	Delay from RCLK to Sample Time		2		2		2	μs	
tSINT	Delay from Stop to Set Interrupt		1		1		1	μs	100 pF Load
tRINT	Delay from –DISTR/DISTR (RD RBR/RDLSR) to Reset Interrupt		1		1		1	μs	100 pF Load

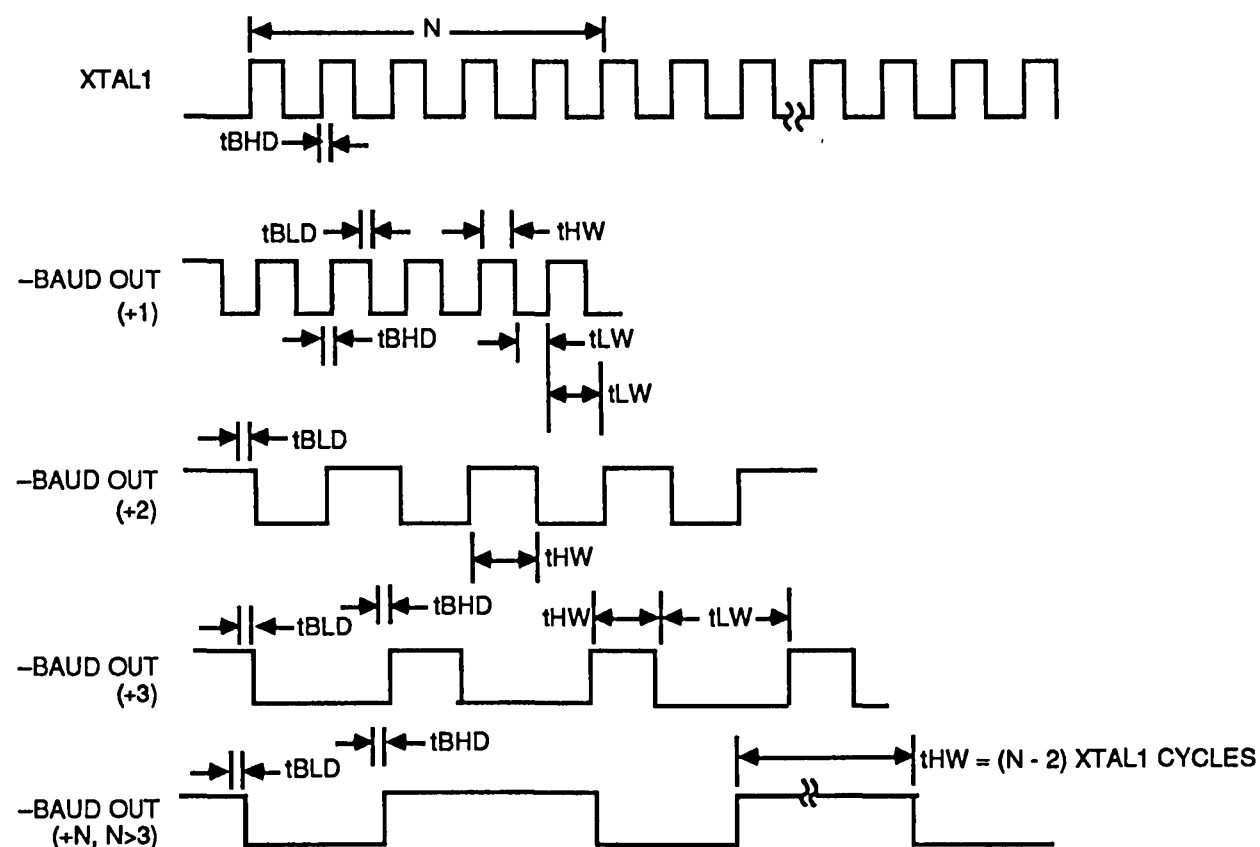
Note: 1. All timings are referenced to valid 0 and valid 1. (See AC TEST POINTS.)

TIMING DIAGRAMS

READ CYCLE

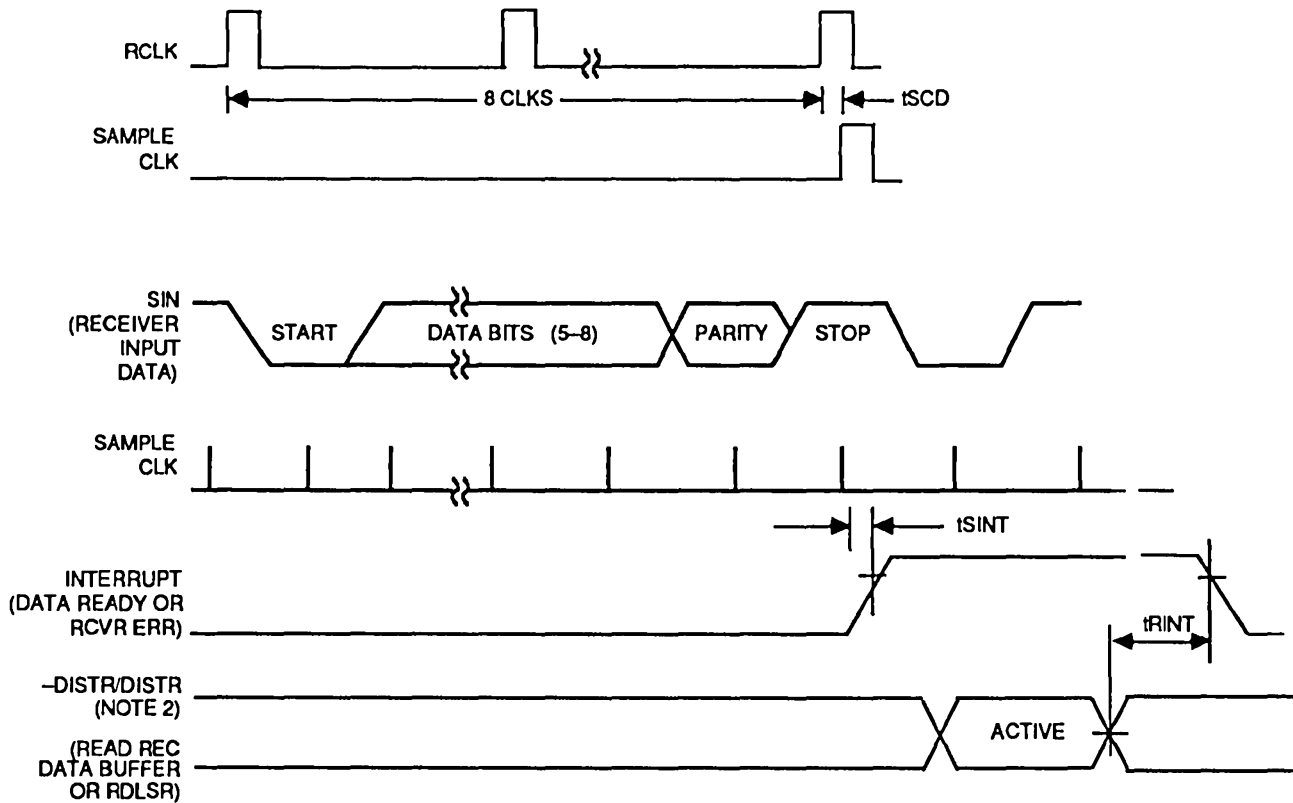


BAUDOUT

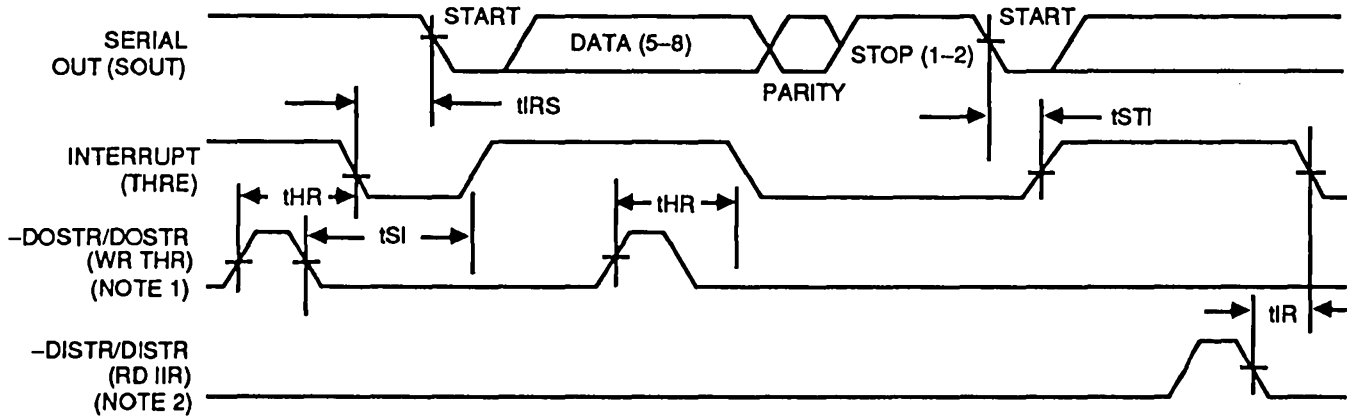




RECEIVER



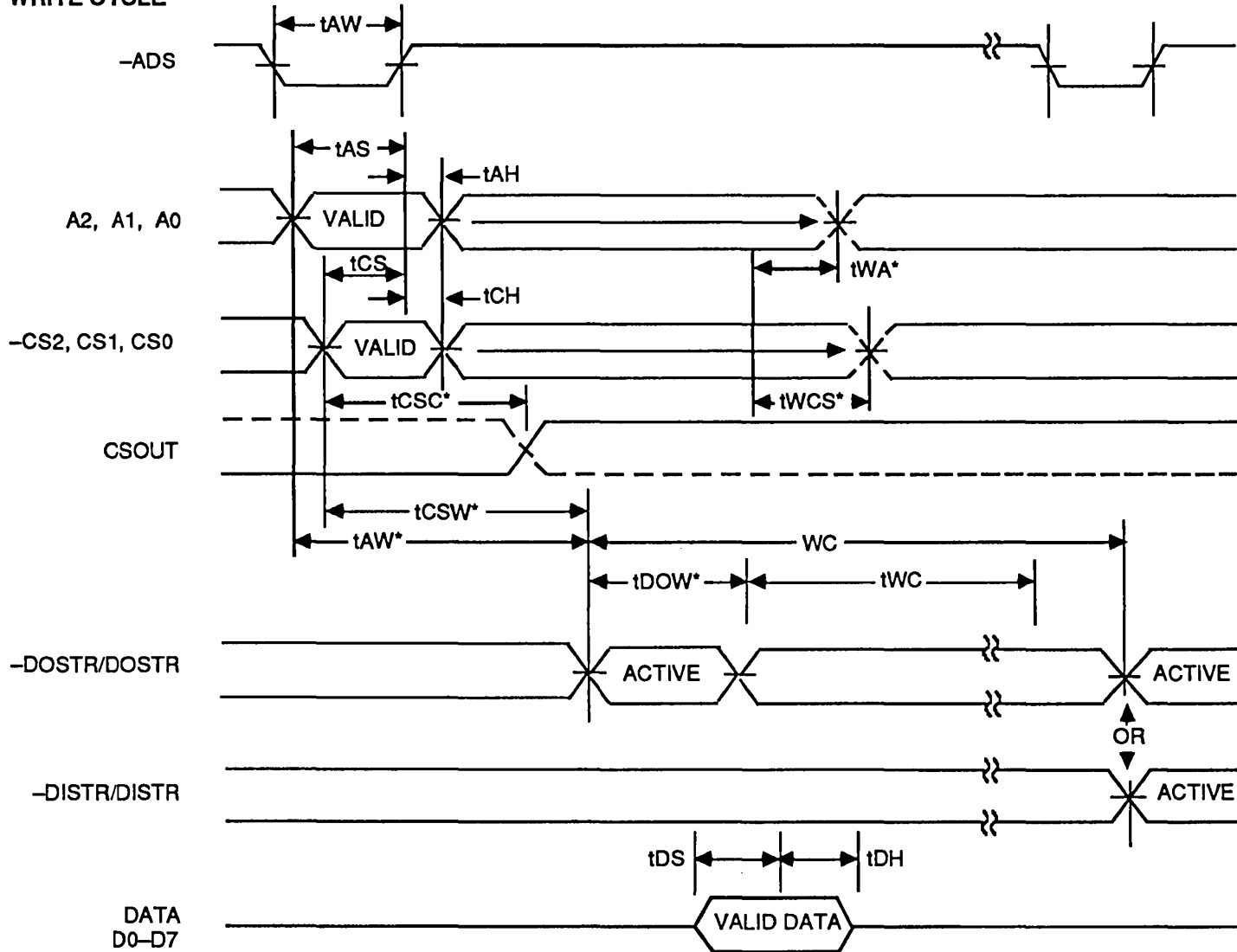
TRANSMITTER



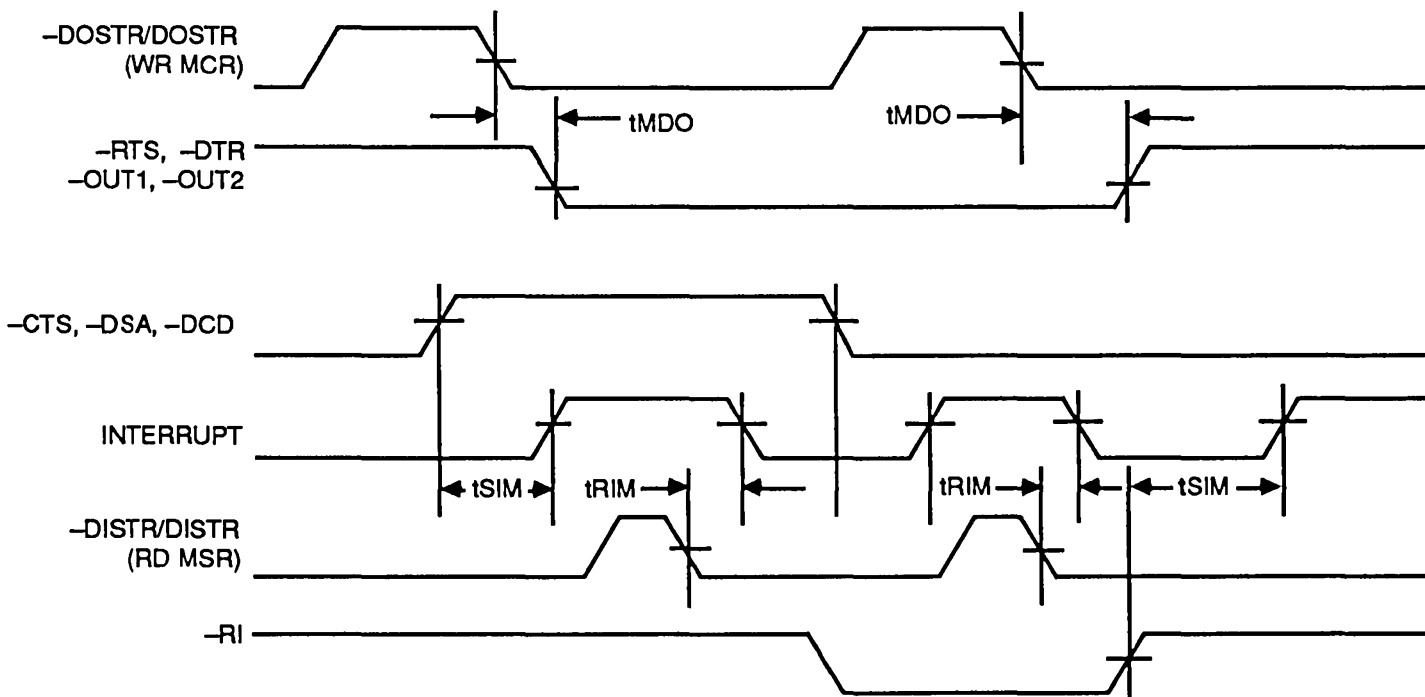
Notes: 1. See WRITE Timing Diagram.
2. See READ Timing Diagram.



WRITE CYCLE



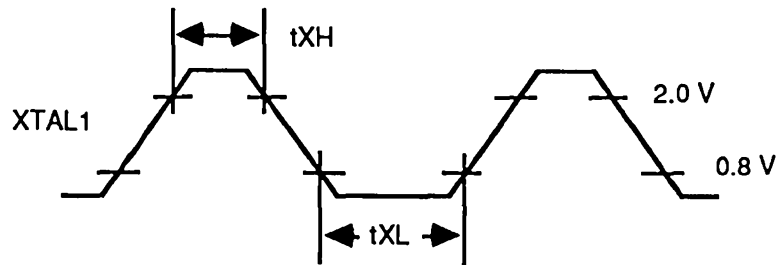
MODEM CONTROLS



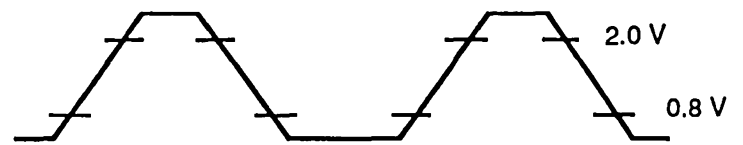


AC TESTING INPUT/OUTPUT WAVEFORMS

EXTERNAL CLOCK INPUT (3.1 MHz MAXIMUM)

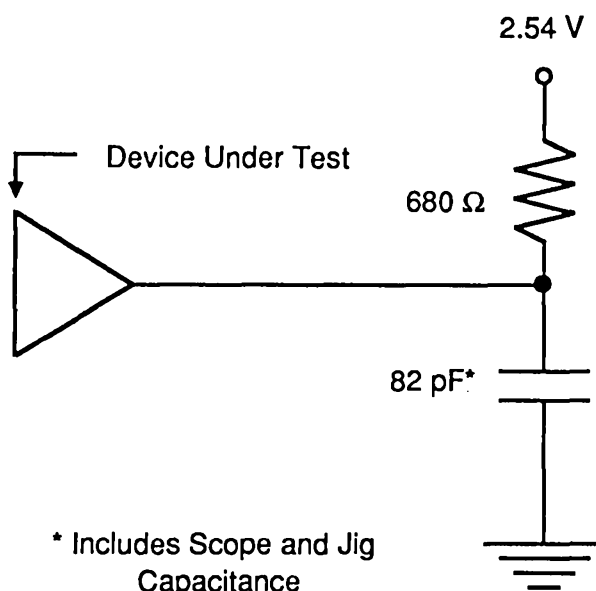


AC TEST POINTS



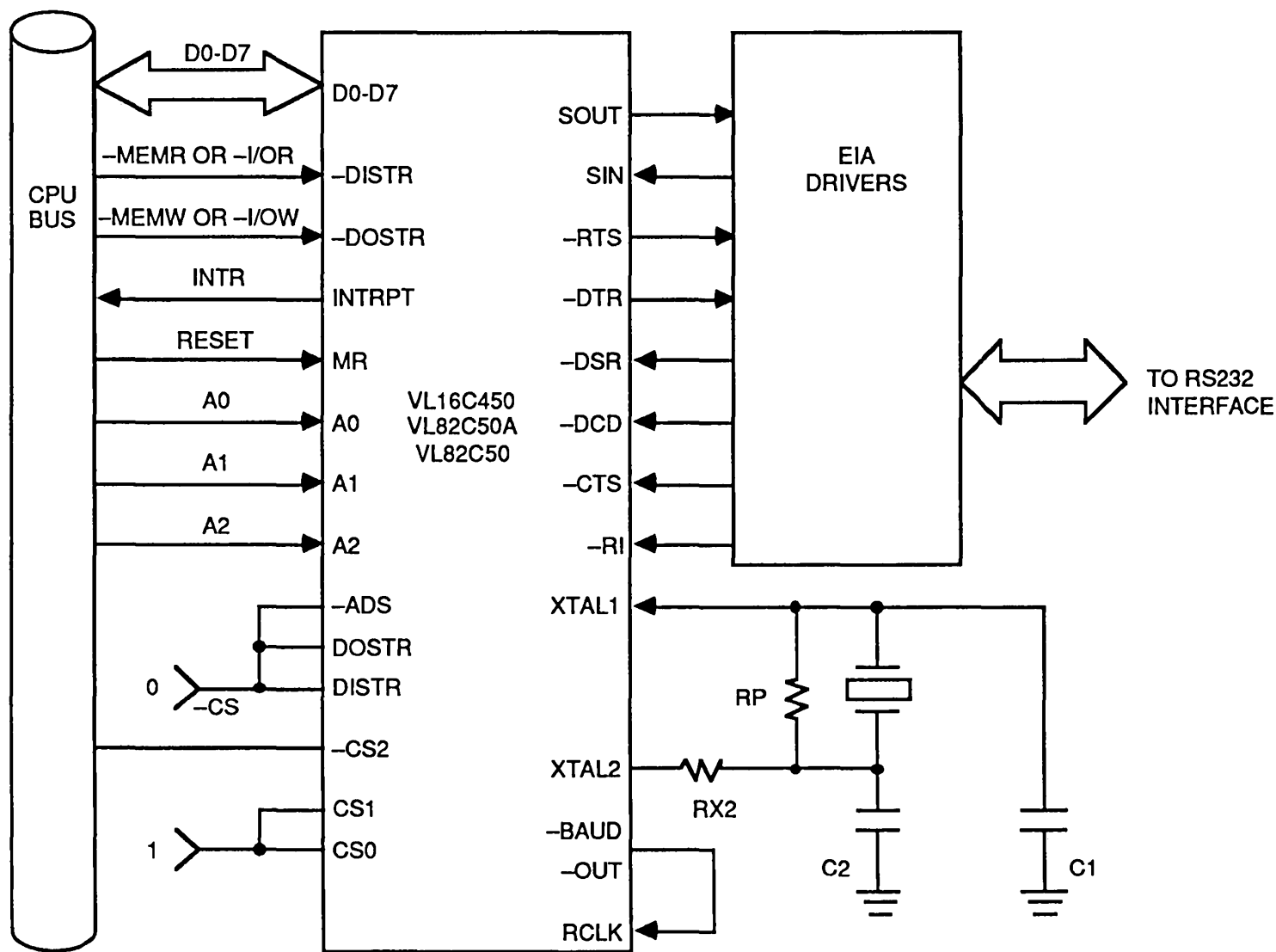
Note: All timings are referenced to valid 0 and valid 1.

TEST CIRCUIT



BASIC CONFIGURATION

VL16C450, VL82C50A, VL82C50



TYPICAL COMPONENT VALUES

Crystal	RP	RX2	C1	C2
3.072 MHz	1 MΩ	1.5 KΩ	10 - 30 pF	40 - 90 pF

ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	–10°C to + 70°C
Storage Temperature	–65°C to + 150°C
Supply Voltage to Ground Potential	–0.5 V to VCC + 0.3 V
Applied Output Voltage	–0.5 V to VCC + 0.3 V
Applied Input Voltage	–0.5 V to + 7.0 V
Power Dissipation	500 mW

Stresses above those listed may cause permanent damage to the device. These are stress ratings only, functional operation of this device at these or any other conditions above those indicated in

this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS: TA = 0° to +70°C, VCC = 5 V ± 5%

Symbol	Parameter	VL16C450		VL82C50A		VL82C50		Units	Conditions
		Min	Max	Min	Max	Min	Max		
VILX	Clock Input Low Voltage	–0.5	0.8	–0.5	0.8	–0.5	0.8	V	
VIHX	Clock Input High Voltage	2.0	VCC	2.0	VCC	2.0	VCC	V	
VIL	Input Low Voltage	–0.5	0.8	–0.5	0.8	–0.5	0.8	V	
VIH	Input High Voltage	2.0	VCC	2.0	VCC	2.0	VCC	V	
VOL	Output Low Voltage		0.4		0.4		0.4	V	IOL 1.6 mA on All
VOH	Output High Voltage	2.4		2.4		2.4		V	IOH = –1.0 mA
ICC (Ave)	Average Power Supply Current (VCC)		10		10		10	mA	VCC = 5.25 V, No Loads on SIN, –DSR, –RLSD, –CTS, –DCD. –RI = 2.0 V. All Other Inputs = 0.8 V. Baud Rate Generator at 4MHz. Baud Rate at 56K.
IIL	Input Leakage		±10		±10		±10	µA	VCC = 5.25 V VSS = 0 V All Other Pins Floating
ICL	Clock Leakage		±10		±10		±10	µA	VIN = 0 V, 5.25 V
IOZ	Three-State Leakage		±20		±20		±20	µA	VCC = 5.25 V VSS = 0 V VOUT = 0 V, 5.25 V 1) Chip Deselected 2) Chip and Write Mode selected
VILMR	MR Schmitt VIL		0.8		0.8		0.8	V	
VIHMR	MR Schmitt VIH	2.0		2.0		2.0		V	

Note: –INIT, –AFD, –STB, and –SLIN are collector output pins that each have an internal pull-up resistor (2.5K Ω - 3.5K Ω) to VCC. This will generate a maximum of 2.0 mA of internal IOL. In addition to this internal current, each pin will sink at least 10 mA, while maintaining the VOL specification of 0.4 V Max.



PARALLEL/ASYNCHRONOUS COMMUNICATIONS ELEMENT

FEATURES

- IBM PC/AT-compatible
- VL16C450 with on-board Centronics printer interface
- Completely pin- and upward-compatible with the dual serial channel VL16C452
- Independent control of transmit, receive, line status and data set interrupts
- Individual modem control signals
- Programmable serial interface characteristics:
 - 5-, 6-, 7- or 8-bit characters
 - Even-, odd- or no-parity bit generation and detection
 - 1, 1 1/2 or 2 stop bit generation
- Three-state TTL drive for the data and control bus

DESCRIPTION

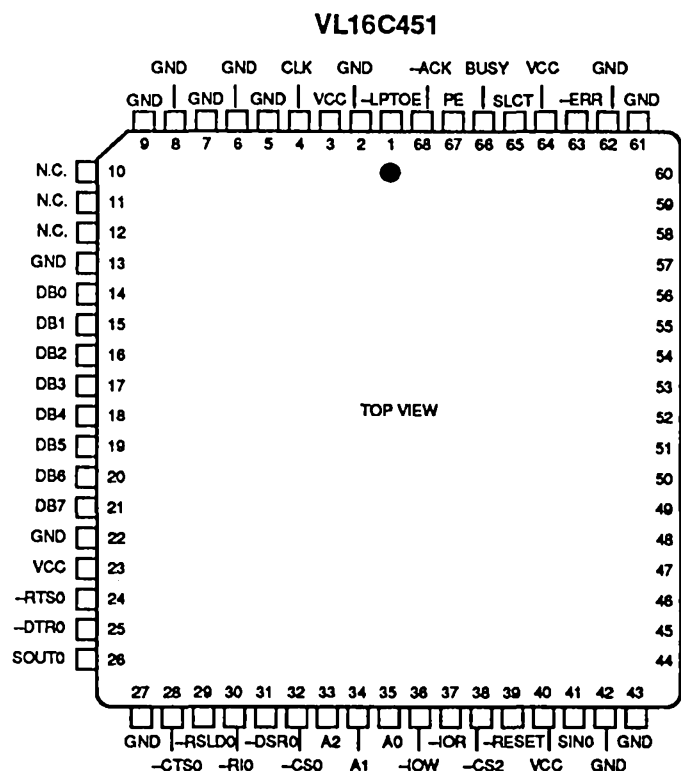
The VL16C451 is an enhanced version of the popular VL16C450 asynchronous communications element (ACE). The serial channel performs serial-to-parallel conversion on data characters received from peripheral devices or modems, and parallel-to-serial conversion on data characters transmitted by the CPU. The complete status of the Parallel/Asynchronous Communications Element (P/ACE) can be read at any time during functional operation by the CPU. The information obtained includes the type and condition of the transfer operations being performed, and error conditions. It is fully pin- and upward-compatible with the dual serial channel VL16C452. The second serial channel of the VL16C452 occupies pins that are VCC, GND, or N.C. (not connected) on the VL16C451.

The VL16C451 also provides the user with a fully bidirectional parallel data port that fully supports the parallel Centronics type printer. This port allows information received from either serial communication port to be printed from the P/ACE. The parallel port, together with the serial port, provide IBM PC/AT-compatible computers with a single device to serve the two system ports.

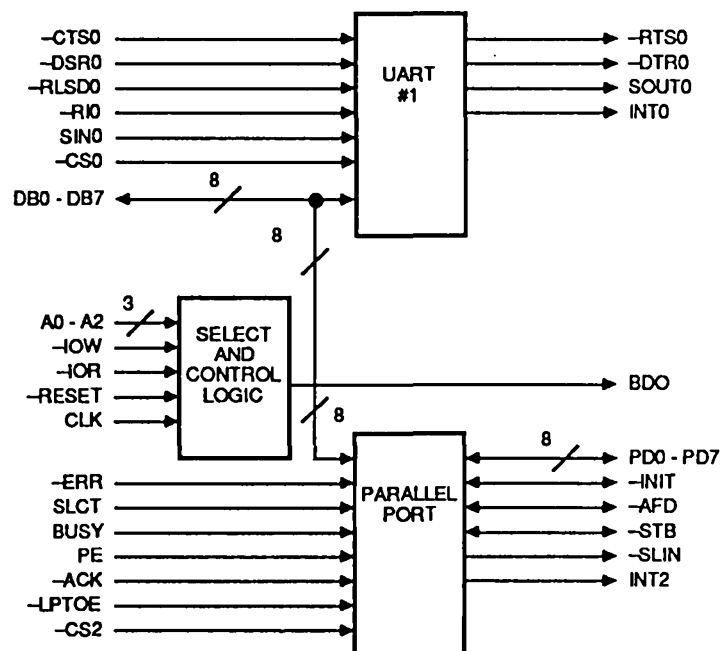
A programmable baud rate generator is included that can divide the timing reference clock input by a divisor between 1 and $(2^{16} - 1)$.

The VL16C451 is housed in a 68-pin plastic leaded chip carrier.

PIN DIAGRAM



BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Maximum Clock Frequency	Package
VL16C451-QC	3.1 MHz	Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range is 0°C to +70°C.

SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Description
-IOR	37	Input/Output Read Strobe - This is an active low input which causes the serial channel to output data to the data bus (DB0-DB7). The data output depends upon the register selected by the address inputs A0, A1, A2. Chip Select 0 (-CS0) selects the UART and Chip Select 2 (-CS2) selects the line printer port.
-IOW	36	Input/Output Write Strobe - This is an active low input which causes data from the data bus (DB0-DB7) to be input to the UART or to the parallel port. The data input depends upon the register selected by the address inputs A0, A1, A2. The chip select inputs (-CS0 and -CS2) enable the UART and the parallel port (respectively).
DB0-DB7	14-21	Data Bits DB0-DB7 - The Data Bus provides eight, three-state I/O lines for the transfer of data, control and status information between the VL16C451 and the CPU. These lines are normally in a high-impedance state except during read operations. D0 is the least significant bit (LSB) and is the first serial data bit to be received or transmitted.
A0, A1, A2	35, 34, 33	Address Lines A0-A2 - The address lines select the internal registers during CPU bus operations. See Table 1 for the decode of the serial channels, Table 11 for the decode of the parallel line printer port.
CLK	4	Clock Input - The external clock input to the UART baud rate divisor
SOUT0,	26	Serial Data Output - This line is the serial data output from the UART's transmitter circuitry. A mark (1) is a logic "one" (high) and space (0) is a logic "zero" (low). SOUT0 is held in the mark condition when the transmitter is disabled, Reset is true, the Transmitter Register is empty, or when in the Loop Mode.
-CTS0	28	Clear to Send Input - The logical state of the -CTS pin is reflected in the CTS bit of the (MSR) Modem Status Register [CTS is bit 4 of the MSR, written MSR(4)] of the UART. A change of state of the -CTS pin, since the previous reading of the MSR causes the setting of DCTS [MSR(0)] of the Modem Status Register. When the -CTS pin is low, the modem is indicating that data on SOUT0 can be transmitted.
DSR0	31	Data Set Ready Input - The logical state of the DSR0 pin is reflected in MSR(5) of the Modem Status Register. DDSR [MSR(1)] indicates whether the DSR0 pin has changed state since the previous reading of the MSR. When the DSR0 pin is low, the modem is indicating that it is ready to exchange data with the UART.
DTR0	25	Data Terminal Ready Output - The DTR0 pin can be set (low) by writing a logic 1 to MCR(0), Modem Control Register bit 0 of the UART. This signal is cleared (high) by writing a logic 0 to the DTR bit [MCR(0)] or whenever a reset occurs. When active (low), the DTR0 pin indicates to the DCE that the UART is ready to receive data.
-RTS0	24	Request to Send Output - The -RTS0 signal is an output on the UART used to enable the modem. The -RTS0 pin is set low by writing a logic 1 to MCR(1) bit 1 of the UART's Modem Control Register. The -RTS0 pin is reset high by Reset. A low on the -RTS0 pin indicates to the DCE that the UART has data ready to transmit. In half duplex operations, -RTS0 is used to control the direction of the line.
-RI0	30	Ring Indicator Input - When low, -RI0 indicates that a telephone ringing signal has been received by the modem or data set. The -RI0 signal is a modem control input whose condition is tested by reading MSR(6) (RI) of the UART. The Modem Status Register output TERI [MSR(2)] indicates whether the RI input has changed from high to low since the previous reading of the MSR. If the interrupt is enabled [IER(3)=1] and -RI0 changes from a high to low, an interrupt is generated.
-LPTOE	1	Parallel Data Output Enable - When low, this signal enables the Write Data Register to the PD0 - PD7 lines. A high puts the PD0 - PD7 lines in the high-impedance state allowing them to be used as inputs. -LPTOE is usually tied low for line printer operation.
SIN0	41	Serial Data Input - The serial data input moves information from the communication line or modem to the VL16C451 receiver circuits. A mark (1) is high, and a space (0) is low. Data on serial data inputs is disabled when operating in the loop mode.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Description
-RLSD0,	29	Receive Line Signal Detect - When low, the -RLSD output indicates that the data carrier has been detected by the modem or data set. -RLSD is a modem input whose condition can be tested by the CPU by reading MSR(7) (RLSD) of the Modem Status Register. MSR(3) (DRLSD) of the Modem Status Register indicates whether the -RLSD input has changed since the previous reading of the MSR. -RLSD has no effect on the receiver. If the -RLSD changes state with the modem status interrupt enabled, an interrupt occurs.
-RESET	39	Reset - When low, the reset input forces the VL16C451 into an idle mode in which all serial data activities are suspended. The Modem Control Register (MCR) along with its output is cleared. The Line Status Register (LSR) is cleared except for the THRE and TEMT bits, which are set. All functions of the device remain in an idle state until programmed to resume serial data activities.
INT0	45	Serial Channel Interrupt Output - This three-state output is enabled by the MCR bit 2. The serial channel interrupt goes active (high) when one of the following interrupts has an active (high) condition and is enabled by the Interrupt Enable Register of the serial channel: Receiver Error flag, Received Data Available, Transmitter Holding Register Empty, and Modem Status. The interrupt is reset low upon appropriate service or a reset.
-CS0, -CS2	32, 38	Chip Selects - Each Chip Select input acts as an enable for the write and read signals for its channel. -CS0 enables the serial port, while -CS2 enables the signals to the line printer port.
BDO	44	Bus Buffer Output - This active high output is asserted when this serial channel or the parallel port is read. This output can be used to control the system bus driver device (74LS245).
PD0-PD7	53-46	Parallel Data Bits (0-7) - These eight lines provide a byte-wide input or output port to the system. The eight lines are held in a high-impedance state when -LPTOE is held in the high state.
-STB	55	Line Printer Strobe - This open-drain line provides communication between the VL16C451 and the line printer. When it is active low, it provides the line printer with a signal to latch the data currently on the parallel port.
-AFD	56	Line Printer Autofeed - This open-drain line provides the line printer with an active low signal when continuous form paper is to be autofed to the printer.
-INIT	57	Line Printer Initialize: This open-drain line provides the line printer with a signal that allows the line printer initialization routine to be started.
-SLIN	58	Line Printer Select: This open-drain line selects the printer when it is active low.
INT2	59	Printer Port Interrupt - This signal is an active high, three-state output, generated by the positive transition of -ACK. It is enabled by bit 4 of the Write Control Register.
-ERROR	63	Line Printer Error - This is an input line from the line printer. The line printer reports an error by holding this line low during the error condition.
SLCT	65	Line Printer Selected - This is an input line from the line printer that goes high when the line printer has been selected.
BUSY	66	Line Printer Busy - This is an input line from the line printer that goes high when the line printer is not ready to accept data.
PE	67	Line Printer Paper Empty - This is an input line from the line printer that goes high when the printer runs out of paper.
-ACK	68	Line Printer Acknowledge - This input goes low to indicate a successful data transfer has taken place. It generates a printer port interrupt during its positive transition.
VCC	3, 23, 40, 64	Power Supply - The power supply requirement is 5 V \pm 5%.
GND	2, 5-9, 13, 22, 27, 42, 43, 54, 61, 62	Ground (0 V) - All pins must be tied to ground for proper operation.

FUNCTIONAL DESCRIPTION:

SERIAL CHANNEL REGISTERS

Three types of internal registers are used in the serial channel of the VL16C451. They are used in the operation of the device, and are the control, status, and data registers. The control registers are the Bit Rate Select Register DLL (Divisor Latch LSB) and DLM (Divisor Latch MSB), Line Control Register, Interrupt Enable Register, and the Modem Control registers, while the status registers are the Line Status Registers and the Modem Status Register. The data registers are the Receiver Buffer Register and the Transmitter Holding Register. The Address, Read, and Write inputs are used in conjunction with the Divisor Latch Access Bit in the Line Control Register [LCR(7)] to select the register to be written or read (see Table 1). Individual bits within these registers are referred to by the register mnemonic and the bit number in parenthesis. An example, LCR(7) refers to Line Control Register Bit 7.

The Transmitter Buffer Register and Receiver Buffer Register are data registers holding from five to eight bits of data. If less than eight data bits are transmitted, data is right justified to the

LSB. Bit 0 of a data word is always the first serial data bit received and transmitted. The VL16C451 data registers are double-buffered so that read and write operations can be performed at the same time the UART is performing the parallel-to-serial and serial-to-parallel conversion.

The format of the data character is controlled by the Line Control Register. The contents of the LCR may be read, eliminating the need for separate storage of the line characteristics in system memory. The contents of the LCR are described below:

- LCR (0) Word Length Select Bit 0 (WLS0)
- LCR (1) Word Length Select Bit 1 (WLS1)
- LCR (2) Stop Bit Select (STB)
- LCR (3) Parity Enable (PEN)
- LCR (4) Even Parity Select (EPS)
- LCR (5) Stick Parity
- LCR (6) Set Break
- LCR (7) Divisor Latch Access Bit (DLAB)

LCR (0) and LCR(1) word length select bit 1: The number of bits in each serial character is programmed as shown in the following chart:

LCR(1)	LCR(0)	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

LCR(2) Stop Bit Select: LCR(2) specifies the number of stop bits in each transmitted character. If LCR(2) is a logic 0, one stop bit is generated in the transmitted data. If LCR(2) is a logic 1 when a 5-bit word length is selected, 1.5 stop bits are generated. If LCR(2) is a logic 1 when either a 6-, 7-, or 8-bit word length is selected, two stop bits are generated. The receiver checks for two stop bits if programmed.

LCR(3) Parity Enable: When LCR(3) is high, a parity bit between the last data word bit and stop bit is generated and checked.

LCR(4) Even Parity Select: When parity is enabled [LCR(3)=1], LCR(4)=0 selects odd parity, and LCR(4)=1 selects even parity.

LCR(5) Stick Parity: When parity is enabled [LCR(3)=1], LCR(5)=1 causes the transmission and reception of a parity bit to be in the opposite state from that indicated by LCR(4). This allows the user to force parity to a known state and for the receiver to check the parity bit in a known state.

LCR(6) Break Control: When LCR(6) is set to a logic "1", the serial output (SOUT) is forced to the spacing (logic 0) state. The break is disabled by setting LCR(6) to a logic "0". The Break Control bit acts only on SOUT and has no effect on the transmitter logic. Break Control enables the CPU to alert a terminal in a computer communications system. If the following sequence is used, no erroneous or extraneous characters will be transmitted because of the break.

1. Load an all "0"s pad character in response to THRE.
2. Set break in response to the next THRE.
3. Wait for the transmitter to be idle (TEMT=1), and clear break when normal transmission has to be restored.

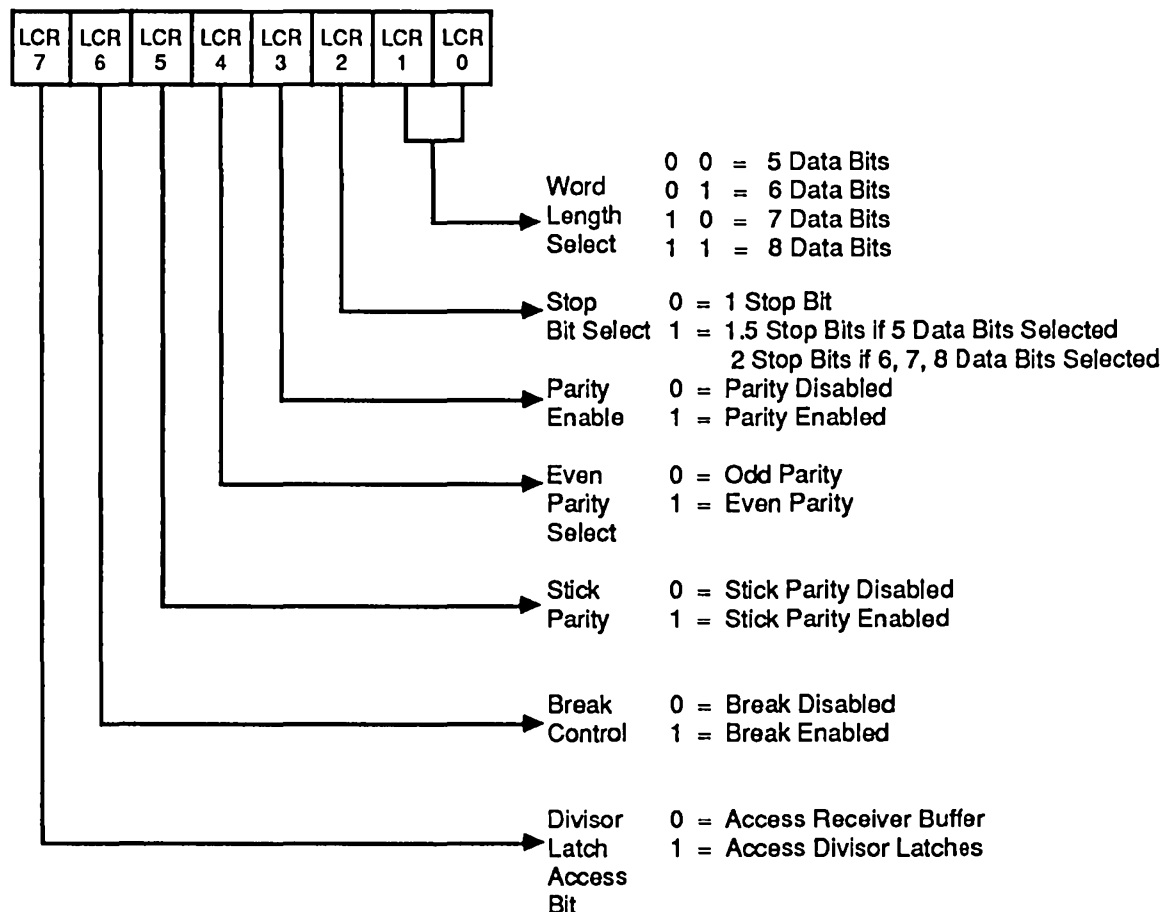
TABLE 1. SERIAL CHANNEL INTERNAL REGISTERS

DLAB	A2	A1	A0	Mnemonic	Register
0	0	0	0	RBR	Receiver Buffer Register (read only)
0	0	0	0	THR	Transmitter Holding Register (write only)
0	0	0	1	IER	Interrupt Enable Register
X	0	1	0	IIR	Interrupt Identification Register (read only)
X	0	1	1	LCR	Line Control Register
X	1	0	0	MCR	Modem Control Register
X	1	0	1	LSR	Line Status Register
X	1	1	0	MSR	Modem Status Register
X	1	1	1	SCR	Scratch Register
1	0	0	0	DLL	Divisor Latch (LSB)
1	0	0	1	DLM	Divisor Latch (MSB)

X = "Don't Care" 0 = Logic Low 1 = Logic High

Note: The serial channel is accessed when -CS0 is low.

FIGURE 1. LINE CONTROL REGISTER



LCR(7) Divisor Latch Access Bit (DLAB): LCR(7) must be set high (logic "1") to access the Divisor Latches DLL and DLM of the Baud Rate Generator during a read or write operation. LCR(7) must be input low to access the Receiver Buffer, the Transmitter Holding, or the Interrupt Enable Registers.

The Line Status Register (LSR) is a single register that provides status indications. The LSR is usually the first register read by the CPU to determine the cause of an interrupt or to poll the status the serial channel of the VL16C451.

Three error flags OE, FE, and PE provide the status of any error conditions detected in the receiver circuitry. During reception of the stop bits, the error flags are set high by an error condition. The error flags are not reset by the absence of an error condition in the next received character. The flags reflect the last character only if no overrun occurred. The Overrun Error

character in the Receiver Buffer Register has been overwritten by a character from the Receiver Shift Register before being read by the CPU. The character is thereby lost. Framing Error (FE) indicates that the last character received contained incorrect (low) stop bits. This is caused by the absence of the required stop bit or by a stop bit too short to be detected. Parity Error (PE) indicates that the last character received had a parity error based on the programmed and calculated parity of the received character.

The Break Interrupt (BI) status bit indicates that the last character received was a break character. A break character is an invalid data character. However, it is an entire character, including parity and stop bits.

The Transmitter Holding Register Empty (THRE) bit indicates that the THR register is empty and may receive another character. The Transmission Shift Register Empty (TEMT) bit

indicates that the Transmitter Shift Register is empty, and the serial channel has completed transmission of the last character to be sent. If the interrupt is enabled [IER(1)], an active THRE causes an interrupt (INTRPT).

The Data Ready (DR) bit indicates that the RBR has been loaded with a received character (including Break) and that the CPU may access this data.

Reading the LSR clears LSR(1)-LSR(4). (OE, PE, FE, and BI.)

The contents of the Line Status Register shown in Table 2 are described below:

LSR(0) Data Ready (DR): Data Ready is set high when an incoming character has been received and transferred into the Receiver Buffer Register. LSR(0) is reset low by a CPU read of the data in the Receiver Buffer Register.

LSR(1) Overrun Error (OE): Overrun Error indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was

TABLE 2. LINE STATUS REGISTER BITS

LSR BITS	Logic 1	Logic 0
LSR (0) Data Ready (DR)	Ready	Not Ready
LSR (1) Overrun Error (OE)	Error	No Error
LSR (2) Parity Error (PE)	Error	No Error
LSR (3) Framing Error (FE)	Error	No Error
LSR (4) Break Interrupt (BI)	Break	No Break
LSR (5) Transmitter Holding Register Empty (THRE)	Empty	Not Empty
LSR (6) Transmitter Empty (TEMT)	Empty	Not Empty
LSR (7) Not Used		

transferred into the Receiver Buffer Register, overwriting the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.

LSR(2) Parity Error (PE): Parity Error indicates that the received data character does not have the correct even or odd parity, as selected by the Even Parity Select bit (LCR(4)). The PE bit is set high upon detection of a parity error, and is reset low when the CPU reads the contents of the LSR.

LSR(3) Framing Error (FE): Framing Error indicates that the received character did not have a valid stop bit. LSR(3) is set high when the stop bit following the last data bit or parity bit is detected as a zero bit (spacing level). The FE indicator is reset low when the CPU reads the contents of the LSR.

LSR(4) Break Interrupt (BI): Break Interrupt is set high when the received data input is held in the spacing (logic 0) state for longer than a full word transmission time (start bit + data bits + parity + stop bits). The BI indicator is reset when the CPU reads the contents of the Line Status Register.

LSR(1) - LSR(4) are the error conditions that produce a Receiver Line Status interrupt (priority 1 interrupt in the Interrupt Identification Register (IIR)) when any of the conditions are detected. This interrupt is enabled by setting IER(2)=1 in the Interrupt Enable Register.

LSR(5) Transmitter Holding Register Empty (THRE): THRE indicates that the VL82C50A is ready to accept a new character for transmission. The THRE

bit is set high when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. LSR(5) is reset low by the loading of the Transmitter Holding Register by the CPU. LSR(5) is not reset by a CPU read of the LSR.

When the THRE interrupt is enabled (IER(1)=1). THRE causes a priority 3 interrupt in the IIR. If THRE is the interrupt source indicated in IIR, INTRPT is cleared by a read of the IIR.

LSR(6) Transmitter Empty (TEMT): TEMT is set high when the Transmitter Holding Register (THR) and the Transmitter Shift Register (TSR) are both empty. LSR(6) is reset low when a character is loaded into the THR and remains low until the character is transferred out of SOUT. TEMT is not reset low by a CPU read of the LSR.

LSR(7): This bit is always 0.

The Modem Control Register (MCR) controls the interface with the modem or data set as described in Table 3.

MCR can be written and read. The -RTS and -DTR outputs are directly controlled by their control bits in this register. A high input asserts a low (true) at the output pins. MCR Bits 0, 1, 3, and 4 are shown below:

MCR(0): When MCR(0) is set high, the -DTR output is forced low. When MCR(0) is reset low, the -DTR output is forced high. The -DTR output of the serial channel may be input into an inverting line driver in order to obtain the proper polarity input at the modem or data set.

MCR(1): When MCR(1) is set high, the RTS output is forced low. When MCR(1) is reset low, the -RTS output is forced high. The -RTS output of the serial channel may be input into an inverting line driver in order to obtain the proper polarity input at the modem or data set.

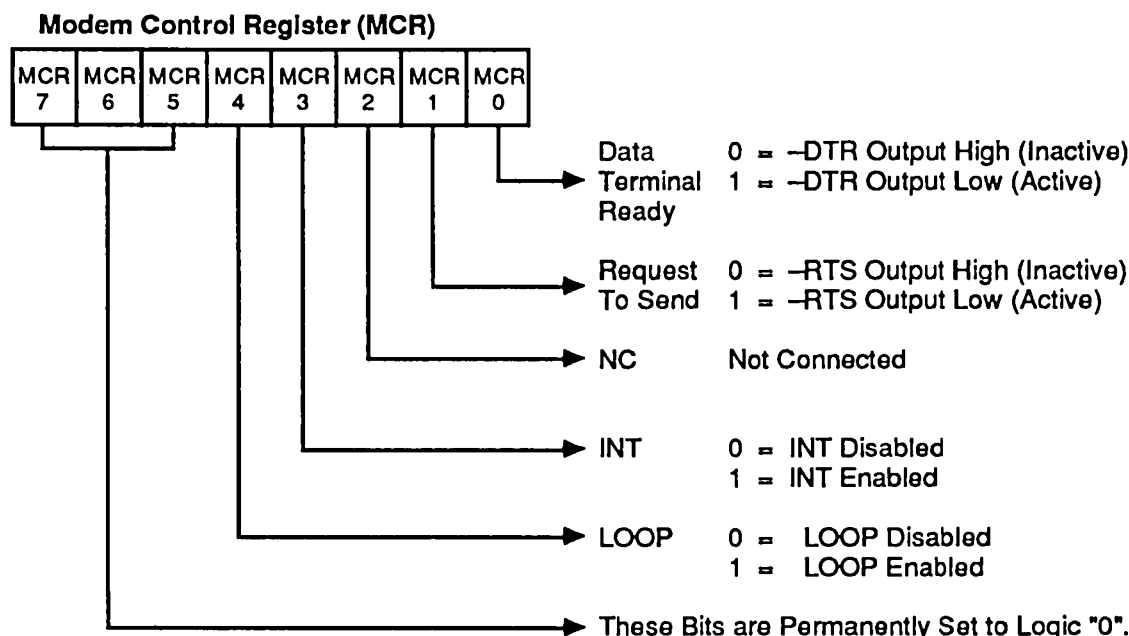
MCR(3): When MCR(3) is set high, the INT output is enabled.

MCR(4): MCR(4) provides a local loopback feature for diagnostic testing of the channel. When MCR(4) is set high, Serial Output (SOUT) is set to the marking (logic "1") state, and the receiver data input Serial Input (SIN) is disconnected. The output of the Transmitter Shift Register is looped back into the Receiver Shift Register input. The three modem control inputs (-CTS, -DSR, and -RI) are disconnected. The modem control outputs (-DTR and -RTS) are internally connected to the four modem control inputs. The modem control output pins are forced to their inactive state (high).

TABLE 3. MODEM CONTROL REGISTER BITS

MCR BITS	Logic 1	Logic 0
MCR (0) DataTerminal Ready (DTR)	-DTR Output Low	-DTR Output High
MCR (1) Request to Send (RTS)	-RTS Output Low	-RTS OutputHigh
MCR (2) 0		
MCR (3) Interrupt (INT) Enable	INT Enabled	INT Disabled
MCR (4) LOOP	Loop Enabled	Loop Disabled
MCR (5) 0		
MCR (6) 0		
MCS (7) 0		

FIGURE 2. MODEM CONTROL REGISTER



In the diagnostic mode, data transmitted is immediately received. This allows the processor to verify the transmit and receive data paths of the selected serial channel. Bits MCR(5) - MCR(7) are permanently set to logic 0.

The MSR provides the CPU with status of the modem input lines from the modem or peripheral devices. The MSR allows the CPU to read the serial channel modem signal inputs by accessing the data bus interface of the VL16C451. In addition to the current status information, four bits of the MSR indicate whether the modem inputs have changed since the last reading of the MSR. The delta status bits are set high when a control input from the modem changes state, and reset low when the CPU reads the MSR.

The modem input lines for the channel are -CTS, -DSR, -RI, and -RLSD. MSR(4) - MSR(7) are status indications of these lines. The status indications follow the status of the input lines. If the modem status interrupt in the Interrupt Enable Register is enabled [IER(3)], a change of state in a modem input signals will be reflected by the modem status bits in the IIR register, and an interrupt (INTRPT) is generated. The MSR is a priority 4 interrupt. The contents of the Modem Status Register are described in Table 4. Note that the state (high or low) of the status bits are

inverted versions of the actual input pins.

MSR(0) Delta Clear to Send (DCTS): DCTS indicates that the -CTS input to the serial channel has changed state since the last time it was read by the CPU.

MSR(1) Delta Data Set Ready (DDSR): DDSR indicates that the -DSR input to the serial channel has changed state since the last time it was read by the CPU.

MSR(2) Trailing Edge of Ring Indicator (TERI): TERI indicates that the -RI input to the serial channel has changed state from high to low since the last time it was read by the CPU. Low to high transitions on -RI do not activate TERI.

MSR(3) Delta Data Carrier Detect (DRSLD): DRSLD indicates that the

-RSLD input to the serial channel has changed state since the last time it was read by the CPU.

MSR(4) Clear to Send (CTS): Clear to Send (CTS) is the status of the -CTS input from the modem indicating to the serial channel that the modem is ready to receive data from the serial channel's transmitter output (SOUT). If the serial channel is in loop mode [MSR(4)=1], MSR(4) is equivalent to -RTS in the MCR.

MSR(5) Data Set Ready (DSR): Data Set Ready (DSR) is a status of the -DSR input from the modem to the serial channel which indicates that the modem is ready to provide received data to the serial channel receiver circuitry. If the channel is in the loop mode [MCR(4)=1], MSR(5) is equivalent to the DTR in the MCR.

TABLE 4. MODEM STATUS REGISTER BITS

MSR Bit	Mnemonic	Description
MSR (1)	DDSR	Delta Data Set Ready
MSR (2)	TERI	Trailing Edge of Ring Indicator
MSR (0)	DCTS	Delta Clear to Send
MSR (3)	DRSLD	Delta Data Carrier Detect
MSR (4)	-CTS	Clear To Send
MSR (5)	-DSR	Data Set Ready
MSR (6)	-RI	Ring Indicator
MSR (7)	-RLSD	Receiver Line Signal Detect



MSR(6) Ring Indicator: Indicates the status of the RI input (pin 39). If the channel is in the loop mode [MCR(4)=1], MSR(6) is not connected in the MCR.

MSR(7) Receive Line Signal Detect : Receive Line Signal Detect indicates the status of the Receive Line Signal Detect (–RLSD) input. If the channel is in the loop mode [MCR(4)=1], MSR(4) is equivalent to OUT2 of the MCR.

The modem status inputs (–RI, –RLSD, –DSR, and –CTS) reflect the modem input lines with any change of status. Reading the MSR register will clear the delta modem status indications but has no effect on the status bits. The status bits reflect the state of the input pins regardless of the mask control signals. If a DCTS, DDSR, TERI, or DRLSD are true, and a state change occurs during a read operation (–IOR), the state change is not indicated in the MSR. If DCTS, DDSR, TERI, or DRLSD are false, and a state change occurs during a read operation, the state change is indicated after the read operation.

For LSR and MSR, the setting of status bits is inhibited during status register read –IOR operations. If a status condition is generated during a read –IOR operation, the status bit is not set until the trailing edge of the read –IOR.

If a status bit is set during a read –IOR operation, and the same status condition occurs, that status bit will be cleared at the trailing edge of the read –IOR instead of being set again.

The VL16C451 serial channel contains a programmable Baud Rate Generator (BRG) that divides the clock (DC to 3.1 MHz) by any divisor from 1 to 2^{16-1} (see also BRG description). The output frequency of the Baud Generator is 16X the data rate [divisor # = clock ÷ (baud rate × 16)]. Two 8-bit divisor latch registers store the divisor in a 16-bit binary format. These Divisor Latch registers must be loaded during initialization. Upon loading either of the Divisor latches, a 16-bit baud counter is immediately loaded. This prevents long counts on initial load.

The receiver circuitry in the serial channel of the VL16C451 is programmable for 5, 6, 7, or 8 data bits per

character. For words of less than 8 bits, the data is right justified to the least significant bit LSB = Data Bit 0 [RBR(0)]. Data Bit 0 of a data word [RBR(0)] is the first data bit received. The unused bits in a character less than 8 bits are output low to the parallel output by the serial channel.

Received data at the SIN input pin is shifted into the Receiver Shift Register by the 16X clock provided at the RCLK input. This clock is synchronized to the incoming data based on the position of the start bit. When a complete character is shifted into the Receiver Shift Register, the assembled data bits are parallel loaded into the Receiver Buffer Register. The DR flag in the LSR register is set.

Double buffering of the received data permits continuous reception of data without losing received data. While the Receiver Shift Register is shifting a new character into the serial channel, the Receiver Buffer Register is holding a previously received character for the CPU to read. Failure to read the data in the RBR before complete reception of the next character result in the loss of the data in the Receiver Register. The OE flag in the LSR register indicates the overrun condition.

RBR Bits 0 thru 7:

RBR(0)	Data Bit 0
RBR(1)	Data Bit 1
RBR(2)	Data Bit 2
RBR(3)	Data Bit 3
RBR(4)	Data Bit 4
RBR(5)	Data Bit 5
RBR(6)	Data Bit 6
RBR(7)	Data Bit 7

The Transmitter Holding Register (THR) holds parallel data from the data bus (D0-D7) until the Transmitter Shift Register is empty and ready to accept a new character for transmission. The transmitter and receiver word length and number of stop bits are the same. If the character is less than eight bits, unused bits at the microprocessor data bus are ignored by the transmitter.

Data Bit 0 [THR(0)] is the first serial data bit transmitted. The THRE flag [LSR(5)] reflect the status of the THR. The TEMT flag [LSR(5)] indicates if both the THR and TSR are empty.

THR Bits 0 thru 7

THR(0)	Data Bit 0
THR(1)	Data Bit 1
THR(2)	Data Bit 2
THR(3)	Data Bit 3
THR(4)	Data Bit 4
THR(5)	Data Bit 5
THR(6)	Data Bit 6
THR(7)	Data Bit 7

Scratchpad Register is an 8-bit Read/Write register that has no effect on either channel in the VL16C451. It is intended to be used by the programmer to hold data temporarily.

SCR Bits 0 thru 7

SCR(0)	Data Bit 0
SCR(1)	Data Bit 1
SCR(2)	Data Bit 2
SCR(3)	Data Bit 3
SCR(4)	Data Bit 4
SCR(5)	Data Bit 5
SCR(6)	Data Bit 6
SCR(7)	Data Bit 7

INTERRUPTS

The Interrupt Identification Register (IIR) in the serial channel of the VL16C451 has interrupt capability for interfacing to current microprocessors. In order to minimize software overhead during data character transfers, the serial channel prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows:

1. Receiver Line Status (priority 1)
2. Received Data Ready (priority 2)
3. Transmitter Holding Register Empty (priority 3)
4. Modem Status (priority 4)

Information indicating that a prioritized interrupt is pending and the type of interrupt is stored in the Interrupt Identification Register (IIR). When addressed during chip select time, the IIR indicates the highest priority interrupt pending. No other interrupts are acknowledged until the interrupt is serviced by the CPU. The logic equivalent of the interrupt control circuit is shown in Figure 3. The contents of the IIR are indicated in Table 5 and are described below.

IIR(0): IIR(0) can be used in either a hard-wired prioritized or polled environment to indicate whether an interrupt is pending. When IIR(0) is low, an interrupt is pending, and IIR contents

TABLE 5. INTERRUPT IDENTIFICATION REGISTER

INTERRUPT IDENTIFICATION				INTERRUPT SET AND RESET FUNCTIONS		
Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Flag	Interrupt Source	Interrupt Reset Control
X	X	1		None	None	
1	1	0	First	Receiver Line Status	OE, PE FE, or BI	LSR Read
1	0	0	Second	Received Data Available	Received Data Available	RBR Read
0	1	0	Third	THRE	THRE	IIR Read if THRE is the Interrupt Source or THR Write
0	0	0	Fourth	Modem Status	-CTS, -DSR -RI, -RSLD	MSR Read

X = Not Defined.

FIGURE 3. INTERRUPT CONTROL LOGIC

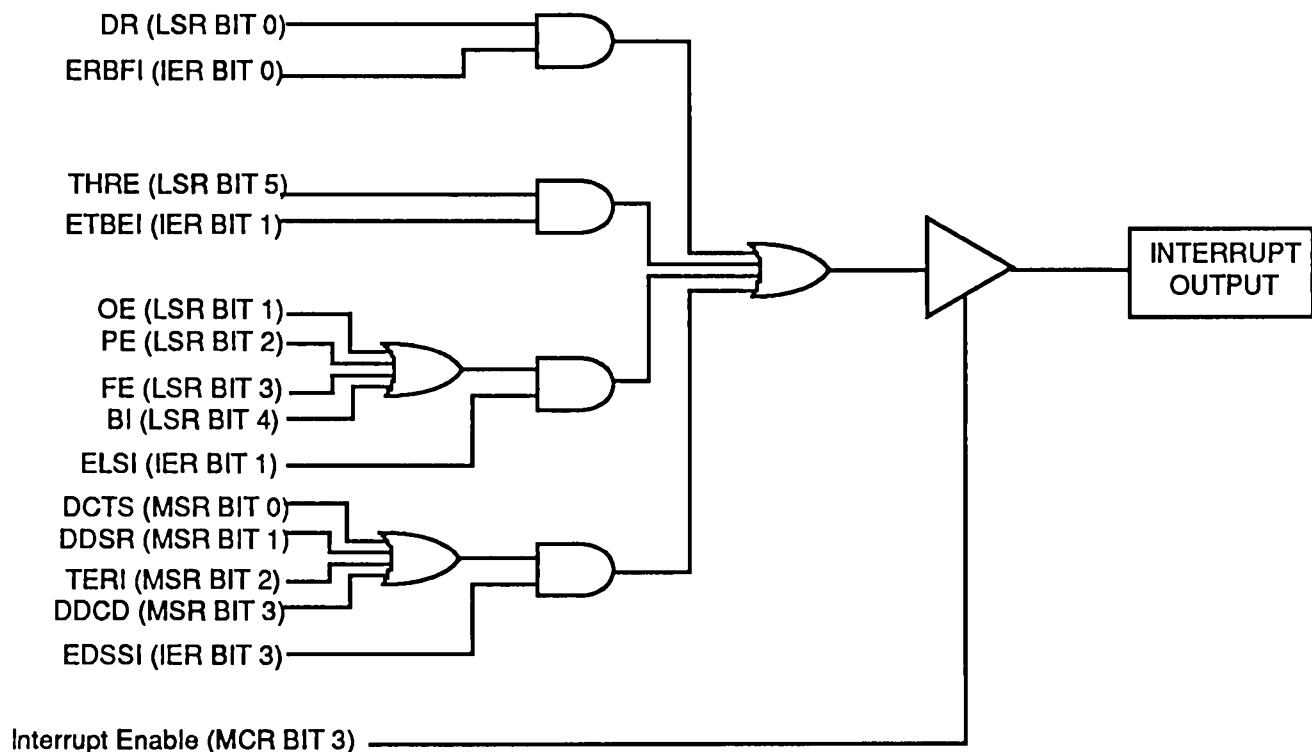


TABLE 6. SERIAL CHANNEL ACCESSIBLE REGISTERS

Register Mnemonic	Register Bit Number							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RBR (Read Only)	Data Bit 7 (MSB)	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0 (LSB)*
THR (Write Only)	Data Bit 7	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0
DLL	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DLM	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
IER	0	0	0	0	(EDSSI) Enable Modem Status Interrupt	(ELSI) Enable Receiver Line Status Interrupt	(ETBEI) Enable Transmitter Holding Register Empty Interrupt	(ERBFI) Enable Received Data Available Interrupt
IIR (Read Only)	0	0	0	0	0	Interrupt ID Bit (1)	Interrupt ID Bit (0)	"0" 1F Interrupt Pending
LCR	(DLAB) Divisor Latch Access Bit	Set Break	Stick Parity	(EPS) Even Parity Select	(PEN) Parity Enable	(STB) Number of Stop Bits	(WLSB1) Word Length Select Bit 1	(WLSB0) Word Length Select Bit 0
MCR	0	0	0	Loop	Out 2	Out 1	(RTS) Request To Send	(DTR) Data Terminal Ready
LSR	0	(TEMT) Transmitter Empty	(THRE) Transmitter Holding Register Empty	(BI) Break Interrupt	(FE) Framing Error	(PE) Parity Error	(OE) Overrun Error	(DR) Data Ready
MSR	(DCD) Data Carrier Detect	(RI) Ring Indicator	(DSR) Data Ready Set	(CTS) Clear to Send	(DRSLD) Delta Receive Line Signal Detect	(TERI) Trailing Edge Ring Indicator	(DDSR) Delta Data Set Ready	(DCTS) Delta Clear to Send
SCR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

*LSB Data Bit 0 is the first bit transmitted or received.

may be used as a pointer to the appropriate interrupt service routine. When IIR(0) is high, no interrupt is pending.

IIR(1) and IIR(2) are used to identify the highest priority interrupt pending as indicated in Table 2.

IIR(3) - IIR(7): These five bits of the IIR are logic 0.

The Interrupt Enable Register (IER) is a Write register used to independently enable the four serial channel interrupts which activate the interrupt (INTRPT) output. All interrupts are disabled by resetting IER(0) - IER(3) of the Interrupt Enable Register. Interrupts are enabled by setting the appropriate bits of the IER high. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INTRPT output. All other system functions operate in their normal manner, including the setting of the Line Status and Modem Status Registers. The contents of the Interrupt Enable Register is described in Table 3 and below:

IER(0): When programmed high [IER(0)=Logic 1], IER(0) enables Received Data Available interrupt.

IER(1): When programmed high [IER(1)=Logic 1], IER(1) enables the Transmitter Holding Register Empty interrupt.

IER(2): When programmed high [IER(2)=Logic 1], IER(2) enables the Receiver Line Status interrupt.

IER(3): When programmed high [IER(3)=Logic 1], IER(3) enables the Modem Status Interrupt.

IER(4) - IER(7): These four bits of the IER are logic 0.

TRANSMITTER

The serial transmitter section consists of a Transmitter Holding Register (THR), Transmitter Shift Register (TSR), and associated control logic. The Transmitter Holding Register Empty (THRE) and Transmitter Shift Register Empty (TEMT) are two bits in the Line Status Register which indicate the status of THR and TSR. To transmit a 5- to 8-bit word, the word is written through D0-D7 to the THR. The microprocessor should perform a write operation only if THRE is high. The THRE is set high when the word is automatically transferred from

the THR to the TSR during the transmission of the start bit.

When the transmitter is idle, THRE and TEMT are high. The first word written causes THRE to be reset to 0. After the transfer, THRE returns high. TEMT remains low for at least the duration of the transmission of the data word. If a second character is transmitted to the THR, the THRE is reset low. Since the data word cannot be transferred from the THR to the TSR until the TSR is empty, THRE remains low until the TSR has completed sending the word. When the last word has been transmitted out of the TSR, TEMT is set high. THRE is set high one THR to TSR transfer time later.

RECEIVER

Serial asynchronous data is input into the SIN pin. The idle state of the line providing the input into SIN is high. A start bit detect circuit continually searches for a high to low transition from the idle state. When the transition is detected, a counter is reset, and counts the 16X clock to 7 1/2, which is the center of the start bit. The start bit is valid if the SIN is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the SIN input.

The Line Control Register determines the number of data bits in a character (LCR(0), LCR(1)), number of stop bits LCR(2), if parity is used LCR(3), and the polarity of parity LCR(4). Status for the receiver is provided in the Line Status Register to the Receiver Buffer Register, the Data Received indication in LSR(0) is set high. The CPU reads the Receiver Buffer Register through D0-D7. This read resets LSR(0). If D0-D7 are not read prior to a new character transfer from the RSR to the RBR, the overrun error status indication is set in LSR(1). The parity check tests for even or odd parity on the parity bit, which precedes the first stop bit. If there is a parity error, the parity error is set in LSR(2). There is circuitry which tests whether the stop bit is high. If it is not, a framing error indication is generated in LSR(3).

The center of the start bit is defined as clock count 7 1/2. If the data into SIN is symmetrical square wave, the center of the data cells will occur within

$\pm 3.125\%$ of the actual center, providing an error margin of 46.875%. The start bit can begin as much as one 16X clock cycle prior to being detected.

BAUD RATE GENERATOR (BRG)

The BRG generates the clocking for the UART function, providing standard ANSI/CCITT bit rates. The oscillator driving the BRG is provided by an external clock into CLK.

The data rate is determined by the Divisor Latch registers DLL and DLM and the external frequency. The bit rate is selected by programming the two divisor latches, Divisor Latch Most Significant Byte and Divisor Latch Least Significant Byte. Setting DLL=1 and DLM=0 selects the divisor to divide by 1 (divide by 1 gives maximum baud rate for a given input frequency at the CLK input).

The BRG can use any of three different popular frequencies to provide standard baud rates. These frequencies are 1.8432 MHz, 2.4576 MHz, and 3.072 MHz. With these frequencies, standard bit rates from 50 to 38.5 kbps are available. Tables 7, 8, and 9 illustrate the divisors needed to obtain standard rates using these three crystal frequencies.

RESET

After power up, the VL16C451 -RESET input should be held low for 500 ns to reset the VL16C451 circuits to an idle mode until initialization. A low on -RESET causes the following:

1. Initializes the transmitter and receiver internal clock counters.
2. Clears the Line Status Register (LSR), except for Transmitter Shift Register Empty (TEMT) and Transmit Holding Register Empty (THRE), which are set. The Modem Control Register (MCR) is also cleared. All of the discrete lines, memory elements and miscellaneous logic associated with these register bits are also cleared or turned off. The Line Control Register (LCR), Divisor Latches, Receiver Buffer Register, Transmitter Buffer Register are not effected.

Following removal of the reset condition (Reset high), the VL16C451 remains in the idle mode until programmed.

A hardware reset of the VL16C451 sets the THRE and TEMT status bit in the LSR. When interrupts are subsequently enabled, an interrupt occurs due to THRE.

A summary of the effect of a reset on the VL16C451 is given in Table 10.

PROGRAMMING

Each serial channel of the VL16C451 is programmed by the control registers LCR, IER, DLL and DLM, and MCR. These control words define the character length, number of stop bits, parity, baud rate, and modem interface.

While the control register can be written in any order, the IER should be written to last because it controls the interrupt enables. Once the serial channel is programmed and operational, these registers can be updated any time the VL16C451 serial channel is not transmitting or receiving data.

The control signals required to access each serial channel's internal registers are shown below.

SOFTWARE RESET

A software reset of the serial channel is a useful method for returning to a

completely known state without a system reset. Such a reset consists of writing to the LCR, Divisor Latches, and MCR registers. The LSR and RBR registers should be read prior to enabling interrupts in order to clear out any residual data or status bits which may be invalid for subsequent operation.

CLOCK INPUT OPERATION

The maximum input frequency of the external clock of the VL16C451 is 3.1 MHz.

TABLE 7. BAUD RATES (1.8432 MHz CLOCK)

Desired Baud Rate	Divisor Used	Percent Error Difference Between Desired and Actual
50	2304	—
75	1536	—
110	1047	0.026
134.5	857	0.058
150	768	—
300	384	—
600	192	—
1200	96	—
1800	64	—
2000	58	0.69
2400	48	—
3600	32	—
4800	24	—
7200	16	—
9600	12	—
19200	6	—
38400	3	—
56000	2	2.86

TABLE 8. BAUD RATES (2.4576 MHz CLOCK)

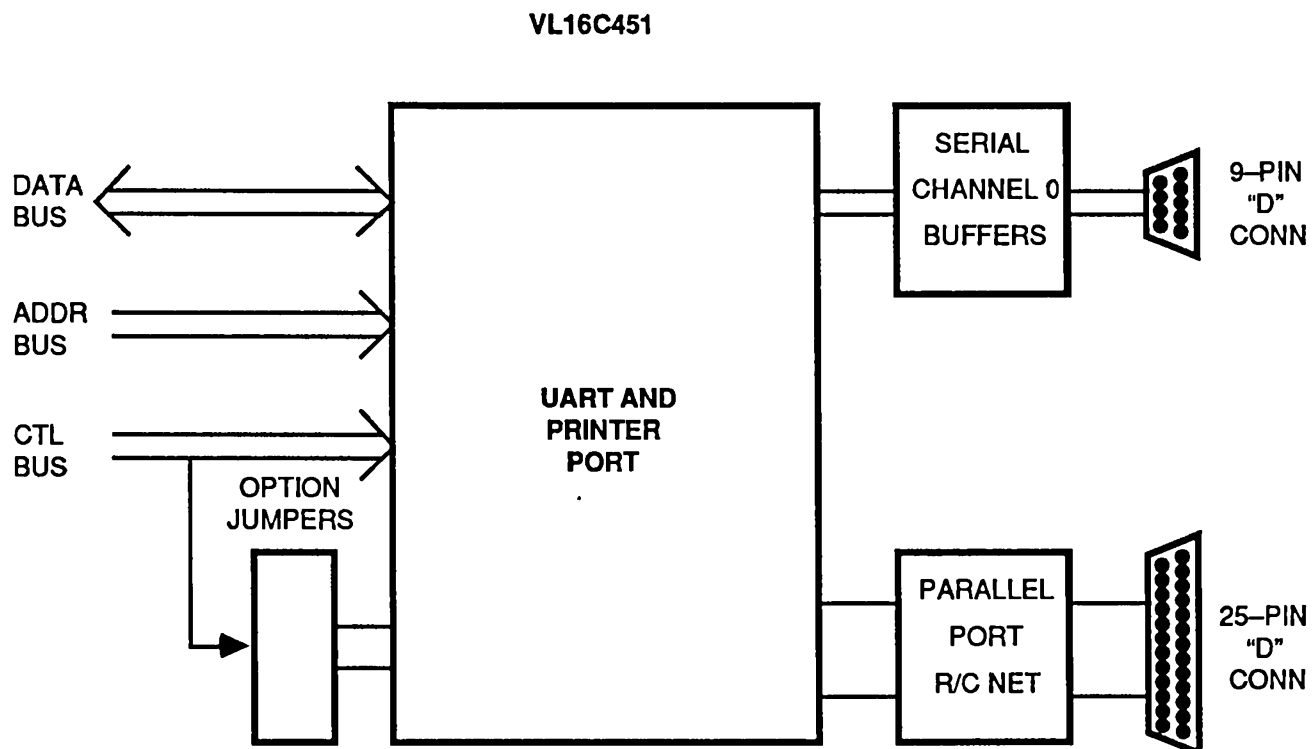
Desired Baud Rate	Divisor Used	Percent Error Difference Between Desired and Actual
50	3072	—
75	2048	—
110	1396	0.026
134.5	1142	0.0007
150	1024	—
300	512	—
600	256	—
1200	128	—
1800	85	0.392
2000	77	0.260
2400	64	—
3600	43	0.775
4800	32	—
7200	21	1.587
9600	16	—
19200	8	—
38400	4	—

TABLE 9. BAUD RATES (3.072 MHz CLOCK)

Desired Baud Rate	Divisor Used	Percent Error Difference Between Desired and Actual
50	3840	—
75	2560	—
110	1745	0.026
134.5	1428	0.034
150	1280	—
300	640	—
600	320	—
1200	160	—
1800	107	0.312
2000	96	—
2400	80	—
3600	53	0.628
4800	40	—
7200	27	1.23
9600	20	—
19200	10	—
38400	5	—

TABLE 10. RESET

Register/Signal	Reset Control	Reset
Interrupt Enable Register	Reset	All Bits Low (0–3 forced and 4–7 permanent)
Interrupt Identification Register	Reset	Bit 0 is High, Bits 1 and 2 Low
Line Control Register	Reset	Bits 3–7 are Permanently Low
MODEM Control Register	Reset	All Bits Low
Line Status Register	Reset	All Bits Low
MODEM Status Register	Reset	All Bits Low, Except Bits 5 and 6 are High
SOUT	Reset	Bits 0–3 Low
Intrpt (RCVR Errs)	Read LSR/Reset	Bits 4–7 Input Signal
Intrpt (RCVR Data Ready)	Read RBR/Reset	High
Intrpt (THRE)	Read IIR/Write THR/Reset	Low
Intrpt (Modem Status Changes)	Read MSR/Reset	Low
–Out2	Reset	Low
–RTS	Reset	High
–DTR	Reset	High
–Out1	Reset	High

DEVICE APPLICATION


FUNCTIONAL DESCRIPTION

PARALLEL PORT REGISTERS

The VL16C451's parallel port interfaces the device to a Centronics-style printer. When Chip Select 2 ($\overline{\text{CS2}}$) is low, the parallel port is selected. Table 11 shows the registers associated with this parallel port. The read or write function of the register is controlled by the state of the read ($\overline{\text{IOR}}$) and write ($\overline{\text{IOW}}$) pin as shown. The Read Data Register allows the microprocessor to read the information on the parallel bus.

The Read Status Register allows the microprocessor to read the status of the printer in the five most significant bits. The status bits are Printer Busy ($\overline{\text{BUSY}}$), Acknowledge ($\overline{\text{ACK}}$) which is a handshake function, Paper Empty (PE), Printer Selected (SLCT), and Error ($\overline{\text{ERROR}}$). The Read Control Register allows the state of the control lines to be read. The Write Control Register sets the state of the control lines.

They are Interrupt Enable (IRQ ENB), Select In (SLIN), Initialize the Printer ($\overline{\text{INIT}}$), Autofeed the Paper (AUTOFD), Strobe (STROBE), which informs the printer of the presence of a valid byte on the parallel bus. The Write Data Register allows the microprocessor to write a byte to the parallel bus.

The parallel port is completely compatible with the parallel port implementation used in the IBM Serial/Parallel Adaptor.

TABLE 11. PARALLEL PORT REGISTERS

Register	Register Bits							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read Data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Read Status	$\overline{\text{BUSY}}$	$\overline{\text{ACK}}$	PE	SLCT	$\overline{\text{ERROR}}$	1	1	1
Read Control	1	1	1	IRQ ENB	SLIN	$\overline{\text{INIT}}$	AUTOFD	STROBE
Write Data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Write Control	1	1	1	IRQ ENB	SLIN	$\overline{\text{INIT}}$	AUTOFD	STROBE

TABLE 12. PARALLEL PORT REGISTER SELECT

Control Pins					Register Selected
$\overline{\text{IOR}}$	$\overline{\text{IOW}}$	$\overline{\text{CS2}}$	A1	A0	
0	1	0	0	0	Read Data
0	1	0	0	1	Read Status
0	1	0	1	0	Read Control
0	1	0	1	1	Invalid
1	0	0	0	0	Write Data
1	0	0	0	1	Invalid
1	0	0	1	0	Write Control
1	0	0	1	1	Invalid

AC CHARACTERISTICS TA= 0°C to +70°C, VCC= 5 V ±5% (Notes 1, 5)

Symbol	Parameter	Min	Max	Units	Conditions
tDIW	–IOR Strobe Width	125		ns	
RC	Read Cycle	360		ns	
tDDD	Delay from –IOR to Data		125	ns	100 pF Load
tHZ	–IOR to Floating Data Delay	0	100	ns	100 pF Load, Note 4
tDOW	–IOW Strobe Width	100		ns	
WC	Write Cycle	360		ns	
tDS	Data Setup Time	40		ns	
tDH	Data Hold Time	40		ns	
tRA	Address Hold Time from –IOR	20		ns	Note 2
tRCS	Chip Select Hold Time from –IOR	20		ns	Note 2
tAR	–IOR Delay from Address	60		ns	Note 2
tCSR	–IOR Delay from Chip Select	50		ns	Note 2
tWA	Address Hold Time from –IOW	20		ns	Note 2
tWCS	Chip Select Hold Time from –IOW	20		ns	Note 2
tAW	–IOW Delay from Address	60		ns	Note 2
tCSW	–IOW Delay from Select	50		ns	Note 2
tRW	Reset Pulse Width	5		μs	
tXH	Duration of Clock High Pulse	140		ns	External Clock
tXL	Duration of Clock Low Pulse	140		ns	External Clock

Notes:

1. All timing specifications apply to pins on both serial channels (e.g. RI refers to both RI0 and RI1).
2. The internal address strobe is always active.
3. RCLK = tXH and tXL.
4. Charge and discharge time is determined by VOL, VOH and the external loading.
5. All timings are referenced to valid 0 and valid 1.
(see AC TEST POINTS).

AC CHARACTERISTICS (Cont.) TA= 0°C to +70°C, VCC= 5 V ±5% (Notes 1, 5)

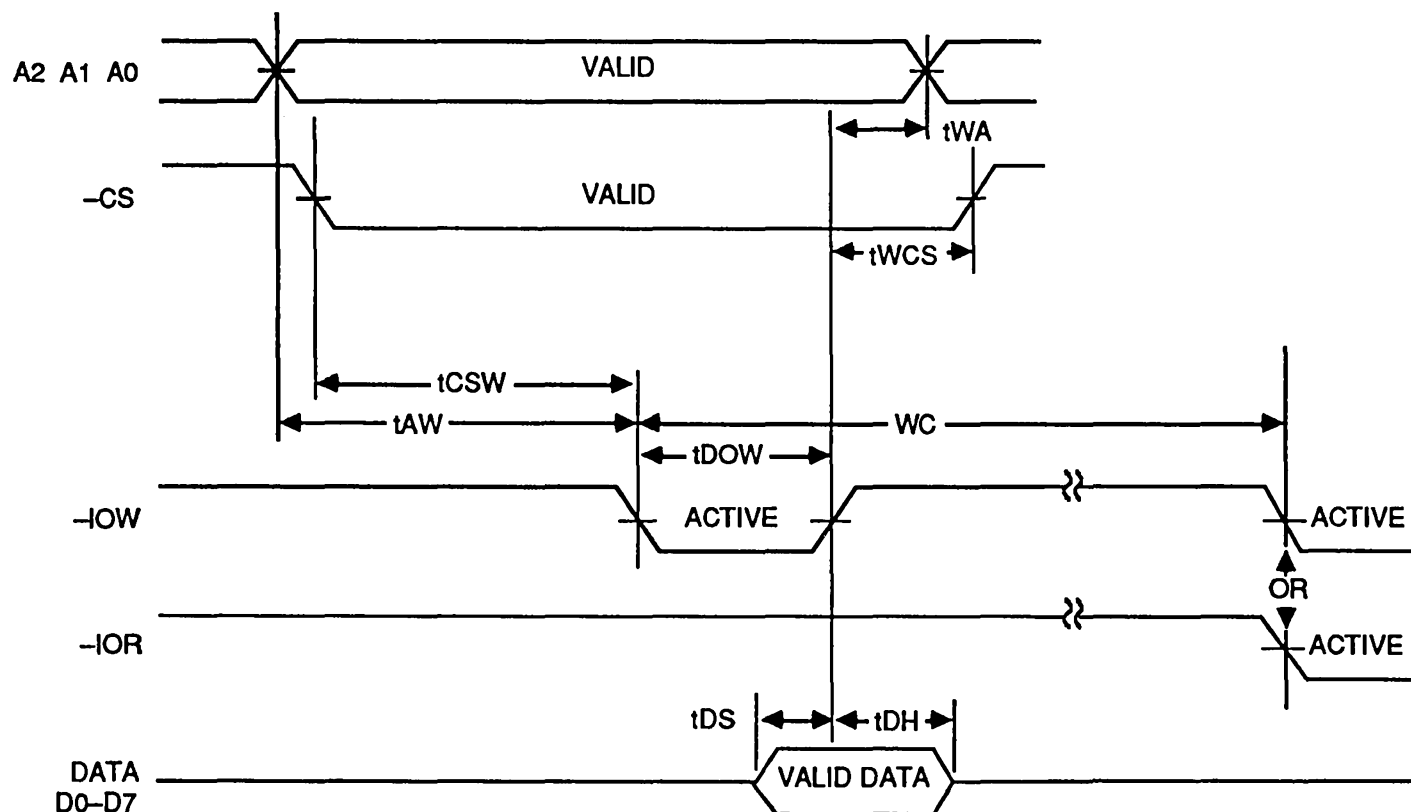
Symbol	Parameter	Min	Max	Units	Conditions
Transmitter					
tHR1	Delay from Rising Edge of $\overline{\text{IOW}}$ (WR THR) To Reset Interrupt		175	ns	100 pF Load
tIRS	Delay from Initial INTR Reset to Transmit Start		16	CLK Cycles	Note 3
tSI	Delay from Initial Write to Interrupt	8	24	CLK Cycles	Note 3
tSTI	Delay from Stop to Interrupt (THRE)		8	CLK Cycles	Note 3
tIR	Delay from $\overline{\text{IOR}}$ (RD IIR) to Reset Interrupt (THRE)		250	ns	100 pF Load
Modem Control					
tMDO	Delay from $\overline{\text{IOW}}$ (WR MCR) to Output		250	ns	100 pF Load
tSIM	Delay to Set Interrupt from MODEM Input		250	ns	100 pF Load
tRIM	Delay to Reset Interrupt from $\overline{\text{IOR}}$ (RS MSR)		250	ns	100 pF Load
Receiver					
tSINT	Delay from Stop to Set Interrupt		1	CLK Cycles	Note 3
tRINT	Delay from $\overline{\text{IOR}}$ (RD RBR/RDLSR) to Reset Interrupt		1	μs	100 pF Load
Parallel Port					
tDT	Data Time	1		μs	
tSB	Strobe Time	1	500	μs	
tAD	Acknowledge Delay (Busy Start to Acknowledge)			μs	Defined by Printer
tAKD	Acknowledge Delay (Busy End to Acknowledge)			μs	Defined by Printer
tAK	Acknowledge Duration Time			μs	Defined by Printer
tBSY	Busy Duration Time			μs	Defined by Printer
tBSD	Busy Delay Time			μs	Defined by Printer

Notes:

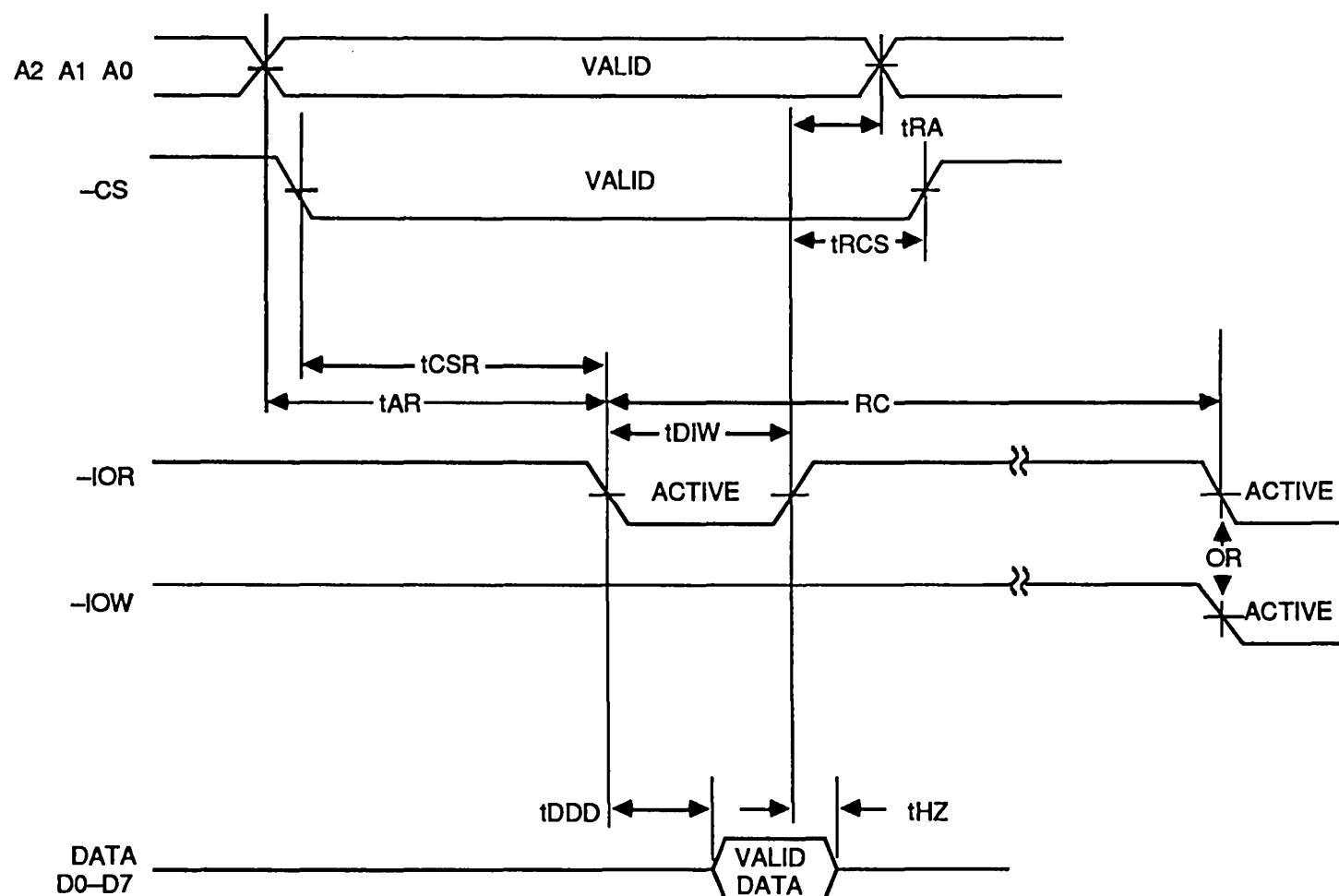
1. All timing specifications apply to pins on both serial channels (e.g. RI refers to both RI0 and RI1).
2. The internal address strobe is always active.
3. RCLK = tXH and tXL.
4. Charge and discharge time is determined by VOL, VOH and the external loading.
5. All timings are referenced to valid 0 and valid 1 (see AC TEST POINTS).



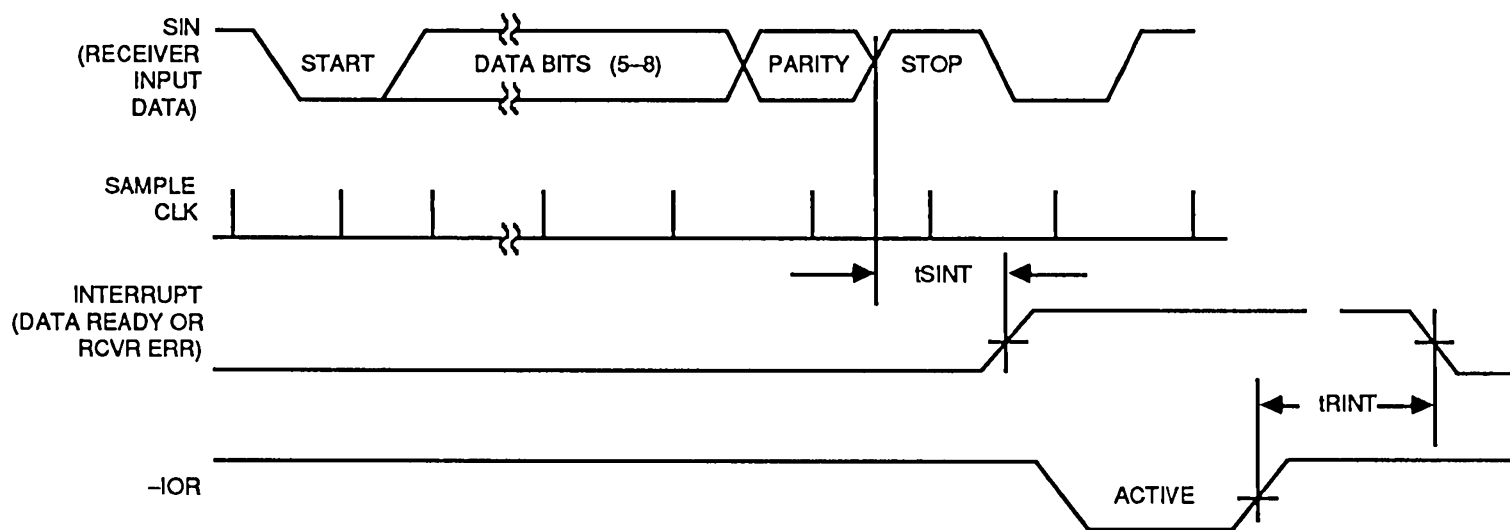
WRITE CYCLE TIMING



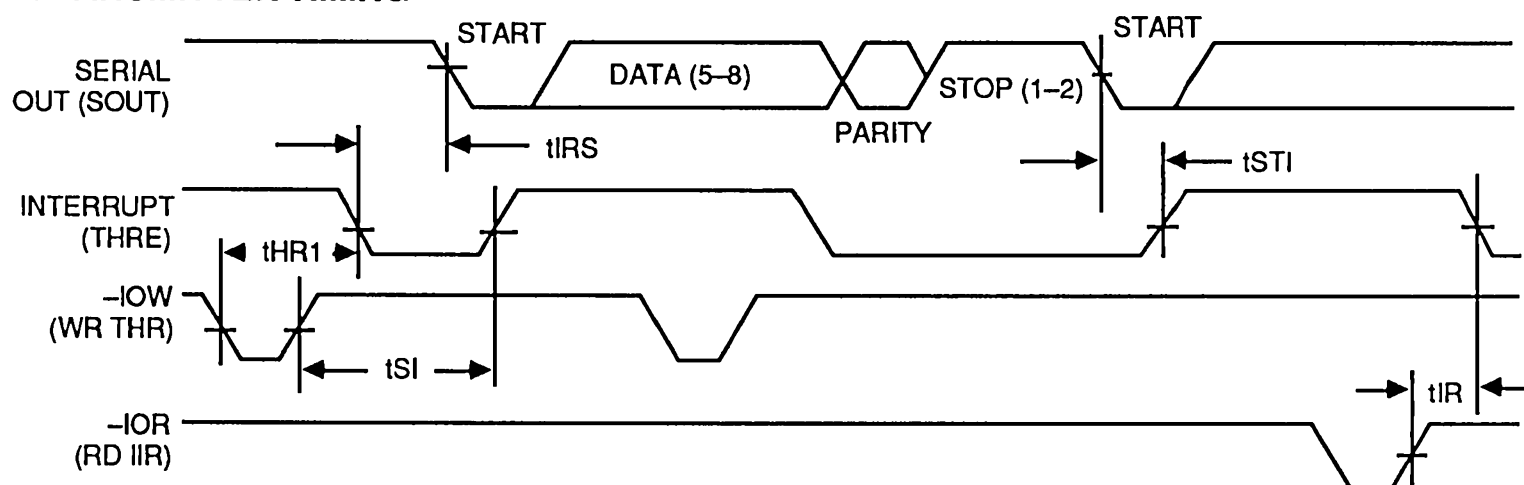
READ CYCLE TIMING



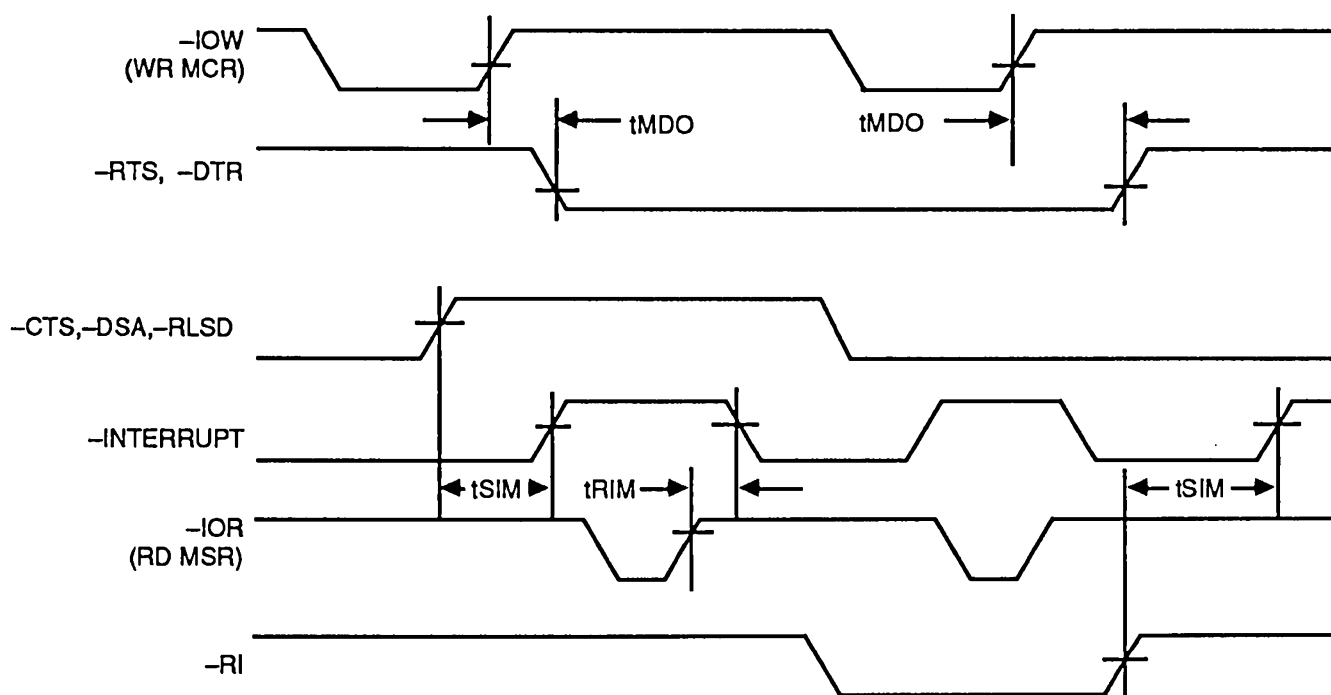
RECEIVER TIMING



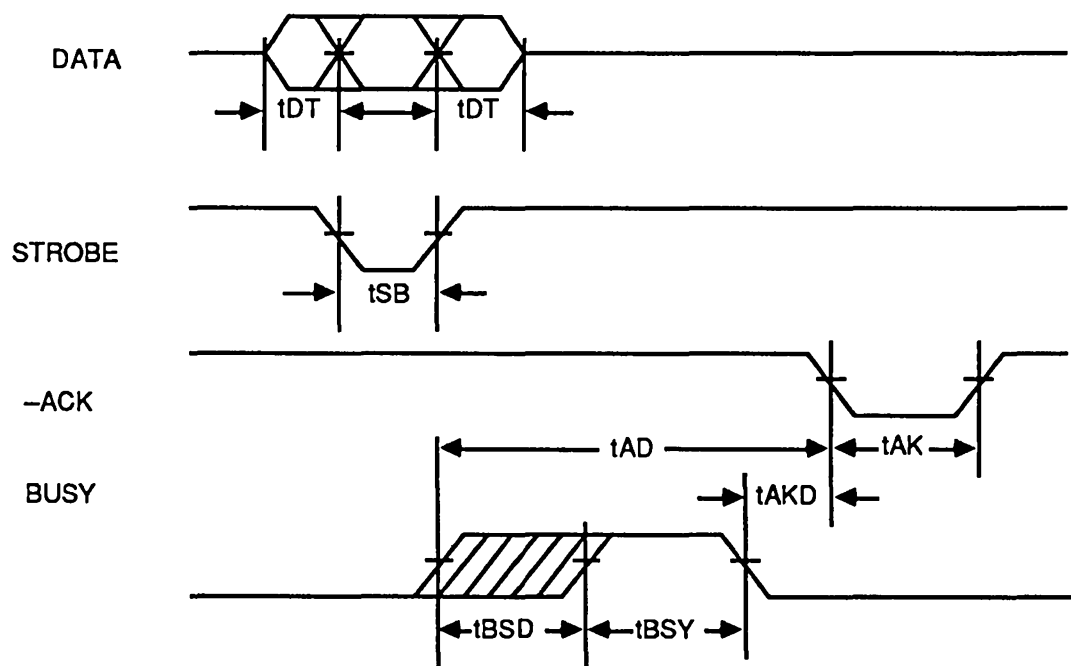
TRANSMITTER TIMING



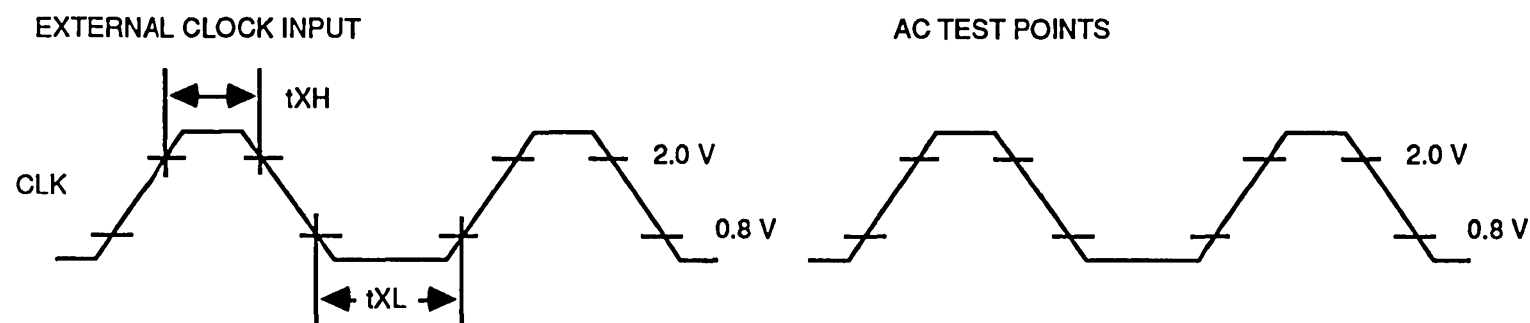
MODEM TIMING



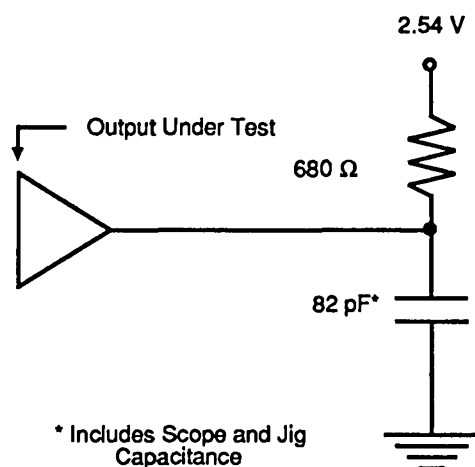
PARALLEL PORT TIMING



AC TESTING INPUT/OUTPUT WAVEFORMS



TEST CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature -10°C to $+70^{\circ}\text{C}$
 Storage Temperature -65°C to $+150^{\circ}\text{C}$
 Supply Voltage to Ground Potential -0.5 V to $\text{VCC} + 0.3\text{ V}$
 Applied Output Voltage -0.5 V to $\text{VCC} + 0.3\text{ V}$
 Applied Input Voltage -0.5 V to $+7.0\text{ V}$
 Power Dissipation 500 mW

Stresses above those listed may cause permanent damage to the device. These are stress ratings only, functional operation of this device at these or any other conditions above

those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS: $T_A = 0$ to $+70^{\circ}\text{C}$, $\text{VCC} = 5\text{ V} \pm 5\%$

Symbol	Parameter	Min	Max	Units	Conditions
VILX	Clock Input Low Voltage	-0.5	0.8	V	
VIHX	Clock Input High Voltage	2.0	VCC	V	
VIL	Input Low Voltage	-0.5	0.8	V	
VIH	Input High Voltage	2.0	VCC	V	
VOL	Output Low Voltage		0.4	V	$\text{IOL} = 4.0\text{ mA}$ on DB0 - DB7 $\text{IOL} = 12\text{ mA}$ on PD0 - PD7 $\text{IOL} = 10\text{ mA}$ on $-\text{NIT}$, $-\text{AFD}$, $-\text{STB}$, and $-\text{SLIN}$ (see Note 1) $\text{IOL} = 2.0\text{ mA}$ on all other outputs
VOH	Output High Voltage	2.4		V	$\text{IOH} = -0.4\text{ mA}$ on DB0 - DB7 $\text{IOH} = -2.0\text{ mA}$ on PD0 - PD7 $\text{IOH} = -0.2\text{ mA}$ on $-\text{INIT}$, $-\text{AFD}$, $-\text{STB}$, and $-\text{SLIN}$ $\text{IOH} = -0.2\text{ mA}$ on all other outputs
ICC	Power Supply Current		50	mA	$\text{VCC} = 5.25\text{ V}$, No loads on SINO; $-\text{DSR0}$; $-\text{RLSD0}$; $-\text{CTS0}$. $-\text{RI0} = 2.0\text{ V}$. Other inputs = 0.8 V . Baud rate generator = 4 MHz . Baud rate = 56 K
IIL	Input Leakage		± 10	μA	$\text{VCC} = 5.25\text{ V}$, $\text{GND} = 0\text{ V}$. All other pins floating.
ICL	Clock Leakage		± 10	μA	$\text{VIN} = 0\text{ V}$, 5.25 V
IOZ	3-State Leakage		± 20	μA	$\text{VCC} = 5.25\text{ V}$, $\text{GND} = 0\text{ V}$. $\text{VOUT} = 0\text{ V}$, 5.25 V 1) Chip deselected 2) Chip and write mode selected
VIL(RES)	Reset Schmitt VIL		0.8	V	
VIH(RES)	Reset Schmitt VIH	2.0		V	

Note 1. $-\text{INIT}$, $-\text{AFD}$, $-\text{STB}$, and $-\text{SLIN}$ are open collector output pins that each have an internal pull-up resistor ($2.5\text{ k}\Omega$ - $3.5\text{ k}\Omega$) to VCC. This will generate a maximum of 2.0 mA of internal IOL. In addition to this internal current, each pin will sink at least 10 mA , while maintaining the VOL specification of 0.4 V Max .

2-2

DUAL ASYNCHRONOUS COMMUNICATIONS ELEMENT

FEATURES

- IBM PC/AT-compatible
- Dual-channel version of VL16C450
- Centronix printer interface
- Independent control of transmit, receive, line status and data set interrupts on each channel
- Individual modem control signals for each channel
- Programmable serial interface characteristics for each channel:
 - 5-, 6-, 7- or 8-bit characters
 - Even-, odd- or no-parity bit generation and detection
 - 1, 1 1/2 or 2 stop bit generation
- Three-state TTL drive for the data and control bus on each channel

DESCRIPTION

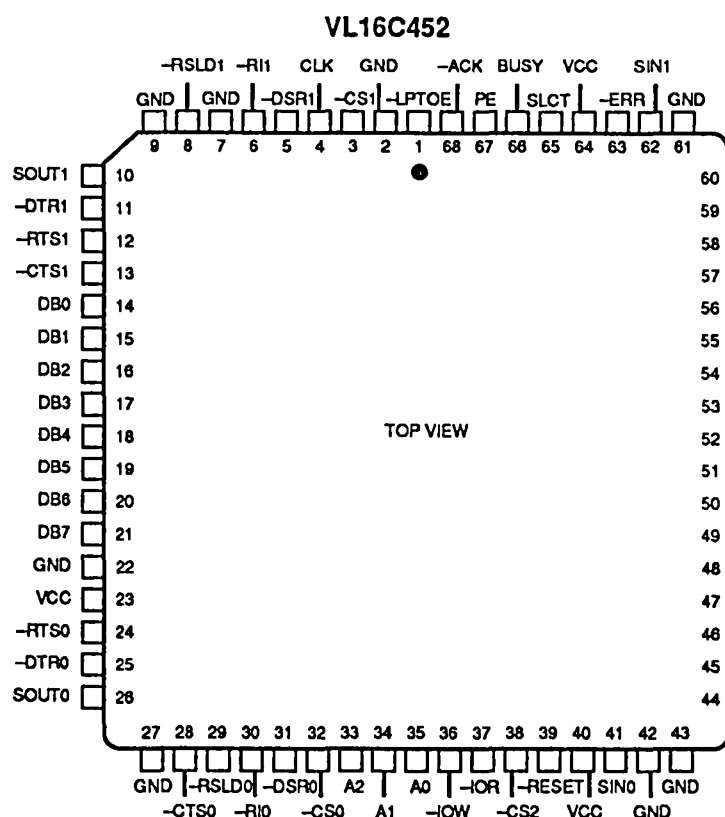
The VL16C452 is an enhanced dual-channel version of the popular VL16C450 asynchronous communications element (ACE). The device serves two serial input/output interfaces simultaneously in microcomputer- or microprocessor-based systems. Each channel performs serial-to-parallel conversion on data characters received from peripheral devices or modems, and parallel-to-serial conversion on data characters transmitted by the CPU. The complete status of each channel of the dual ACE can be read at any time during functional operation by the CPU. The information obtained includes the type and condition of the transfer operations being performed, and error conditions.

In addition to its dual communications interface capabilities, the VL16C452 provides the user with a fully bidirectional parallel data port that fully supports the parallel Centronics type printer. This port allows information received from either serial communication port to be printed from the dual ACE. The parallel port, together with the two serial ports, provide IBM PC/AT-compatible computers with a single device to serve the three system ports.

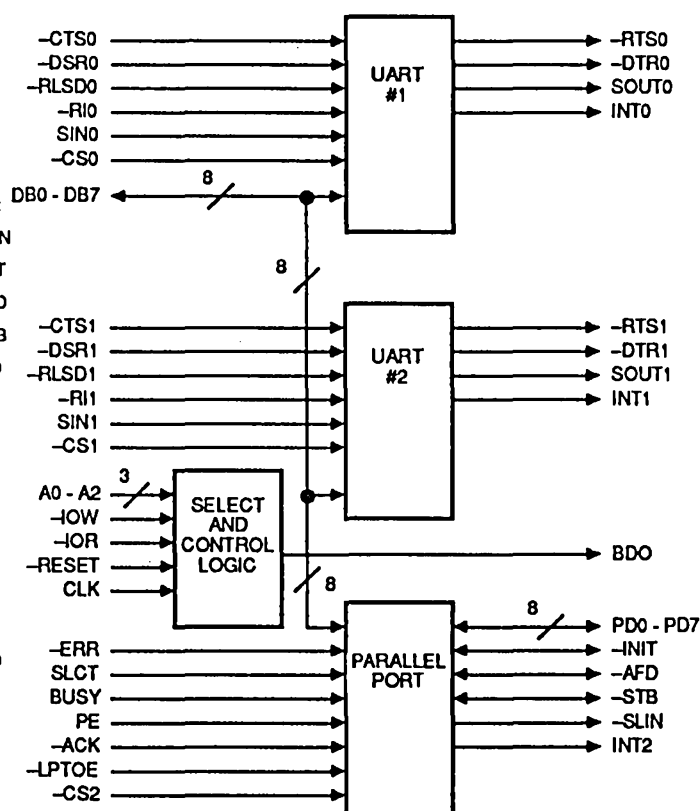
A programmable baud rate generator is included that can divide the timing reference clock input by a divisor between 1 and $(2^{16} - 1)$.

The VL16C452 is housed in a 68-terminal plastic leaded chip carrier.

PIN DIAGRAM



BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Maximum Clock Frequency	Package
VL16C452-QC	3.1 MHz	Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range is 0°C to +70°C.

SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Description
-IOR	37	Input/Output Read Strobe - This is an active low input which causes the selected channel to output data to the data bus (DB0-DB7). The data output depends upon the register selected by the address inputs A0, A1, A2. Chip Select 0 (-CS0) selects UART #1, Chip Select 1 (-CS1) selects UART #2, and Chip Select 2 (-CS2) selects the line printer port.
-IOW	36	Input/Output Write Strobe - This is an active low input which causes data from the data bus (DB0-DB7) to be input to either UART or to the parallel port. The data input depends upon the register selected by the address inputs A0, A1, A2. The chip select inputs (-CS0, -CS1, and -CS2) enable UART#1, UART #2, and the parallel port (respectively).
DB0-DB7	14-21	Data Bits DB0-DB7 - The Data Bus provides eight, three-state I/O lines for the transfer of data, control and status information between the VL16C452 and the CPU. These lines are normally in a high-impedance state except during read operations. D0 is the least significant bit (LSB) and is the first serial data bit to be received or transmitted.
A0, A1, A2	35, 34, 33	Address Lines A0-A2 - The address lines select the internal registers during CPU bus operations. See Table 1 for the decode of the serial channels, Table 11 for the decode of the parallel line printer port..
CLK	4	Clock Input: The external clock input to the baud rate divisor of each UART.
SOUT0, SOUT1	26, 10	Serial Data Outputs - These lines are the serial data outputs from the UARTs' transmitter circuitry. A mark (1) is a logic "one" (high) and space (0) is a logic "zero" (low). Each SOUT is held in the mark condition when the transmitter is disabled, Reset is true, the Transmitter Register is empty, or when in the Loop Mode.
-CTS0, -CTS1	28, 13	Clear to Send Inputs - The logical state of each -CTS pin is reflected in the CTS bit of the (MSR) Modem Status Register [CTS is bit 4 of the MSR, written MSR (4)] of each UART. A change of state in either -CTS pin since the previous reading of the associated MSR causes the setting of DCTS [MSR(0)] of each Modem Status Register. When a -CTS pin is low, the modem is indicating that data on the associated SOUT can be transmitted.
DSR0, DSR1	31, 5	Data Set Ready Inputs - The logical state of the DSR pins is reflected in MSR(5) of its associated Modem Status Register. DDSR [MSR(1)] indicates whether the associated DSR pin has changed state since the previous reading of the MSR. When a DSR pin is low, its modem is indicating that it is ready to exchange data with the associated UART.
DTR0, DTR1	25, 11	Data Terminal Ready Lines - Each DTR pin can be set (low) by writing a logic 1 to MCR(0), Modem Control Register bit 0 of its associated UART. This signal is cleared (high) by writing a logic 0 to the DTR bit [MCR(0)] or whenever a reset occurs. When active (low), the DTR pin indicates to the DCE that its UART is ready to receive data.
-RTS0, -RTS1	24, 12	Request to Send Outputs - The -RTS signal is an output on each UART used to enable the modem. An -RTS pin is set low by writing a logic 1 to MCR(1) bit 1 of its UART's Modem Control Register. Both -RTS pins are reset high by Reset. A low on the -RTS pin indicates to the DCE that its UART has data ready to transmit. In half duplex operations, -RTS is used to control the direction of the line.
-RI0, -RI1	30, 6	Ring Indicator Inputs - When low, -RI indicates that a telephone ringing signal has been received by the modem or data set. The -RI signal is a modem control input whose condition is tested by reading MSR(6) (RI) of each UART. The Modem Status Register output TERI [MSR(2)] indicates whether the RI input has changed from high to low since the previous reading of the MSR. If the interrupt is enabled [IER(3)=1] and RI changes from a high to low, an interrupt is generated.
-LPTOE	1	Parallel Data Output Enable - When low, this signal enables the Write Data Register to the PD0 - PD7 lines. A high puts the PD0 - PD7 lines in the high-impedance state allowing them to be used as inputs. -LPTOE is usually tied low for line printer operation.
VCC	23, 40, 64	Power Supply - The power supply requirement is 5 V \pm 5%.
GND	2, 7, 9, 22, 27, 42, 43, 54, 61	Ground (0 V) - All pins must be tied to ground for proper operation.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Description
-RLSD0, -RLSD1	29, 8	Receive Line Signal Detect - When low, the -RLSD output indicates that the data carrier has been detected by the modem or data set. -RLSD is a modem input whose condition can be tested by the CPU by reading MSR(7) (RLSD) of the Modem Status Registers. MSR(3) (DRLSD) of the Modem Status Register indicates whether the -RLSD input has changed since the previous reading of the MSR. -RLSD has no effect on the receiver. If the -RLSD changes state with the modem status interrupt enabled, an interrupt occurs.
-RESET	39	Reset - When low, the reset input forces the VL16C452 into an idle mode in which all serial data activities are suspended. The Modem Control Register (MCR) along with its associated outputs are cleared. The Line Status Register (LSR) is cleared except for the THRE and TMT bits, which are set. All functions of the device remain in an idle state until programmed to resume serial data activities.
INT0, INT1	45, 60	Serial Channel Interrupts - Each three-state, serial channel interrupt output (enabled by bit 3 of the MCR) goes active (high) when one of the following interrupts has an active (high) condition and is enabled by the Interrupt Enable Register of its associated channel: Receiver Error flag, Received Data Available, Transmitter Holding Register Empty, and Modem Status. The interrupt is reset low upon appropriate service or a reset operation.
SIN0, SIN1	41, 62	Serial Data Inputs - The serial data inputs move information from the communication line or modem to the VL16C452 receiver circuits. A mark (1) is high, and a space (0) is low. Data on serial data inputs is disabled when operating in the loop mode.
-CS0, -CS1, -CS2	32, 3, 38	Chip Selects - Each Chip Select input acts as an enable for the write and read signals for the serial channels 0 (-CS0) and 1 (-CS1). -CS2 enables the signals to the line printer port.
BDO	44	Bus Buffer Output - This active high output is asserted when either serial channel or the parallel port is read. This output can be used to control the system bus driver device (74LS245).
PD0-PD7	53-46	Parallel Data Bits (0-7) - These eight lines provide a byte-wide input or output port to the system. The eight lines are held in a high-impedance state when -LPTOE is held in the high state.
-STB	55	Line Printer Strobe - This open-drain line provides communication between the VL16C452 and the line printer. When it is active low, it provides the line printer with a signal to latch the data currently on the parallel port.
-AFD	56	Line Printer Autofeed - This open-drain line provides the line printer with an active low signal when continuous form paper is to be autofed to the printer.
-INIT	57	Line Printer Initialize: This open-drain line provides the line printer with a signal that allows the line printer initialization routine to be started.
-SLIN	58	Line Printer Select: This open-drain line selects the printer when it is active low.
INT2	59	Printer Port Interrupt - This signal is an active high, three-state output, generated by the positive transition of -ACK. It is enabled by bit 4 of the Write Control Register.
-ERROR	63	Line Printer Error - This is an input line from the line printer. The line printer reports an error by holding this line low during the error condition.
SLCT	65	Line Printer Selected - This is an input line from the line printer that goes high when the line printer has been selected.
BUSY	66	Line Printer Busy - This is an input line from the line printer that goes high when the line printer is not ready to accept data.
PE	67	Line Printer Paper Empty - This is an input line from the line printer that goes high when the printer runs out of paper.
-ACK	68	Line Printer Acknowledge - This input goes low to indicate a successful data transfer has taken place. It generates a printer port interrupt during its positive transition.

FUNCTIONAL DESCRIPTION:

SERIAL CHANNEL REGISTERS

Three types of internal registers are used in each serial channel of the VL16C452. They are used in the operation of the device, and are the control, status, and data registers. The control registers are the Bit Rate Select Register DLL (Divisor Latch LSB) and DLM (Divisor Latch MSB), Line Control Register, Interrupt Enable Register, and the Modem Control registers, while the status registers are the Line Status Registers and the Modem Status Register. The data registers are the Receiver Buffer Register and the Transmitter Holding Register. The Address, Read, and Write inputs are used in conjunction with the Divisor Latch Access Bit in the Line Control Register [LCR(7)] to select the register to be written or read (see Table 1). Individual bits within these registers are referred to by the register mnemonic and the bit number in parenthesis. An example, LCR(7) refers to Line Control Register Bit 7.

The Transmitter Buffer Register and Receiver Buffer Register are data registers holding from five to eight bits of data. If less than eight data bits are transmitted, data is right justified to the

LSB. Bit 0 of a data word is always the first serial data bit received and transmitted. The VL16C452 data registers are double-buffered so that read and write operations can be performed at the same time the UART is performing the parallel-to-serial and serial-to-parallel conversion.

The format of the data character is controlled by the Line Control Register. The contents of the LCR may be read, eliminating the need for separate storage of the line characteristics in system memory. The contents of the LCR are described below:

- LCR (0) Word Length Select Bit 0 (WLS0)
- LCR (1) Word Length Select Bit 1 (WLS1)
- LCR (2) Stop Bit Select (STB)
- LCR (3) Parity Enable (PEN)
- LCR (4) Even Parity Select (EPS)
- LCR (5) Stick Parity
- LCR (6) Set Break
- LCR (7) Divisor Latch Access Bit (DLAB)

LCR (0) and LCR(1) word length select bit 1: The number of bits in each serial character is programmed as shown in the following chart:

LCR(1)	LCR(0)	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

LCR(2) Stop Bit Select: LCR(2) specifies the number of stop bits in each transmitted character. If LCR(2) is a logic 0, one stop bit is generated in the transmitted data. If LCR(2) is a logic 1 when a 5-bit word length is selected, 1.5 stop bits are generated. If LCR(2) is a logic 1 when either a 6-, 7-, or 8-bit word length is selected, two stop bits are generated. The receiver checks for two stop bits if programmed.

LCR(3) Parity Enable: When LCR(3) is high, a parity bit between the last data word bit and stop bit is generated and checked.

LCR(4) Even Parity Select: When parity is enabled [LCR(3)=1], LCR(4)=0 selects odd parity, and LCR(4)=1 selects even parity.

LCR(5) Stick Parity: When parity is enabled [LCR(3)=1], CLR(5)=1 causes the transmission and reception of a parity bit to be in the opposite state from that indicated by LCR(4). This allows the user to force parity to a known state and for the receiver to check the parity bit in a known state.

LCR(6) Break Control: When LCR(6) is set to a logic "1", the serial output (SOUT) is forced to the spacing (logic 0) state. The break is disabled by setting LCR(6) to a logic "0". The Break Control bit acts only on SOUT and has no effect on the transmitter logic. Break Control enables the CPU to alert a terminal in a computer communications system. If the following sequence is used, no erroneous or extraneous characters will be transmitted because of the break.

1. Load an all "0"s pad character in response to THRE.
2. Set break in response to the next THRE.
3. Wait for the transmitter to be idle (TEMT=1), and clear break when normal transmission has to be restored.

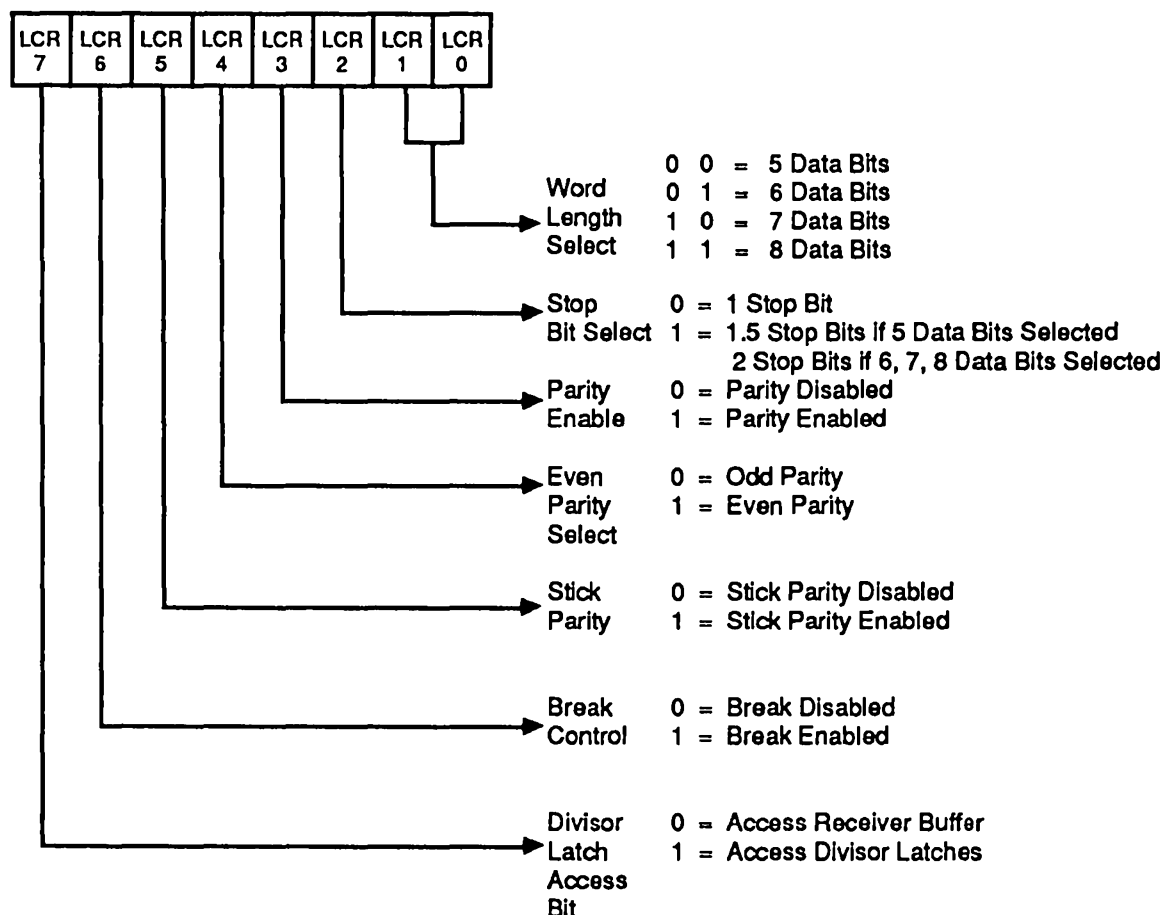
TABLE 1. SERIAL CHANNEL INTERNAL REGISTERS

DLAB	A2	A1	A0	Mnemonic	Register
0	0	0	0	RBR	Receiver Buffer Register (read only)
0	0	0	0	THR	Transmitter Holding Register (write only)
0	0	0	1	IER	Interrupt Enable Register
X	0	1	0	IIR	Interrupt Identification Register (read only)
X	0	1	1	LCR	Line Control Register
X	1	0	0	MCR	Modem Control Register
X	1	0	1	LSR	Line Status Register
X	1	1	0	MSR	Modem Status Register
X	1	1	1	SCR	Scratch Register
1	0	0	0	DLL	Divisor Latch (LSB)
1	0	0	1	DLM	Divisor Latch (MSB)

X = "Don't Care" 0 = Logic Low 1 = Logic High

Note: Serial Channel 0 is accessed when -CS0 is low; Serial Channel 1 is accessed when -CS1 is low. Selecting both channels simultaneously is an invalid condition.

FIGURE 1. LINE CONTROL REGISTER



LCR(7) Divisor Latch Access Bit (DLAB): LCR(7) must be set high (logic "1") to access the Divisor Latches DLL and DLM of the Baud Rate Generator during a read or write operation. LCR(7) must be input low to access the Receiver Buffer, the Transmitter Holding, or the Interrupt Enable Registers.

The Line Status Register (LSR) is a single register that provides status indications. The LSR is usually the first register read by the CPU to determine the cause of an interrupt or to poll the status of each serial channel of the VL16C452.

Three error flags OE, FE, and PE provide the status of any error conditions detected in the receiver circuitry. During reception of the stop bits, the error flags are set high by an error condition. The error flags are not reset by the absence of an error condition in the next received character. The flags reflect the last character only if no overrun occurred. The Overrun Error

character in the Receiver Buffer Register has been overwritten by a character from the Receiver Shift Register before being read by the CPU. The character is thereby lost. Framing Error (FE) indicates that the last character received contained incorrect (low) stop bits. This is caused by the absence of the required stop bit or by a stop bit too short to be detected. Parity Error (PE) indicates that the last character received had a parity error based on the programmed and calculated parity of the received character.

The Break Interrupt (BI) status bit indicates that the last character received was a break character. A break character is an invalid data character. However, it is an entire character, including parity and stop bits.

The Transmitter Holding Register Empty (THRE) bit indicates that the THR register is empty and may receive another character. The Transmission Shift Register Empty (TEMT) bit

indicates that the Transmitter Shift Register is empty, and the serial channel has completed transmission of the last character to be sent. If the interrupt is enabled [IER(1)], an active THRE causes an interrupt (INTRPT).

The Data Ready (DR) bit indicates that the RBR has been loaded with a received character (including Break) and that the CPU may access this data.

Reading the LSR clears LSR(1)-LSR(4). (OE, PE, FE, and BI.)

The contents of the Line Status Register shown in Table 2 are described below:

LSR(0) Data Ready (DR): Data Ready is set high when an incoming character has been received and transferred into the Receiver Buffer Register. LSR(0) is reset low by a CPU read of the data in the Receiver Buffer Register.

LSR(1) Overrun Error (OE): Overrun Error indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was

TABLE 2. LINE STATUS REGISTER BITS

LSR BITS	Logic 1	Logic 0
LSR (0) Data Ready (DR)	Ready	Not Ready
LSR (1) Overrun Error (OE)	Error	No Error
LSR (2) Parity Error (PE)	Error	No Error
LSR (3) Framing Error (FE)	Error	No Error
LSR (4) Break Interrupt (BI)	Break	No Break
LSR (5) Transmitter Holding Register Empty (THRE)	Empty	Not Empty
LSR (6) Transmitter Empty (TEMT)	Empty	Not Empty
LSR (7) Not Used		

transferred into the Receiver Buffer Register, overwriting the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.

LSR(2) Parity Error (PE): Parity Error indicates that the received data character does not have the correct even or odd parity, as selected by the Even Parity Select bit (LCR(4)). The PE bit is set high upon detection of a parity error, and is reset low when the CPU reads the contents of the LSR.

LSR(3) Framing Error (FE): Framing Error indicates that the received character did not have a valid stop bit. LSR(3) is set high when the stop bit following the last data bit or parity bit is detected as a zero bit (spacing level). The FE indicator is reset low when the CPU reads the contents of the LSR.

LSR(4) Break Interrupt (BI): Break Interrupt is set high when the received data input is held in the spacing (logic 0) state for longer than a full word transmission time (start bit + data bits + parity + stop bits). The BI indicator is reset when the CPU reads the contents of the Line Status Register.

LSR(1) - LSR(4) are the error conditions that produce a Receiver Line Status interrupt (priority 1 interrupt in the Interrupt Identification Register (IIR)) when any of the conditions are detected. This interrupt is enabled by setting IER(2)=1 in the Interrupt Enable Register.

LSR(5) Transmitter Holding Register Empty (THRE): THRE indicates that the VL82C50A is ready to accept a new character for transmission. The THRE

bit is set high when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. LSR(5) is reset low by the loading of the Transmitter Holding Register by the CPU. LSR(5) is not reset by a CPU read of the LSR.

When the THRE interrupt is enabled (IER(1)=1), THRE causes a priority 3 interrupt in the IIR. If THRE is the interrupt source indicated in IIR, INTRPT is cleared by a read of the IIR.

LSR(6) Transmitter Empty (TEMT): TEMT is set high when the Transmitter Holding Register (THR) and the Transmitter Shift Register (TSR) are both empty. LSR(6) is reset low when a character is loaded into the THR and remains low until the character is transferred out of SOUT. TEMT is not reset low by a CPU read of the LSR.

LSR(7): This bit is always 0.

The Modem Control Register (MCR) controls the interface with the modem or data set as described in Table 3.

MCR can be written and read. The -RTS and -DTR outputs are directly controlled by their control bits in this register. A high input asserts a low (true) at the output pins. MCR Bits 0, 1, 3, and 4 are shown below:

MCR(0): When MCR(0) is set high, the -DTR output is forced low. When MCR(0) is reset low, the -DTR output is forced high. The -DTR output of the serial channel may be input into an inverting line driver in order to obtain the proper polarity input at the modem or data set.

MCR(1): When MCR(1) is set high, the RTS output is forced low. When MCR(1) is reset low, the -RTS output is forced high. The -RTS output of the serial channel may be input into an inverting line driver in order to obtain the proper polarity input at the modem or data set.

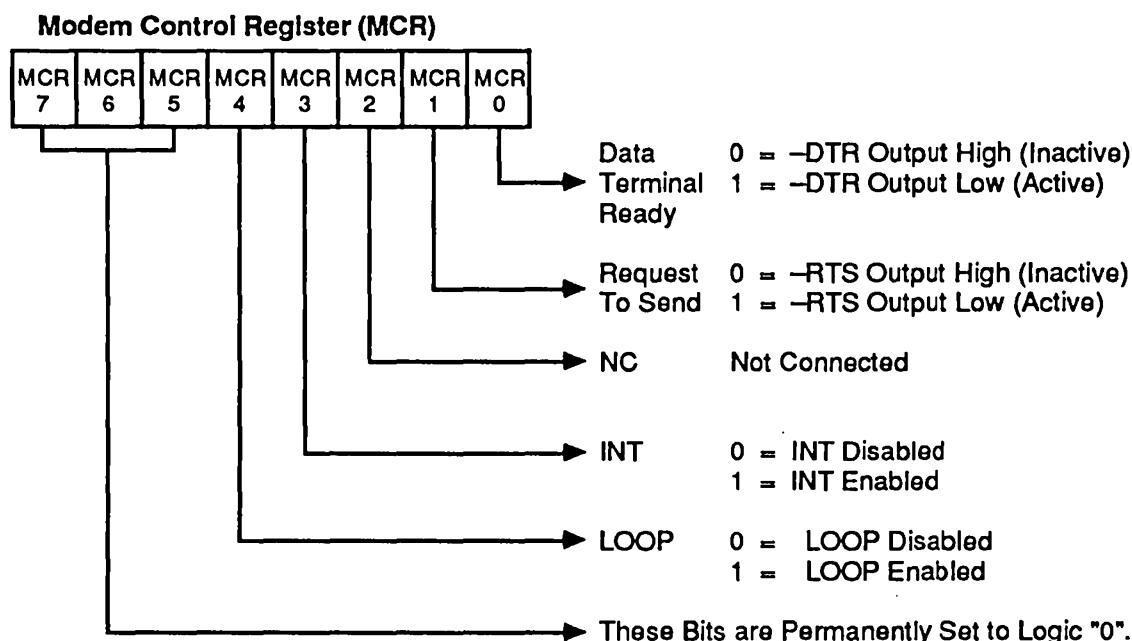
MCR(3): When MCR(3) is set high, the INT output is enabled.

MCR(4): MCR(4) provides a local loopback feature for diagnostic testing of the channel. When MCR(4) is set high, Serial Output (SOUT) is set to the marking (logic "1") state, and the receiver data input Serial Input (SIN) is disconnected. The output of the Transmitter Shift Register is looped back into the Receiver Shift Register input. The three modem control inputs (-CTS, -DSR, and -RI) are disconnected. The modem control outputs (-DTR and -RTS) are internally connected to the four modem control inputs. The modem control output pins are forced to their inactive state (high).

TABLE 3. MODEM CONTROL REGISTER BITS

MCR BITS	Logic 1	Logic 0
MCR (0) Data Terminal Ready (DTR)	-DTR Output Low	-DTR Output High
MCR (1) Request to Send (RTS)	-RTS Output Low	-RTS Output High
MCR (2) 0		
MCR (3) Interrupt (INT) Enable	INT Enabled	INT Disabled
MCR (4) LOOP	Loop Enabled	Loop Disabled
MCR (5) 0		
MCR (6) 0		
MCR (7) 0		

FIGURE 2. MODEM CONTROL REGISTER



In the diagnostic mode, data transmitted is immediately received. This allows the processor to verify the transmit and receive data paths of the selected serial channel. Bits MCR(5) - MCR(7) are permanently set to logic 0.

The MSR provides the CPU with status of the modem input lines from the modem or peripheral devices. The MSR allows the CPU to read each of the serial channel modem signal inputs by accessing the data bus interface of the VL16C452. In addition to the current status information, four bits of the MSR indicate whether the modem inputs have changed since the last reading of the MSR. The delta status bits are set high when a control input from the modem changes state, and reset low when the CPU reads the MSR.

The modem input lines for each channel are -CTS, -DSR, -RI, and -RLSD.

MSR(4) - MSR(7) are status indications of these lines. The status indications follow the status of the input lines. If the modem status interrupt in the Interrupt Enable Register is enabled [IER(3)], a change of state in a modem input signals will be reflected by the modem status bits in the IIR register, and an interrupt (INTRPT) is generated. The MSR is a priority 4 interrupt. The contents of the Modem Status Register are described in Table 4. Note that the state (high or low) of the status bits are

inverted versions of the actual input pins.

MSR(0) Delta Clear to Send (DCTS): DCTS indicates that the -CTS input to the serial channel has changed state since the last time it was read by the CPU.

MSR(1) Delta Data Set Ready (DDSR): DDSR indicates that the -DSR input to the serial channel has changed state since the last time it was read by the CPU.

MSR(2) Trailing Edge of Ring Indicator (TERI): TERI indicates that the -RI input to the serial channel has changed state from high to low since the last time it was read by the CPU. Low to high transitions on -RI do not activate TERI.

MSR(3) Delta Data Carrier Detect (DRSLD): DRSLD indicates that the

-RSLD input to the serial channel has changed state since the last time it was read by the CPU.

MSR(4) Clear to Send (CTS): Clear to Send (CTS) is the status of the -CTS input from the modem indicating to the serial channel that the modem is ready to receive data from the serial channel's transmitter output (SOUT). If the serial channel is in loop mode [MSR(4)=1], MSR(4) is equivalent to -RTS in the MCR.

MSR(5) Data Set Ready (DSR): Data Set Ready (DSR) is a status of the -DSR input from the modem to the serial channel which indicates that the modem is ready to provide received data to the serial channel receiver circuitry. If the channel is in the loop mode [MCR(4)=1], MSR(5) is equivalent to the DTR in the MCR.

TABLE 4. MODEM STATUS REGISTER BITS

MSR Bit	Mnemonic	Description
MSR (1)	DDSR	Delta Data Set Ready
MSR (2)	TERI	Trailing Edge of Ring Indicator
MSR (0)	DCTS	Delta Clear to Send
MSR (3)	DRSLD	Delta Data Carrier Detect
MSR (4)	-CTS	Clear To Send
MSR (5)	-DSR	Data Set Ready
MSR (6)	-RI	Ring Indicator
MSR (7)	-RLSD	Receiver Line Signal Detect

MSR(6) Ring Indicator: Indicates the status to the RI input (pin 39). If the channel is in the loop mode [MCR(4)=1], MSR(6) is not connected in the MCR.

MSR(7) Receive Line Signal Detect : Receive Line Signal Detect indicates the status of the Receive Line Signal Detect (–RLSD) input . If the channel is in the loop mode [MCR(4)-1], MSR(4) is equivalent to OUT2 of the MCR.

The modem status inputs (–RI, –RLSD, –DSR, and –CTS) reflect the modem input lines with any change of status. Reading the MSR register will clear the delta modem status indications but has no effect on the status bits. The status bits reflect the state of the input pins regardless of the mask control signals. If a DCTS, DDSR, TERI, or DRLSD are true, and a state change occurs during a read operation (–IOR), the state change is not indicated in the MSR. If DCTS, DDSR, TERI, or DRLSD are false, and a state change occurs during a read operation, the state change is indicated after the read operation.

For LSR and MSR, the setting of status bits is inhibited during status register read –IOR operations. If a status condition is generated during a read –IOR operation, the status bit is not set until the trailing edge of the read –IOR.

If a status bit is set during a read –IOR operation, and the same status condition occurs, that status bit will be cleared at the trailing edge of the read –IOR instead of being set again.

Each VL16C452 serial channel contains a programmable Baud Rate Generator (BRG) that divides the clock (DC to 3.1 MHz) by any divisor from 1 to 2^{16-1} (see also BRG description). The output frequency of the Baud Generator is 16X the data rate [divisor # = clock ÷ (baud rate x 16)]. Two 8-bit divisor latch registers store the divisor in a 16-bit binary format. These Divisor Latch registers must be loaded during initialization. Upon loading either of the Divisor latches, a 16-bit baud counter is immediately loaded. This prevents long counts on initial load.

The receiver circuitry in each serial channel of the VL16C452 is programmable for 5, 6, 7, or 8 data bits per

character. For words of less than 8 bits, the data is right justified to the least significant bit LSB = Data Bit 0 [RBR(0)]. Data Bit 0 of a data word [RBR(0)] is the first data bit received. The unused bits in a character less than 8 bits are output low to the parallel output by the serial channel.

Received data at the SIN input pin is shifted into the Receiver Shift Register by the 16X clock provided at the RCLK input. This clock is synchronized to the incoming data based on the position of the start bit. When a complete character is shifted into the Receiver Shift Register, the assembled data bits are parallel loaded into the Receiver Buffer Register. The DR flag in the LSR register is set.

Double buffering of the received data permits continuous reception of data without losing received data. While the Receiver Shift Register is shifting a new character into the serial channel, the Receiver Buffer Register is holding a previously received character for the CPU to read. Failure to read the data in the RBR before complete reception of the next character result in the low of the data in the Receiver Register. The OE flag in the LSR register indicates the overrun condition.

RBR Bits 0 thru 7:

RBR(0)	Data Bit 0
RBR(1)	Data Bit 1
RBR(2)	Data Bit 2
RBR(3)	Data Bit 3
RBR(4)	Data Bit 4
RBR(5)	Data Bit 5
RBR(6)	Data Bit 6
RBR(7)	Data Bit 7

The Transmitter Holding Register (THR) holds parallel data from the data bus (D0-D7) until the Transmitter Shift Register is empty and ready to accept a new character for transmission. The transmitter and receiver word length and number of stop bits are the same. If the character is less than eight bits, unused bits at the microprocessor data bus are ignored by the transmitter.

Data Bit 0 [THR(0)] is the first serial data bit transmitted. The THRE flag [LSR(5)] reflect the status of the THR. The TEMT flag [LSR(5)] indicates if both the THR and TSR are empty.

THR Bits 0 thru 7

THR(0)	Data Bit 0
THR(1)	Data Bit 1
THR(2)	Data Bit 2
THR(3)	Data Bit 3
THR(4)	Data Bit 4
THR(5)	Data Bit 5
THR(6)	Data Bit 6
THR(7)	Data Bit 7

Scratchpad Register is an 8-bit Read/Write register that has no effect on any channel in the VL16C452. It is intended to be used by the programmer to hold data temporarily.

SCR Bits 0 thru 7

SCR(0)	Data Bit 0
SCR(1)	Data Bit 1
SCR(2)	Data Bit 2
SCR(3)	Data Bit 3
SCR(4)	Data Bit 4
SCR(5)	Data Bit 5
SCR(6)	Data Bit 6
SCR(7)	Data Bit 7

INTERRUPTS

The Interrupt Identification Register (IIR) of each serial channel of the VL16C452 has interrupt capability for interfacing to current microprocessors. In order to minimize software overhead during data character transfers, the serial channel prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows:

1. Receiver Line Status (priority 1)
2. Received Data Ready (priority 2)
3. Transmitter Holding Register Empty (priority 3)
4. Modem Status (priority 4)

Information indicating that a prioritized interrupt is pending and the type of interrupt is stored in the Interrupt Identification Register (IIR). When addressed during chip select time, the IIR indicates the highest priority interrupt pending. No other interrupts are acknowledged until the interrupt is serviced by the CPU. The logic equivalent of the interrupt control circuit is shown in Figure 3. The contents of the IIR are indicated in Table 5 and are described below.

IIR(0): IIR(0) can be used in either a hard-wired prioritized or polled environment to indicate whether an interrupt is pending. When IIR(0) is low, an interrupt is pending, and IIR contents

TABLE 5. INTERRUPT IDENTIFICATION REGISTER

INTERRUPT IDENTIFICATION				INTERRUPT SET AND RESET FUNCTIONS		
Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Flag	Interrupt Source	Interrupt Reset Control
X	X	1		None	None	
1	1	0	First	Receiver Line Status	OE, PE, FE, or BI	LSR Read
1	0	0	Second	Received Data Available	Received Data Available	RBR Read
0	1	0	Third	THRE	THRE	IIR Read if THRE is the Interrupt Source or THR Write
0	0	0	Fourth	Modem Status	-CTS, -DSR, -RI, -RSLD	MSR Read

X = Not Defined.

FIGURE 3. INTERRUPT CONTROL LOGIC

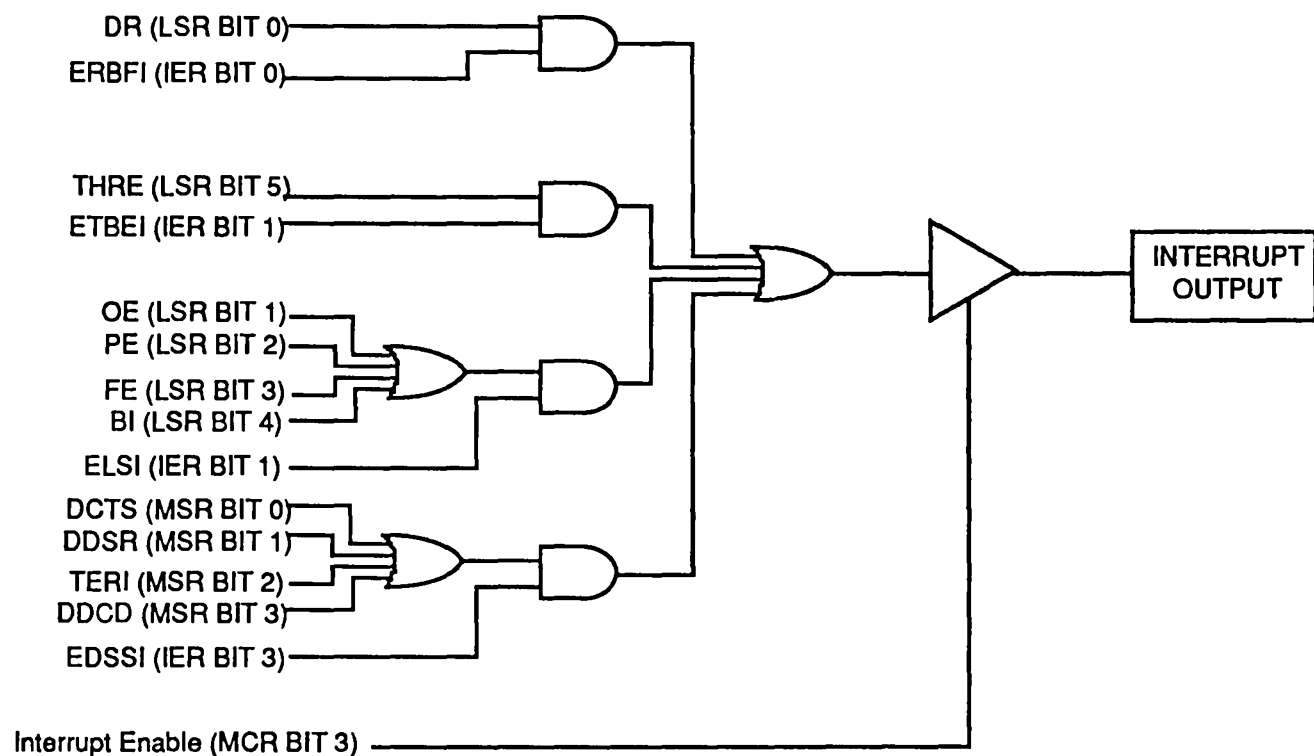


TABLE 6. SERIAL CHANNEL ACCESSIBLE REGISTERS

Register Mnemonic	Register Bit Number							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RBR (Read Only)	Data Bit 7 (MSB)	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0 (LSB)*
THR (Write Only)	Data Bit 7	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0
DLL	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DLM	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
IER	0	0	0	0	(EDSSI) Enable Modem Status Interrupt	(ELSI) Enable Receiver Line Status Interrupt	(ETBEI) Enable Transmitter Holding Register Empty Interrupt	(ERBFI) Enable Received Data Available Interrupt
IIR (Read Only)	0	0	0	0	0	Interrupt ID Bit (1)	Interrupt ID Bit (0)	"0" 1F Interrupt Pending
LCR	(DLAB) Divisor Latch Access Bit	Set Break	Stick Parity	(EPS) Even Parity Select	(PEN) Parity Enable	(STB) Number of Stop Bits	(WLSB1) Word Length Select Bit 1	(WLSB0) Word Length Select Bit 0
MCR	0	0	0	Loop	Out 2	Out 1	(RTS) Request To Send	(DTR) Data Terminal Ready
LSR	0	(TEMT) Transmitter Empty	(THRE) Transmitter Holding Register Empty	(BI) Break Interrupt	(FE) Framing Error	(PE) Parity Error	(OE) Overrun Error	(DR) Data Ready
MSR	(DCD) Data Carrier Detect	(RI) Ring Indicator	(DSR) Data Ready Set	(CTS) Clear to Send	(DRSLD) Delta Receive Line Signal Detect	(TERI) Trailing Edge Ring Indicator	(DDSR) Delta Data Set Ready	(DCTS) Delta Clear to Send
SCR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

*LSB Data Bit 0 is the first bit transmitted or received.

may be used as a pointer to the appropriate interrupt service routine. When IIR(0) is high, no interrupt is pending.

IIR(1) and IIR(2) are used to identify the highest priority interrupt pending as indicated in Table 2.

IIR(3) - IIR(7): These five bits of the IIR are logic 0.

The Interrupt Enable Register (IER) is a Write register used to independently enable the four serial channel interrupts which activate the interrupt (INTRPT) output. All interrupts are disabled by resetting IER(0) - IER(3) of the Interrupt Enable Register. Interrupts are enabled by setting the appropriate bits of the IER high. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INTRPT output. All other system functions operate in their normal manner, including the setting of the Line Status and Modem Status Registers. The contents of the Interrupt Enable Register is described in Table 3 and below:

IER(0): When programmed high [IER(0)=Logic 1], IER(0) enables Received Data Available interrupt.

IER(1): When programmed high [IER(1)=Logic 1], IER(1) enables the Transmitter Holding Register Empty interrupt.

IER(2): When programmed high [IER(2)=Logic 1], IER(2) enables the Receiver Line Status interrupt.

IER(3): When programmed high [IER(3)=Logic 1], IER(3) enables the Modem Status Interrupt.

IER(4) - IER(7): These four bits of the IER are logic 0.

TRANSMITTER

The serial transmitter section consists of a Transmitter Holding Register (THR), Transmitter Shift Register (TSR), and associated control logic. The Transmitter Holding Register Empty (THRE) and Transmitter Shift Register Empty (TEMT) are two bits in the Line Status Register which indicate the status of THR and TSR. To transmit a 5- to 8-bit word, the word is written through D0-D7 to the THR. The microprocessor should perform a write operation only if THRE is high. The THRE is set high when the word is automatically transferred from

the THR to the TSR during the transmission of the start bit.

When the transmitter is idle, THRE and TEMT are high. The first word written causes THRE to be reset to 0. After the transfer, THRE returns high. TEMT remains low for at least the duration of the transmission of the data word. If a second character is transmitted to the THR, the THRE is reset low. Since the data word cannot be transferred from the THR to the TSR until the TSR is empty, THRE remains low until the TSR has completed sending the word. When the last word has been transmitted out of the TSR, TEMT is set high. THRE is set high one THR to TSR transfer time later.

RECEIVER

Serial asynchronous data is input into the SIN pin. The idle state of the line providing the input into SIN is high. A start bit detect circuit continually searches for a high to low transition from the idle state. When the transition is detected, a counter is reset, and counts the 16X clock to 7 1/2, which is the center of the start bit. The start bit is valid if the SIN is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the SIN input.

The Line Control Register determines the number of data bits in a character (LCR(0), LCR(1)), number of stop bits LCR(2), if parity is used LCR(3), and the polarity of parity LCR(4). Status for the receiver is provided in the Line Status Register to the Receiver Buffer Register, the Data Received indication in LSR(0) is set high. The CPU reads the Receiver Buffer Register through D0-D7. This read resets LSR(0). If D0-D7 are not read prior to a new character transfer from the RSR to the RBR, the overrun error status indication is set in LSR(1). The parity check tests for even or odd parity on the parity bit, which precedes the first stop bit. If there is a parity error, the parity error is set in LSR(2). There is circuitry which tests whether the stop bit is high. If it is not, a framing error indication is generated in LSR(3).

The center of the start bit is defined as clock count 7 1/2. If the data into SIN is symmetrical square wave, the center of the data cells will occur within

+/- 3.125% of the actual center, providing an error margin of 46.875%. The start bit can begin as much as one 16X clock cycle prior to being detected.

BAUD RATE GENERATOR (BRG)

The BRG generates the clocking for the UART function, providing standard ANSI/CCITT bit rates. The oscillator driving the BRG is provided by an external clock into CLK.

The data rate is determined by the Divisor Latch registers DLL and DLM and the external frequency. The bit rate is selected by programming the two divisor latches, Divisor Latch Most Significant Byte and Divisor Latch Least Significant Byte. Setting DLL=1 and DLM=0 selects the divisor to divide by 1 (divide by 1 gives maximum baud rate for a given input frequency at the CLK input).

The BRG can use any of three different popular frequencies to provide standard baud rates. These frequencies are 1.8432 MHz, 2.4576 MHz, and 3.072 MHz. With these frequencies, standard bit rates from 50 to 38.5 kbps are available. Tables 7, 8, and 9 illustrate the divisors needed to obtain standard rates using these three crystal frequencies.

RESET

After power up, the VL16C452 -RESET input should be held low for 500 ns to reset the VL16C452 circuits to an idle mode until initialization. A low on -RESET causes the following:

1. Initializes the transmitter and receiver internal clock counters.
2. Clears the Line Status Register (LSR), except for Transmitter Shift Register Empty (TEMT) and Transmit Holding Register Empty (THRE), which are set. The Modem Control Register (MCR) is also cleared. All of the discrete lines, memory elements and miscellaneous logic associated with these register bits are also cleared or turned off. The Line Control Register (LCR), Divisor Latches, Receiver Buffer Register, Transmitter Buffer Register are not effected.

Following removal of the reset condition (Reset high), the VL16C452 remains in the idle mode until programmed.



A hardware reset of the VL16C452 sets the THRE and TEMT status bit in the LSR. When interrupts are subsequently enabled, an interrupt occurs due to THRE.

A summary of the effect of a reset on the VL16C452 is given in Table 10.

PROGRAMMING

Each serial channel of the VL16C452 is programmed by the control registers LCR, IER, DLL and DLM, and MCR.

These control words define the character length, number of stop bits, parity, baud rate, and modem interface.

While the control register can be written in any order, the IER should be written to last because it controls the interrupt enables. Once a serial channel is programmed and operational, these registers can be updated any time the VL16C452 serial channel is not transmitting or receiving data.

The control signals required to access each serial channel's internal registers are shown below.

SOFTWARE RESET

A software reset of the serial channel is a useful method for returning to a

completely known state without a system reset. Such a reset consists of writing to the LCR, Divisor Latches, and MCR registers. The LSR and RBR registers should be read prior to enabling interrupts in order to clear out any residual data or status bits which may be invalid for subsequent operation.

CLOCK INPUT OPERATION

The maximum input frequency of the external clock of the VL16C452 is 3.1 MHz.

TABLE 7. BAUD RATES (1.8432 MHz CLOCK)

Desired Baud Rate	Divisor Used	Percent Error Difference Between Desired and Actual
50	2304	—
75	1536	—
110	1047	0.026
134.5	857	0.058
150	768	—
300	384	—
600	192	—
1200	96	—
1800	64	—
2000	58	0.69
2400	48	—
3600	32	—
4800	24	—
7200	16	—
9600	12	—
19200	6	—
38400	3	—
56000	2	2.86

TABLE 8. BAUD RATES (2.4576 MHz CLOCK)

Desired Baud Rate	Divisor Used	Percent Error Difference Between Desired and Actual
50	3072	—
75	2048	—
110	1396	0.026
134.5	1142	0.0007
150	1024	—
300	512	—
600	256	—
1200	128	—
1800	85	0.392
2000	77	0.260
2400	64	—
3600	43	0.775
4800	32	—
7200	21	1.587
9600	16	—
19200	8	—
38400	4	—

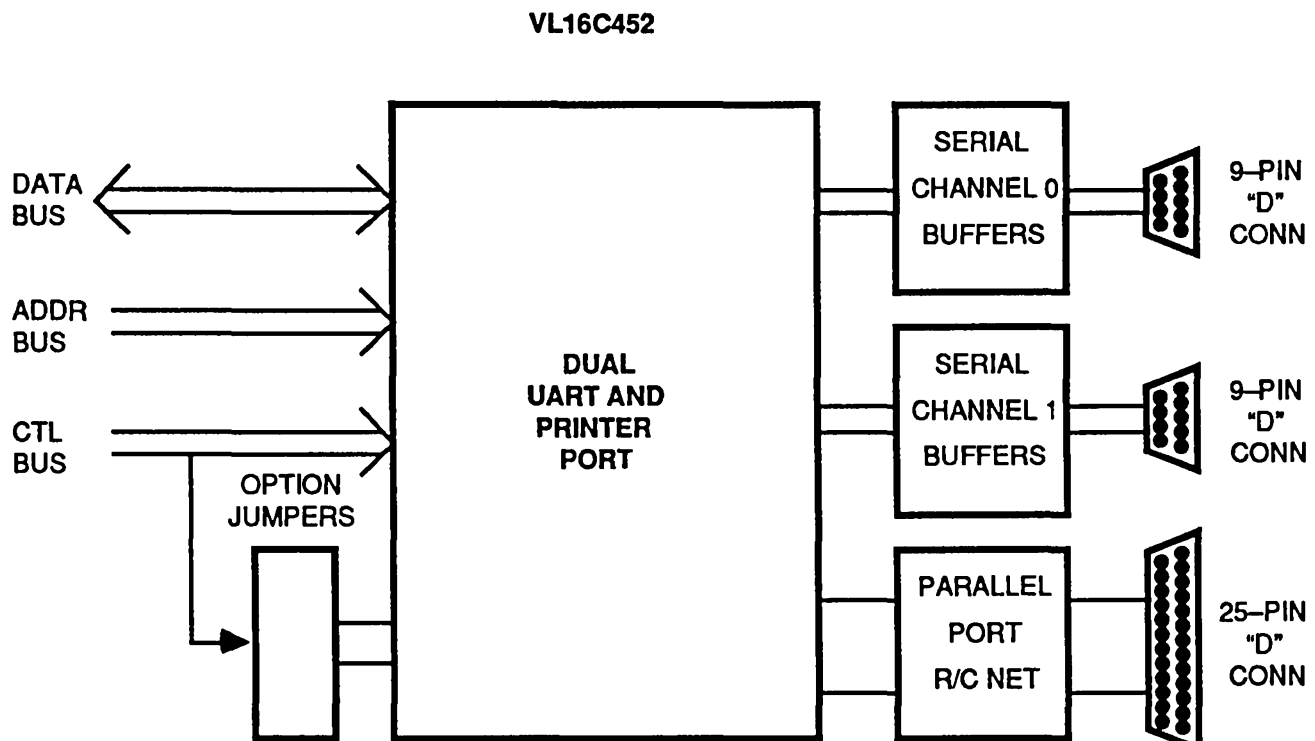
TABLE 9. BAUD RATES (3.072 MHz CLOCK)

Desired Baud Rate	Divisor Used	Percent Error Difference Between Desired and Actual
50	3840	—
75	2560	—
110	1745	0.026
134.5	1428	0.034
150	1280	—
300	640	—
600	320	—
1200	160	—
1800	107	0.312
2000	96	—
2400	80	—
3600	53	0.628
4800	40	—
7200	27	1.23
9600	20	—
19200	10	—
38400	5	—

TABLE 10. RESET

Register/Signal	Reset Control	Reset
Interrupt Enable Register	Reset	All Bits Low (0–3 forced and 4–7 permanent)
Interrupt Identification Register	Reset	Bit 0 is High, Bits 1 and 2 Low
Line Control Register	Reset	Bits 3–7 are Permanently Low
MODEM Control Register	Reset	All Bits Low
Line Status Register	Reset	All Bits Low
MODEM Status Register	Reset	All Bits Low, Except Bits 5 and 6 are High
SOUT	Reset	Bits 0–3 Low
Intrpt (RCVR Errs)	Read LSR/Reset	Bits 4–7 Input Signal
Intrpt (RCVR Data Ready)	Read RBR/Reset	High
Intrpt (THRE)	Read IIR/Write THR/Reset	Low
Intrpt (Modem Status Changes)	Read MSR/Reset	Low
–Out2	Reset	Low
–RTS	Reset	High
–DTR	Reset	High
–Out1	Reset	High

DEVICE APPLICATION





FUNCTIONAL DESCRIPTION

PARALLEL PORT REGISTERS

The VL16C452's parallel port interfaces the device to a Centronics-style printer. When Chip Select 2 (--CS2) is low, the parallel port is selected. Table 11 shows the registers associated with this parallel port. The read or write function of the register is controlled by the state of the read (--IOR) and write (--IOW) pin as shown. The Read Data Register allows the microprocessor to read the information on the parallel bus.

The Read Status Register allows the microprocessor to read the status of the printer in the five most significant bits. The status bits are Printer Busy (--BUSY), Acknowledge (--ACK) which is a handshake function, Paper Empty (PE), Printer Selected (SLCT), and Error (--ERROR). The Read Control Register allows the state of the control lines to be read. The Write Control Register sets the state of the control lines.

They are Interrupt Enable (IRQ ENB), Select In (SLIN), Initialize the Printer (--INIT), Autofeed the Paper (AUTOFD), Strobe (STROBE), which informs the printer of the presence of a valid byte on the parallel bus. The Write Data Register allows the microprocessor to write a byte to the parallel bus.

The parallel port is completely compatible with the parallel port implementation used in the IBM Serial/Parallel Adaptor.

TABLE 11. PARALLEL PORT REGISTERS

Register	Register Bits							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read Data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Read Status	--BUSY	--ACK	PE	SLCT	--ERROR	1	1	1
Read Control	1	1	1	IRQ ENB	SLIN	--INIT	AUTOFD	STROBE
Write Data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Write Control	1	1	1	IRQ ENB	SLIN	--INIT	AUTOFD	STROBE

TABLE 12. PARALLEL PORT REGISTER SELECT

Control Pins					Register Selected
--IOR	--IOW	--CS2	A1	A0	
0	1	0	0	0	Read Data
0	1	0	0	1	Read Status
0	1	0	1	0	Read Control
0	1	0	1	1	Invalid
1	0	0	0	0	Write Data
1	0	0	0	1	Invalid
1	0	0	1	0	Write Control
1	0	0	1	1	Invalid

AC CHARACTERISTICS $T_A = 0^\circ\text{C to } +70^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 5\%$ (Notes 1, 5)

Symbol	Parameter	Min	Max	Units	Conditions
tDIW	–IOR Strobe Width	125		ns	
RC	Read Cycle	360		ns	
tDDD	Delay from –IOR to Data		125	ns	100 pF Load
tHZ	–IOR to Floating Data Delay	0	100	ns	100 pF Load, Note 4
tDOW	–IOW Strobe Width	100		ns	
WC	Write Cycle	360		ns	
tDS	Data Setup Time	40		ns	
tDH	Data Hold Time	40		ns	
tRA	Address Hold Time from –IOR	20		ns	Note 2
tRCS	Chip Select Hold Time from –IOR	20		ns	Note 2
tAR	–IOR Delay from Address	60		ns	Note 2
tCSR	–IOR Delay from Chip Select	50		ns	Note 2
tWA	Address Hold Time from –IOW	20		ns	Note 2
tWCS	Chip Select Hold Time from –IOW	20		ns	Note 2
tAW	–IOW Delay from Address	60		ns	Note 2
tCSW	–IOW Delay from Select	50		ns	Note 2
tRW	Reset Pulse Width	5		μs	
tXH	Duration of Clock High Pulse	140		ns	External Clock
tXL	Duration of Clock Low Pulse	140		ns	External Clock

Notes:

1. All timing specifications apply to pins on both serial channels (e.g. RI refers to both RI0 and RI1).
2. The internal address strobe is always active.
3. RCLK = tXH and tXL.
4. Charge and discharge time is determined by VOL, VOH and the external loading.
5. All timings are referenced to valid 0 and valid 1.
(see AC TEST POINTS).
6. RCLK is internally derived from the internal –BAUDOUT signal.

**AC CHARACTERISTICS (Cont.)** TA= 0°C to +70°C, VCC= 5 V ±5% (Notes 1, 5)

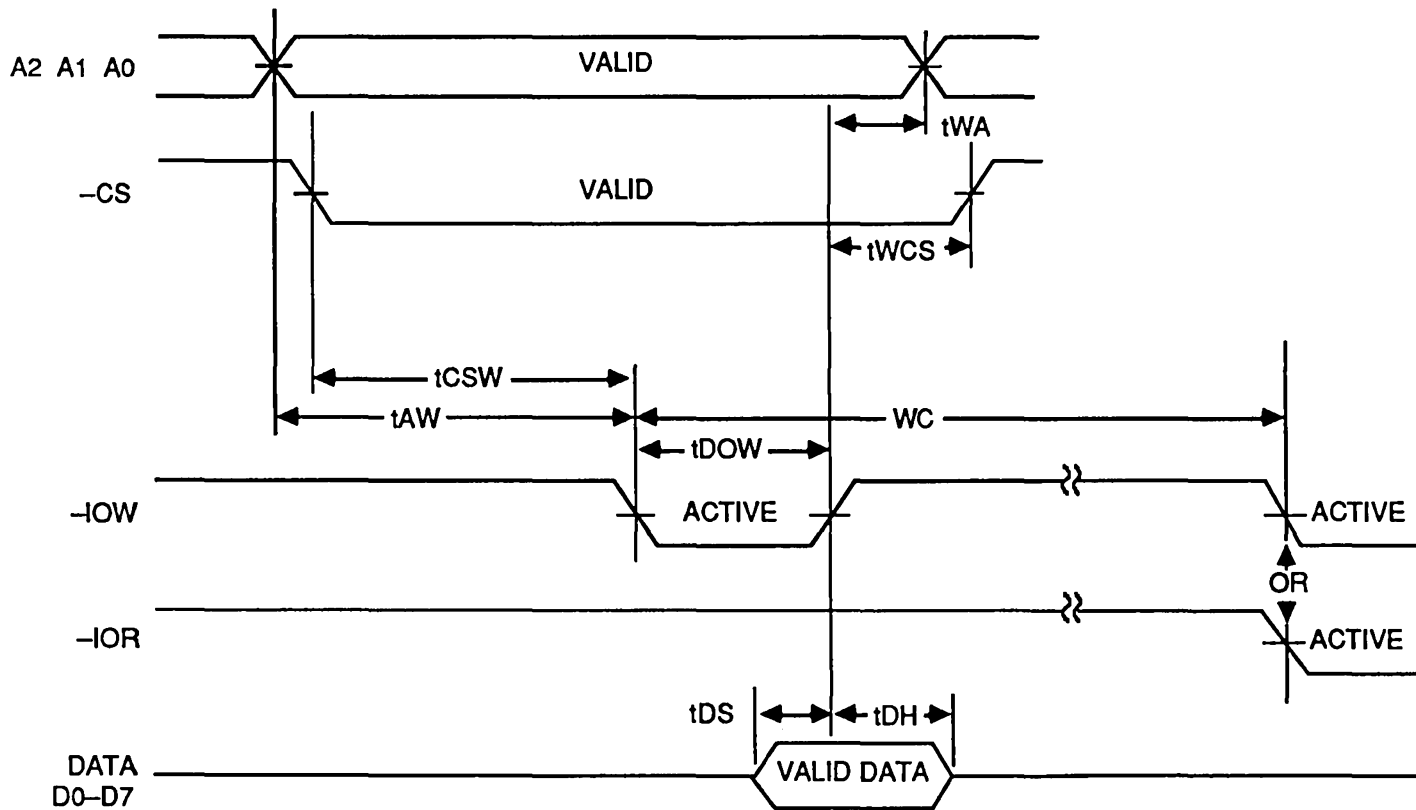
Symbol	Parameter	Min	Max	Units	Conditions
Transmitter					
tHR1	Delay from Rising Edge of --IOW (WR THR) To Reset Interrupt		175	ns	100 pF Load
tIRS	Delay from Initial INTR Reset to Transmit Start		16	CLK Cycles	Note 3
tSI	Delay from Initial Write to Interrupt	8	24	CLK Cycles	Note 3
tSTI	Delay from Stop to Interrupt (THRE)		8	CLK Cycles	Note 3
tIR	Delay from --IOR (RD IIR) to Reset Interrupt (THRE)		250	ns	100 pF Load
Modem Control					
tMDO	Delay from --IOW (WR MCR) to Output		250	ns	100 pF Load
tSIM	Delay to Set Interrupt from MODEM Input		250	ns	100 pF Load
tRIM	Delay to Reset Interrupt from --IOR (RS MSR)		250	ns	100 pF Load
Receiver					
tSINT	Delay from Stop to Set Interrupt		1	CLK Cycles	Note 3
tRINT	Delay from --IOR (RD RBR/RDLSR) to Reset Interrupt		1	μs	100 pF Load
Parallel Port					
tDT	Data Time	1		μs	
tSB	Strobe Time	1	500	μs	
tAD	Acknowledge Delay (Busy Start to Acknowledge)			μs	Defined by Printer
tAKD	Acknowledge Delay (Busy End to Acknowledge)			μs	Defined by Printer
tAK	Acknowledge Duration Time			μs	Defined by Printer
tBSY	Busy Duration Time			μs	Defined by Printer
tBSD	Busy Delay Time			μs	Defined by Printer

Notes:

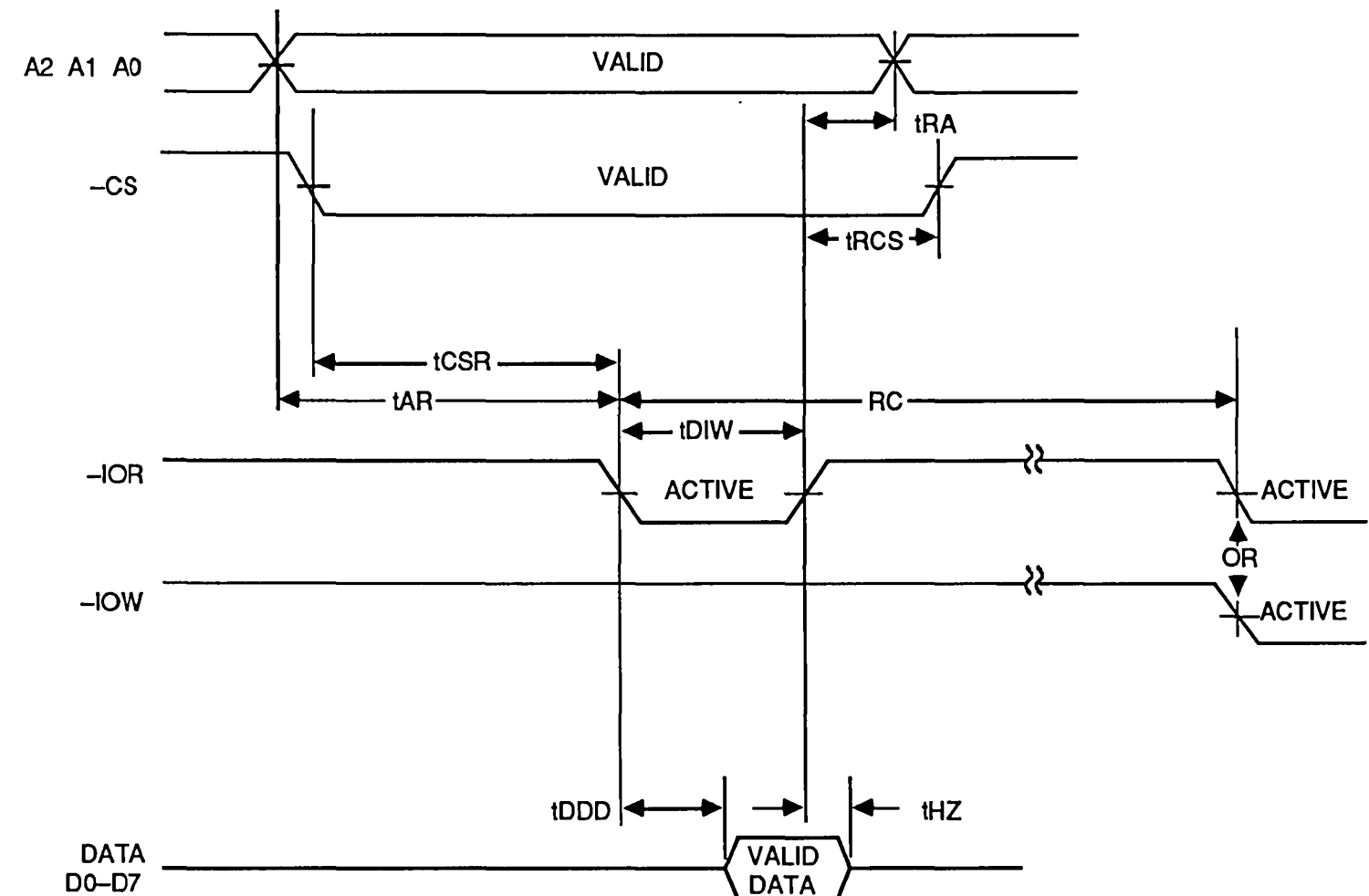
1. All timing specifications apply to pins on both serial channels (e.g. RI refers to both RI0 and RI1).
2. The internal address strobe is always active.
3. RCLK = tXH and tXL.
4. Charge and discharge time is determined by VOL, VOH and the external loading.
5. All timings are referenced to valid 0 and valid 1 (see AC TEST POINTS).



WRITE CYCLE TIMING

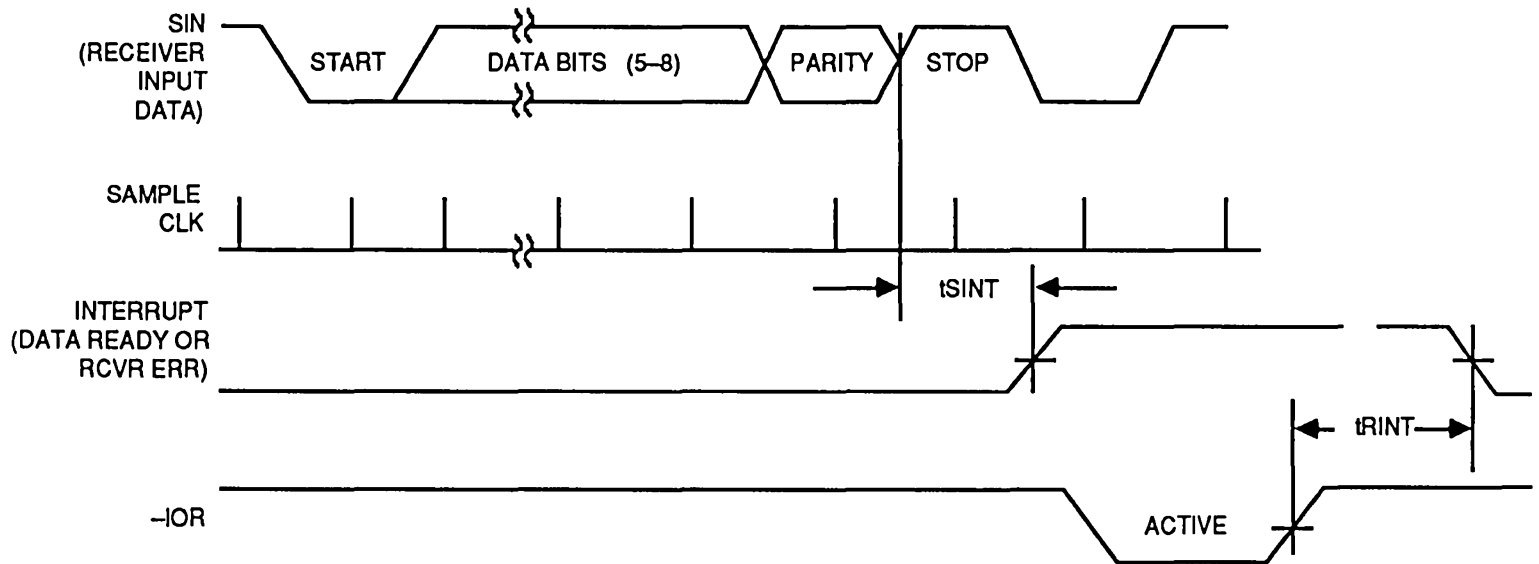


READ CYCLE TIMING

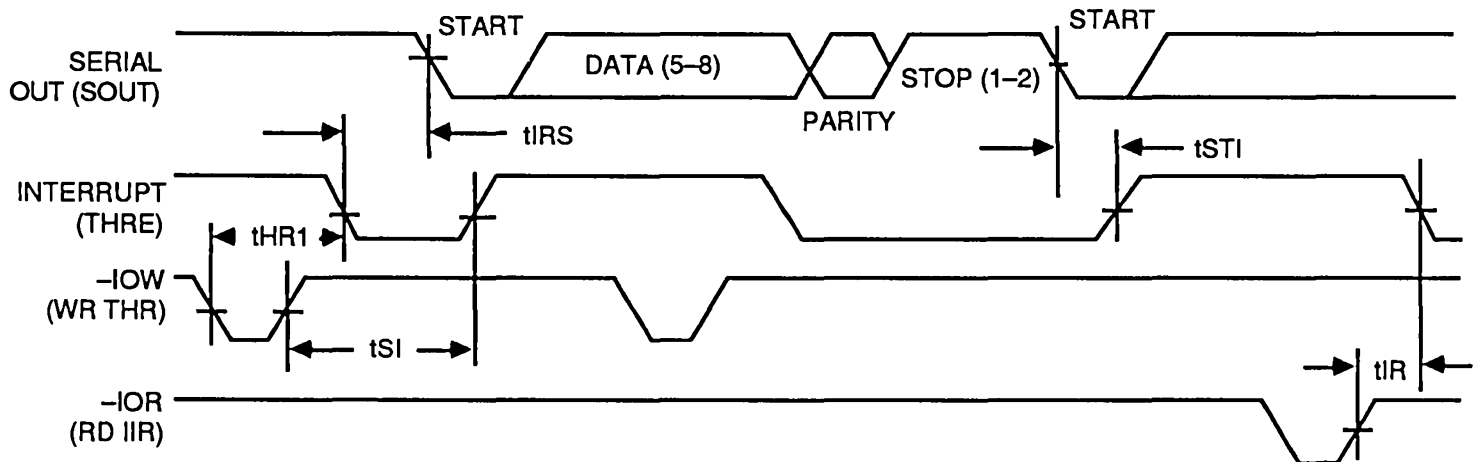




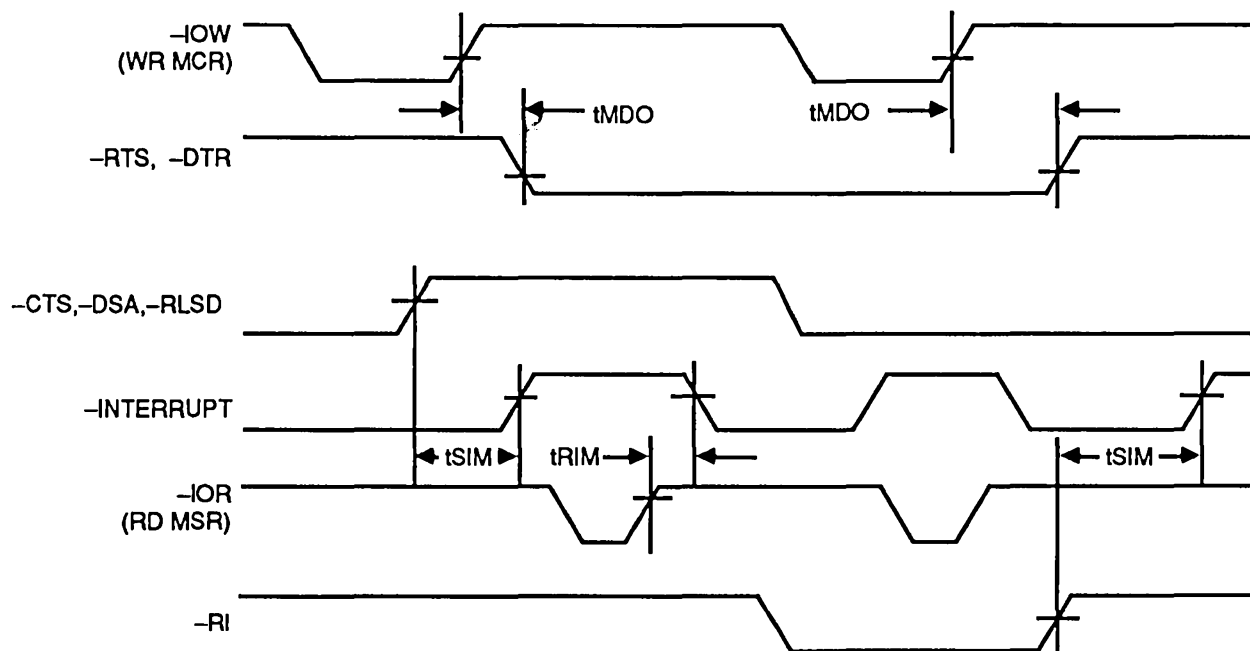
RECEIVER TIMING



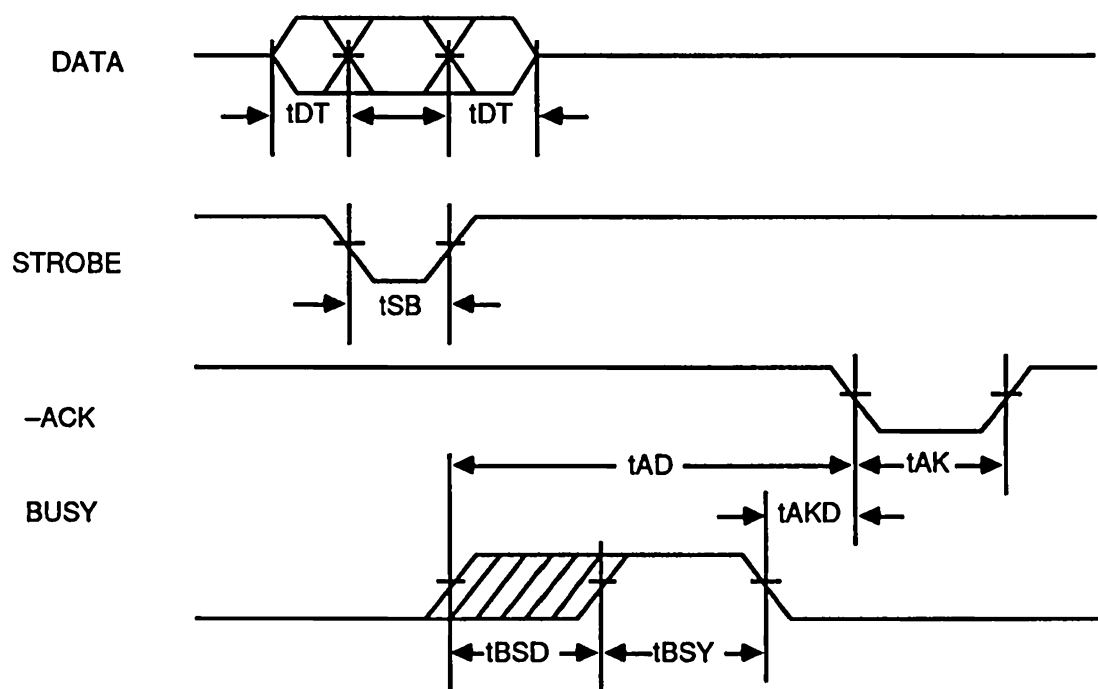
TRANSMITTER TIMING



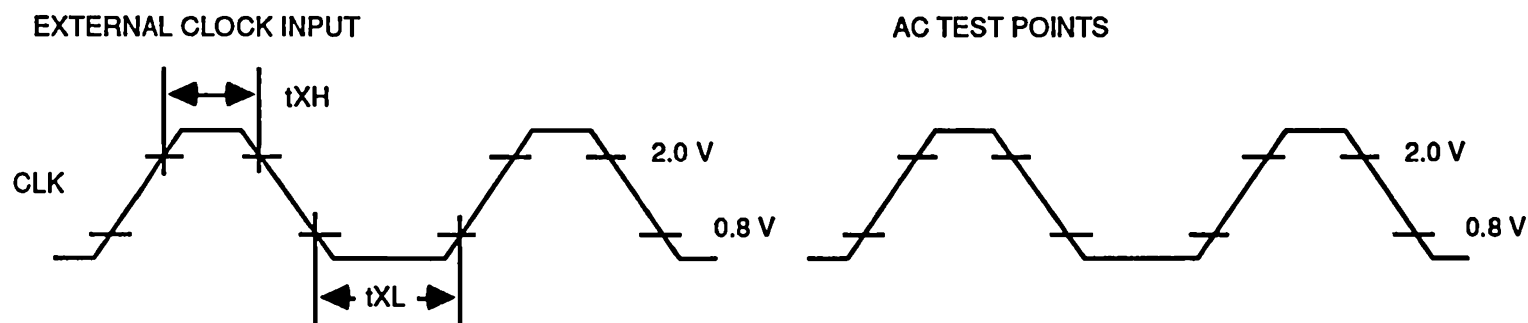
MODEM TIMING



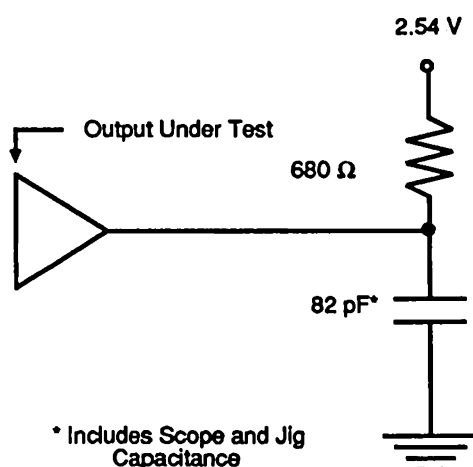
PARALLEL PORT TIMING



AC TESTING INPUT/OUTPUT WAVEFORMS



TEST CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature -10°C to $+70^{\circ}\text{C}$
 Storage Temperature -65°C to $+150^{\circ}\text{C}$
 Supply Voltage to Ground Potential -0.5 V to $\text{VCC} + 0.3\text{ V}$
 Applied Output Voltage -0.5 V to $\text{VCC} + 0.3\text{ V}$
 Applied Input Voltage -0.5 V to $+7.0\text{ V}$
 Power Dissipation 500 mW

Stresses above those listed may cause permanent damage to the device. These are stress ratings only, functional operation of this device at these or any other conditions above

those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS: $T_A = 0$ to $+70^{\circ}\text{C}$, $\text{VCC} = 5\text{ V} \pm 5\%$

Symbol	Parameter	Min	Max	Units	Conditions
VILX	Clock Input Low Voltage	-0.5	0.8	V	
VIHX	Clock Input High Voltage	2.0	VCC	V	
VIL	Input Low Voltage	-0.5	0.8	V	
VIH	Input High Voltage	2.0	VCC	V	
VOL	Output Low Voltage		0.4	V	IOL = 4.0 mA on DB0 - DB7 IOL = 12 mA on PD0 - PD7 IOL = 10 mA on -NIT, -AFD, -STB, and -SLIN (see Note 1) IOL = 2.0 mA on all other outputs
VOH	Output High Voltage	2.4		V	IOH = -0.4 mA on DB0 - DB7 IOH = -2.0 mA on PD0 - PD7 IOH = -0.2 mA on -INIT, -AFD, -STB, and -SLIN IOH = -0.2 mA on all other outputs
ICC	Power Supply Current		50	mA	VCC = 5.25 V , No loads on SIN0,1; -DSR0,1; -RLSD0,1; -CTS0,1. -RI0, -RI1 = 2.0 V . Other inputs = 0.8 V . Baud rate generator = 4 MHz . Baud rate = 56 K
IIL	Input Leakage		± 10	μA	VCC = 5.25 V , GND = 0 V . All other pins floating.
ICL	Clock Leakage		± 10	μA	VIN = 0 V , 5.25 V
IOZ	3-State Leakage		± 20	μA	VCC = 5.25 V , GND = 0 V . VOUT = 0 V , 5.25 V 1) Chip deselected 2) Chip and write mode selected
VIL(RES)	Reset Schmitt VIL		0.8	V	
VIH(RES)	Reset Schmitt VIH	2.0		V	

Note 1. -INIT, -AFD, -STB, and -SLIN are open collector output pins that each have an internal pull-up resistor ($2.5\text{ k}\Omega$ - $3.5\text{ k}\Omega$) to VCC. This will generate a maximum of 2.0 mA of internal IOL. In addition to this internal current, each pin will sink at least 10 mA , while maintaining the VOL specification of 0.4 V Max .

ASYNCHRONOUS COMMUNICATIONS ELEMENT WITH FIFOs

FEATURES

- Fully compatible with VL16C450 ACE
- 16 byte FIFO reduces CPU interrupts
- Full double buffering
- Modem control signals include -CTS, -RTS, -DSR, -DTR, -RI and -DCD
- Programmable serial characteristics:
 - 5-, 6-, 7- or 8-bit characters
 - Even-, odd-, or no-parity bit generation and detection
 - 1-, 1 1/2- or 2-stop bit generation
 - Baud rate generation (dc to 56K baud)
- Independent control of transmit, receive, line status, data set interrupts, FIFOs
- Full status reporting capabilities
- Three-state, TTL drive capabilities for bidirectional data bus and control bus

DESCRIPTIONS

The VL16C550 is an asynchronous communications element (ACE) that is functionally equivalent to the VL16C450, and additionally incorporates a 16 byte FIFO. The FIFOs are available on both the transmitter and receiver, and can be activated by placing the device in the FIFO mode. After a reset, the registers of the VL16C550 are identical to those of the VL16C450.

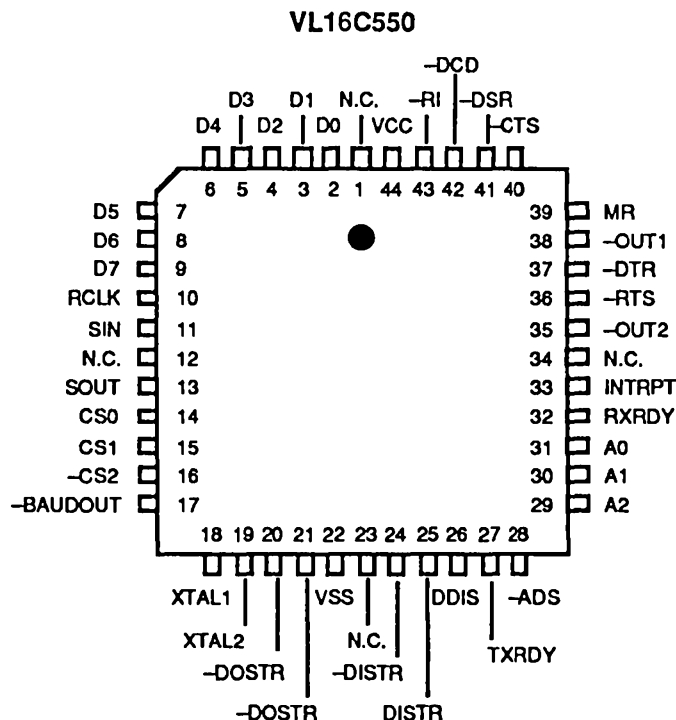
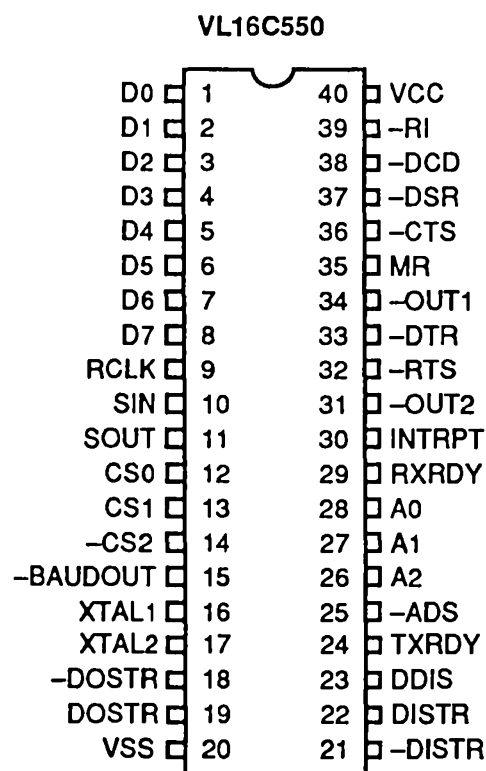
Improved VL16C550 specifications provide compatibility with most newer state-of-the-art CPUs. The VL16C550 serves as a serial data input/output interface in microcomputer systems. It performs serial-to-parallel conversion on data characters received from peripheral devices or modems, and parallel-to-serial conversion on data

characters transmitted by the CPU. In the FIFO Mode, FIFOs are enabled permitting 16 bytes to be stored in both transmit and receive mode. The FIFOs also provide three bits per byte of error data in the receiver FIFO. The complete status of the ACE can be read at any time during functional operation by the CPU. The information obtained includes the type and condition of the transfer operations being performed, and error conditions involving parity, overrun, framing, or break interrupt.

A programmable baud rate generator is included that can divide the timing reference clock input by a divisor between 1 and ($2^{16}-1$).

The VL16C550 ACE with FIFOs is available in both plastic and ceramic DIP as well as a PLCC.

PIN DIAGRAMS



ORDER INFORMATION

Part Number	External Clock Frequency	Package
VL16C550-PC	3.1 MHz	Plastic DIP
VL16C550-CC		Ceramic DIP
VL16C550-QC		Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range is 0 C to + 70 C.



FLOPPY DISK CONTROLLER/FORMATTER

FEATURES

- Built-in data separator
- Built-in write precompensation
- Single and double density
- Motor control
- 128, 256, 512, or 1024 sector lengths
- TTL compatible
- 8-bit bidirectional data bus
- Fast step rates
- 28-pin DIP
- Single 5 V power supply

DESCRIPTION

The VL1772-02 is an MOS/LSI device that performs the functions of a floppy disk controller/formatter. It replaces the

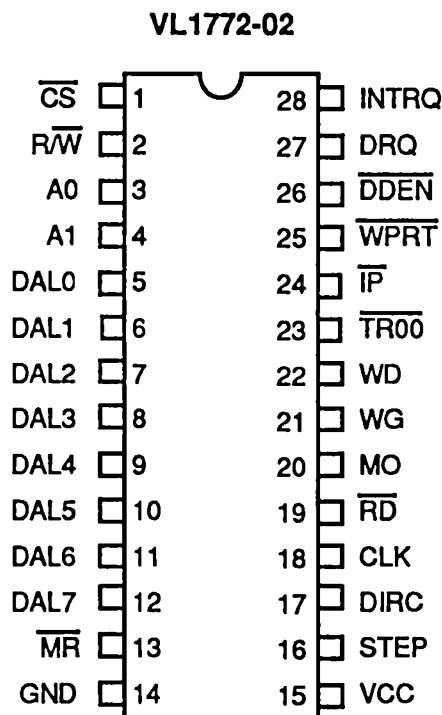
older 1770-type device. The drive side of the interface needs no additional logic except for buffers/receivers. Designed for single- or double-density operation, the device contains a programmable Motor On signal.

The VL1772-02 is implemented in NMOS silicon-gate technology and is available in a 28-pin dual in-line package. It is a low-cost version of the WD179X Floppy Disk Controller/Formatter and is compatible with generic 179X types. It also has a built-in digital data separator and write precompensation circuits. A single read (RD) line (pin 19) is the only input required to recover serial FM or MFM data from the disk drive. The device has been specifically designed for control of floppy disk drives

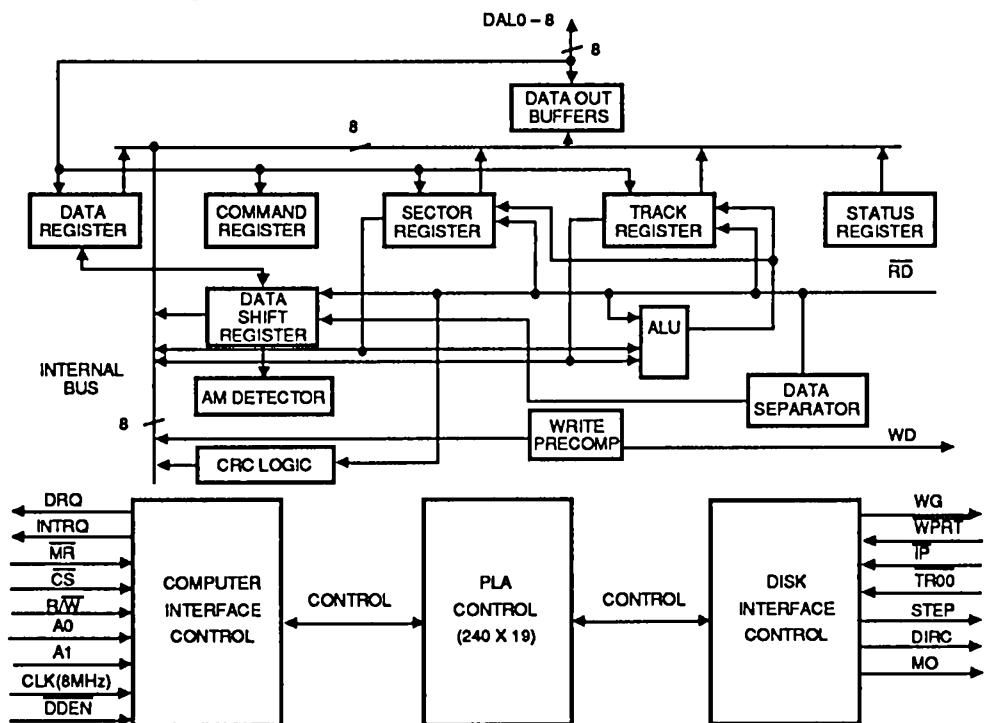
with data rates of 125K bps (single density) and 250K bps (double density). In addition, it can write a precompensation that is 125 ns from nominal, and can be enabled at any point through simple software commands. Another programmable feature, Motor On, has been incorporated to automatically enable the spindle motor prior to operating a selected drive. The VL1772-02 offers stepping rates of 2, 3, 6, and 12 ms.

The processor interface consists of an 8-bit bidirectional bus for transfer of the status information, data, and commands. All host communication with the drive occurs through these data lines. They are capable of driving one standard TTL load or three LS loads.

PIN DIAGRAM



BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Package
VL1772-02PC	Plastic DIP
VL1772-02QC	Plastic Leaded Chip Carrier (PLCC)
VL1772-02CC	Ceramic DIP

Note: Operating temperature range is 0°C to +70°C.

**SIGNAL
DESCRIPTIONS**

Signal Name	Pin Number	Signal Description																									
\overline{CS}	1	Chip Select - A logic low on this input selects the chip and enables host communication with the device.																									
R/\overline{W}	2	Read/Write - A logic high on this input controls the placement of data on the $\overline{D0-D7}$ lines from a selected register, while a logic low causes a write operation to a selected register.																									
A0, A1	3, 4	Address 0, 1 - These two inputs select a register to read or write data: <table><tr><th>\overline{CS}</th><th>A1</th><th>A0</th><th>$R/\overline{W} = 1$</th><th>$R/\overline{W} = 0$</th></tr><tr><td>0</td><td>0</td><td>0</td><td>Status Register</td><td>Command Register</td></tr><tr><td>0</td><td>0</td><td>1</td><td>Track Register</td><td>Track Register</td></tr><tr><td>0</td><td>1</td><td>0</td><td>Sector Register</td><td>Sector Register</td></tr><tr><td>0</td><td>1</td><td>1</td><td>Data Register</td><td>Data Register</td></tr></table>	\overline{CS}	A1	A0	$R/\overline{W} = 1$	$R/\overline{W} = 0$	0	0	0	Status Register	Command Register	0	0	1	Track Register	Track Register	0	1	0	Sector Register	Sector Register	0	1	1	Data Register	Data Register
\overline{CS}	A1	A0	$R/\overline{W} = 1$	$R/\overline{W} = 0$																							
0	0	0	Status Register	Command Register																							
0	0	1	Track Register	Track Register																							
0	1	0	Sector Register	Sector Register																							
0	1	1	Data Register	Data Register																							
DAL0 - DAL7	5 - 12	Data Access Lines 0 through 7 - Eight-bit bidirectional bus used for transfer of data, control, or status. This bus is enabled by \overline{CS} and R/\overline{W} . Each line drives one TTL load.																									
\overline{MR}	13	Master Reset - A logic low pulse on this line resets the device and initializes the status register (internal pull-up).																									
GND	14	Ground - Ground																									
VCC	15	Power Supply - +5 V $\pm 5\%$ power supply input.																									
STEP	16	Step - The Step output contains a pulse for each step of the drive's R/\overline{W} head. This is a pulse to the disk drive.																									
DIRC	17	Direction - The Direction output is high when stepping in towards the center of the diskette, and low when stepping out.																									
CLK	18	Clock - This input requires a free-running 50% duty cycle clock (for internal timing) at 8 MHz $\pm 1\%$.																									
\overline{RD}	19	Read Data - This active-low input is the raw data line containing both clock and data pulses from the drive.																									
MO	20	Motor On - Active high output used to enable the spindle motor prior to read, write, or stepping operations.																									
WG	21	Write Gate - This output is made valid prior to writing on the diskette.																									
WD	22	Write Data - FM or MFM clock and data pulses are placed on this line to be written on the diskette.																									
$\overline{TR00}$	23	Track 00 - This active-low input informs the VL1772-02 that the drive's R/\overline{W} heads are positioned over Track zero (internal pull-up).																									
\overline{IP}	24	Index Pulse - This active-low input informs the VL1772-02 when the physical index hole has been encountered on the diskette (internal pull-up).																									
\overline{WPRT}	25	Write Protect - This input is sampled whenever a Write Command is received. A logic low on this line prevents any Write Command from executing (internal pull-up).																									
\overline{DDEN}	26	Double Density <u>Enable</u> - This input pin selects either single (FM) or double (MFM) density. When $\overline{DDEN} = 0$, double density is selected (internal pull-up).																									
DRQ	27	Data Request - This active-high output indicates that the Data Register is full (on a Read) or empty (on a Write) operation.																									
INTRQ	28	Interrupt Request - This active-high output is set at the completion of any command or a read of the Status Register.																									

ARCHITECTURE

The VL1772-02 Floppy Disk Controller/Formatter block diagram is illustrated on the front page. The primary sections include the parallel processor interface and the floppy disk interface.

Data Shift Register - This 8-bit register assembles serial data from the Read Data input (\overline{RD}) during read operations and transfers serial data to the Write Data output during write operations.

Data Register - This 8-bit register is used as a holding register during disk read and write operations. In disk read operations, the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In disk write operations, information is transferred in parallel from the Data Register to the Data Shift Register.

When executing the Seek command, the Data Register holds the address of the desired track position. This register is loaded from the Data Access Lines (DAL) and gated onto the DAL under processor control.

Track Register - This 8-bit register holds the track number of the current read/write head position. It is incremented by one every time the head is stepped in and decremented by one every time the head is stepped out (towards Track 00). The contents of the register are com-

pared with the recorded track number in the ID field during disk read, write, and verify operations. The Track Register can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

Sector Register (SR) - This 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk read or write operations. The Sector Register contents can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

Command Register (CR) - This 8-bit register holds the command presently being executed. This register should not be loaded when the device is busy, unless the new command is a forced interrupt. The Command Register can be loaded from the DAL but not read onto the DAL.

Status Register (STR) - This 8-bit register holds device status information. The meaning of the status bits is a function of the type of command previously executed. This register can be read onto the DAL but not loaded from the DAL.

CRC Logic - This logic is used to check or to generate the 16-bit cyclic redun-

dancy check (CRC). The polynomial is:

$$G(x) = x^{16} + x^{12} + x^5 + 1$$

The CRC includes all information starting with the address mark and up to the CRC characters. The CRC register is preset to ones prior to data being shifted through the circuit.

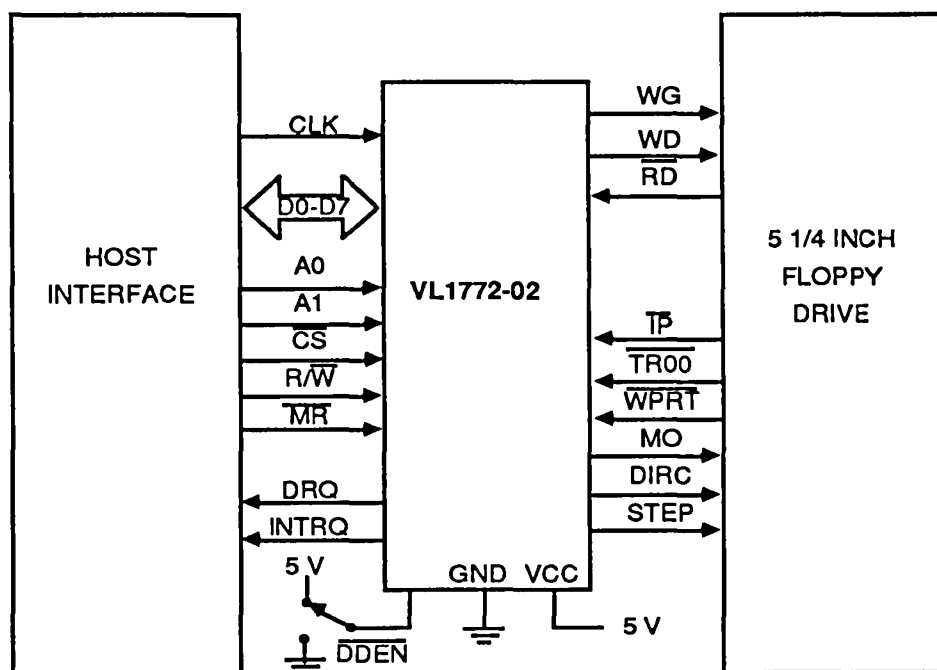
Arithmetic/Logic Unit (ALU) - The ALU is a serial comparator, incrementer, and decremter and is used for register modification and comparisons with the disk-recorded ID field.

Timing and Control - All computer and floppy disk interface controls are generated through this logic. The internal device timing is generated from an external crystal clock. The VL1772-02 has two different modes of operation according to the state of \overline{DDEN} : When $\overline{DDEN} = 0$, double density (MFM) is enabled. When $\overline{DDEN} = 1$, single density is enabled.

Address Mark Detector - The AM detector detects ID, data, and index address marks during read and write operations.

Data Separator - A digital data separator, consisting of a ring shift register and data window detection logic, provides read data and a recovery clock to the AM detector.

FIGURE 1. SYSTEM BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

PROCESSOR INTERFACE

The interface to the processor is accomplished through the eight data access lines (DALs) and associated control signals. The DALs are used to transfer data, status, and control words out of, or into the VL1772-02. The DALs are three-state buffers that are enabled as output drivers when Chip Select (\overline{CS}) = 0 and R/\overline{W} = 1 are active, or act as input receivers when \overline{CS} and R/\overline{W} = 0 are active.

When transfer of data with the Floppy Disk Controller is required by the host processor, the device address is decoded and \overline{CS} is made low. The address bits A1 and A0, combined with the signal R/\overline{W} during a read or write operation, are interpreted as selecting the following registers:

A1 - A0	READ (R/\overline{W} = 1)	WRITE (R/\overline{W} = 0)
0 0	Status Register	Command Register
0 1	Track Register	Track Register
1 0	Sector Register	Sector Register
1 1	Data Register	Data Register

After any register is written to, the same register cannot be read from until 16 μ s in MFM or 32 μ s in FM have elapsed.

During direct memory access (DMA) types of data transfers between the Data Register of the VL1772-02 and the processor, the Data Request (DRQ) output is used in data transfer control. This signal also appears as status bit 1 during read and write operations.

On disk read operations, the Data Request is activated (set high) when an assembled serial input byte is transferred in parallel to the Data Register. This bit is cleared when the Data Register is read by the processor. If the Data Register is read after one or more characters are lost, by having new data transferred into the register prior to processor readout, the Lost Data bit is set in the Status Register. The read operation continues until the end of

sector is reached.

On disk write operations, the Data Request is activated when the Data Register transfers its contents to the Data Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor. If new data is not loaded at the time the next serial byte is required by the floppy disk, a byte of zeros is written on the diskette and the Lost Data bit is set in the Status Register.

At the completion of every command an INTRQ is generated; it is reset by either reading the status register or by loading the command register with a new command. In addition, INTRQ is generated if a Force Interrupt command condition is met.

The VL1772-02 has two modes of operation, according to the state of \overline{DDEN} . When \overline{DDEN} = 1, single density is selected. In either case, the CLK input is at 8 MHz.

GENERAL DISK READ OPERATIONS

Sector lengths of 128, 256, 512, or 1024 bytes are obtainable in either FM or MFM formats. For FM, \overline{DDEN} should be placed to logical "1". For MFM formats, \overline{DDEN} should be placed to a logical "0".

Sector lengths are determined at format time by the fourth byte in the "ID" field.

SECTOR LENGTH TABLE	
SECTOR LENGTH FIELD (HEX)	NUMBER OF BYTES IN SECTOR (DECIMAL)
00	128
01	256
02	512
03	1024

There are from 0 to 244 sectors per track for the VL1772-02, and from 0 to 244 tracks.

GENERAL DISK WRITE OPERATION

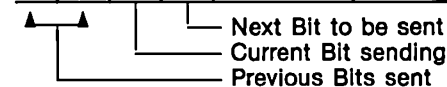
When writing is to take place on the disk the Write Gate (WG) output is activated, allowing current to flow into the read/write head. As a precaution to erroneous writing, the first data byte must be loaded into the Data Register in response to a Data Request from the device before the Write Gate signal can be activated.

Writing is inhibited when the Write Protect input is a logic low, in which case any Write command is immediately terminated, an interrupt is generated, and the Write Protect status bit is set.

For write operations, the VL1772-02 provides Write Gate to enable a write condition, and Write Data which consists of a series of active-high pulses. These pulses contain both clock and data information in FM and MFM. Write Data provides the unique missing clock patterns for recording address marks.

The Precompensation Enable bit in Write commands allow automatic write precompensation to take place. The outgoing write data stream is delayed or advanced from nominal by 187ns according to the following table:

PATTERN				MFM	FM
X	1	1	0	Early	N/A
X	0	1	1	Late	N/A
0	0	0	1	Early	N/A
1	0	0	0	Late	N/A



Precompensation is typically enabled on the innermost tracks where bit shifts usually occur and bit density is at its maximum.

COMMANDS

The VL1772-02 accepts eleven commands. Command words should only be loaded in the Command Register when the Busy Status Bit is off (Status Bit 0). The one exception is the Force Interrupt command. Whenever a command is being executed, the Busy Status Bit is set. When a command is completed, an interrupt is generated and the Busy status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault-free. For ease of discussion, commands are divided into four types and are summarized in Table 1.

The Type I Commands (see Figure 2) include the Restore, Seek, Step, Step-in, and Step-out commands. Each of the Type I Commands contains a rate field (r_0, r_1), which determines the stepping motor rate.

A 4 μ s (MFM) or 8 μ s (FM) pulse is provided as an output to the drive. For every step pulse issued, the drive moves one track location in a direction deter-

mined by the direction output. The chip will step the drive in the same direction it last stepped unless the command changes the direction.

The Direction signal is active-high when stepping in and low when stepping out. The Direction signal is valid 24 μ s before the first stepping pulse is generated.

After the last directional step, an additional 30 ms of head settling time takes place if the Verify flag is set in Type I commands. There is also a 30 ms head settling time if the E flag is set in any Type II or III command.

When a Seek, Step, or Restore command is executed, an optional verification of read/write head position can be performed by setting bit 2 ($V = 1$) in the command word to logic 1. The verification operation begins at the end of the 30 ms settling time after the head is loaded against the media. The track number from the first encountered ID Field is compared against the contents of the Track Register. If the track numbers compare and the ID Field cyclic

redundancy check (CRC) is correct, the verify operation is complete and an INTRQ is generated with no errors. If there is a match but not a valid CRC, the CRC Error Status Bit is set (Status Bit 3), and the next encountered ID field is read from the disk for the verification operation.

The VL1772-02 must find an ID field with correct track number and correct CRC within five revolutions of the media, otherwise, the seek error is set and an INTRQ is generated. If $V = 0$, no verification is performed.

All commands, except the Force Interrupt command, may be programmed via the h Flag to delay for spindle motor start up time. If the h Flag is not set and the Motor On line is low when a command is received, the VL1772-02 will force Motor On to a logic 1 and waits six revolutions before executing the command. At 300 RPM, this guarantees a one-second spindle start-up time. If, after finishing the

TABLE 1. COMMAND SUMMARY

TYPE	COMMAND	BITS							
		7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	u	h	V	r_1	r_0
I	Step-In	0	1	0	u	h	V	r_1	r_0
I	Step-out	0	1	1	u	h	V	r_1	r_0
II	Read Sector	1	0	0	m	h	E	0	0
II	Write Sector	1	0	1	m	h	E	P	a_0
III	Read Address	1	1	0	0	h	E	0	0
III	Read Track	1	1	1	0	h	E	0	0
III	Write Track	1	1	1	1	h	E	P	0
IV	Force Interrupt	1	1	0	1	l_3	l_2	l_1	l_0

FLAG SUMMARY

TYPE I COMMANDS

h = Motor On Flag (Bit 3)

h = 0, Enable Spin-up Sequence
h = 1, Disable Spin-up Sequence

V = Verify Flag (Bit 2)

V = 0, No Verify
V = 1, Verify on Destination Track

r_1, r_0 = Stepping Rate (Bits 1,0)

r_1	r_0	1772-02
0	0	6 ms
0	1	12 ms
1	0	2 ms
1	1	3 ms

u = Update Flag (Bit 4)

u = 0, No Update
u = 1, Update Track Register

TYPE II & III COMMANDS

m = Multiple Sector Flag (Bit 4)

m = 0, Single Sector
m = 1, Multiple Sector

H = Motor On Flag (Bit 3)

H = 0, Enable Spin Up Sequence
H = 1, Disable Spin Up Sequence

a_0 = Data Address Mark (Bit 0)

a_0 = Write Normal Data Mark
 a_0 = 1, Write Deleted Data Mark

E = 15ms Settling Delay (Bit 2)

E = 0, No Delay
E = 1, Add 15ms Delay

P = Write Precompensation (Bit 1)

P = 0, Enable Write Precomp
P = 1, Disable Write Precomp

TYPE IV COMMANDS

l_3-l_0 Interrupt Condition (Bits 3-0)

l_0 = 1, Not Used

l_1 = 1, Not Used

l_2 = 1, Interrupt on Index Pulse

l_3 = 1, Immediate Interrupt

l_3-l_0 = 0, Terminate without interrupt

command, the device remains idle for ten revolutions, the Motor On line goes back to a logic 0. If a command is issued while Motor On is high, the command executes immediately, defeating the six-revolution start up. This feature allows consecutive read or write commands without waiting for each motor start-up; the VL1772-02 assumes the spindle motor is up to speed.

RESTORE (SEEK TRACK 0)
Upon receipt of this command, the Track 00 (TR00) input is sampled. If TR00 is active-low indicating the read/write head is positioned over Track 00, the Track Register is loaded with zeros and an interrupt is generated. If TR00 is not active-low, stepping pulses (pin 16) at a rate specified by the r1, r0 field are issued until the TR00 input is activated.

At this time, the Track Register is loaded with zeros and an interrupt is generated. If the TR00 input does not go active-low after 255 stepping pulses, the VL1772-02 terminates operation, interrupts, and sets the Seek Error Status Bit, providing the V flag is set. A verification operation also takes place if the V flag is set. The h bit allows the Motor On option at the start of command.

FIGURE 2. TYPE I COMMAND FLOWCHART

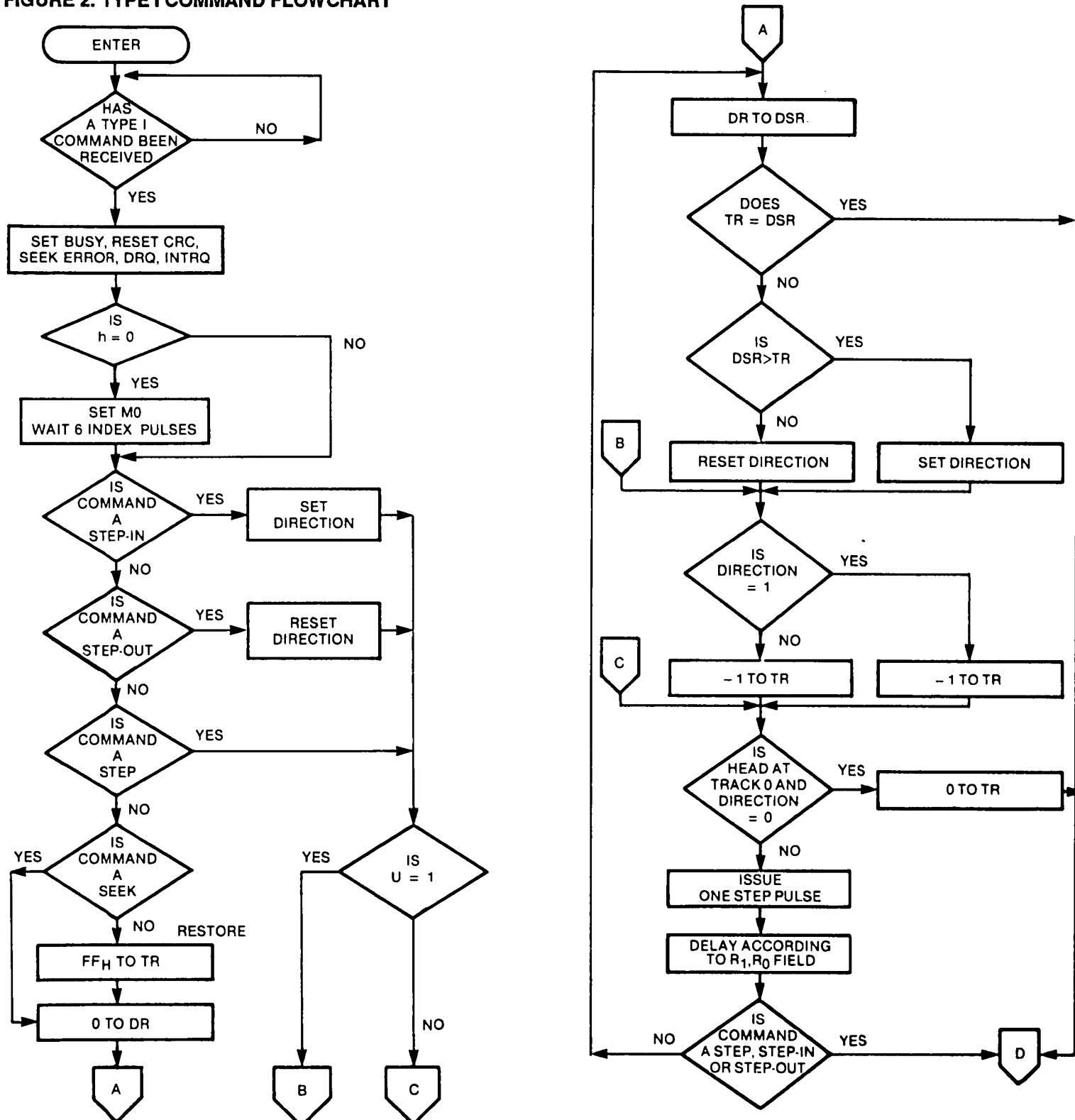


FIGURE 2. TYPE I COMMAND FLOWCHART (Cont.)

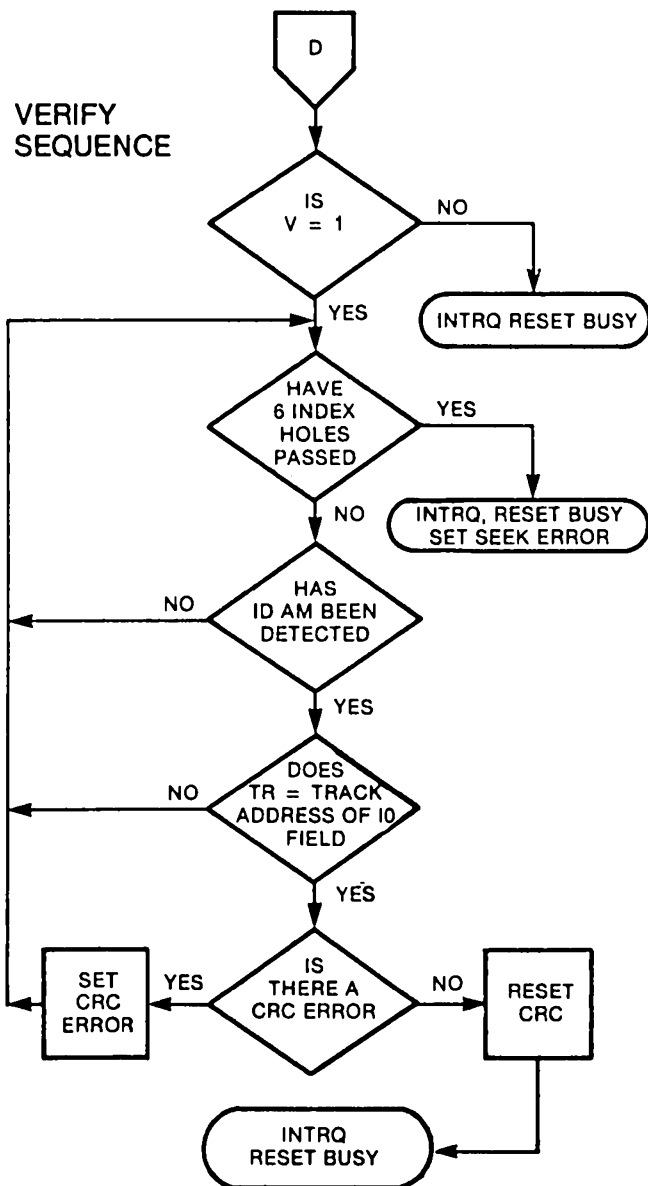
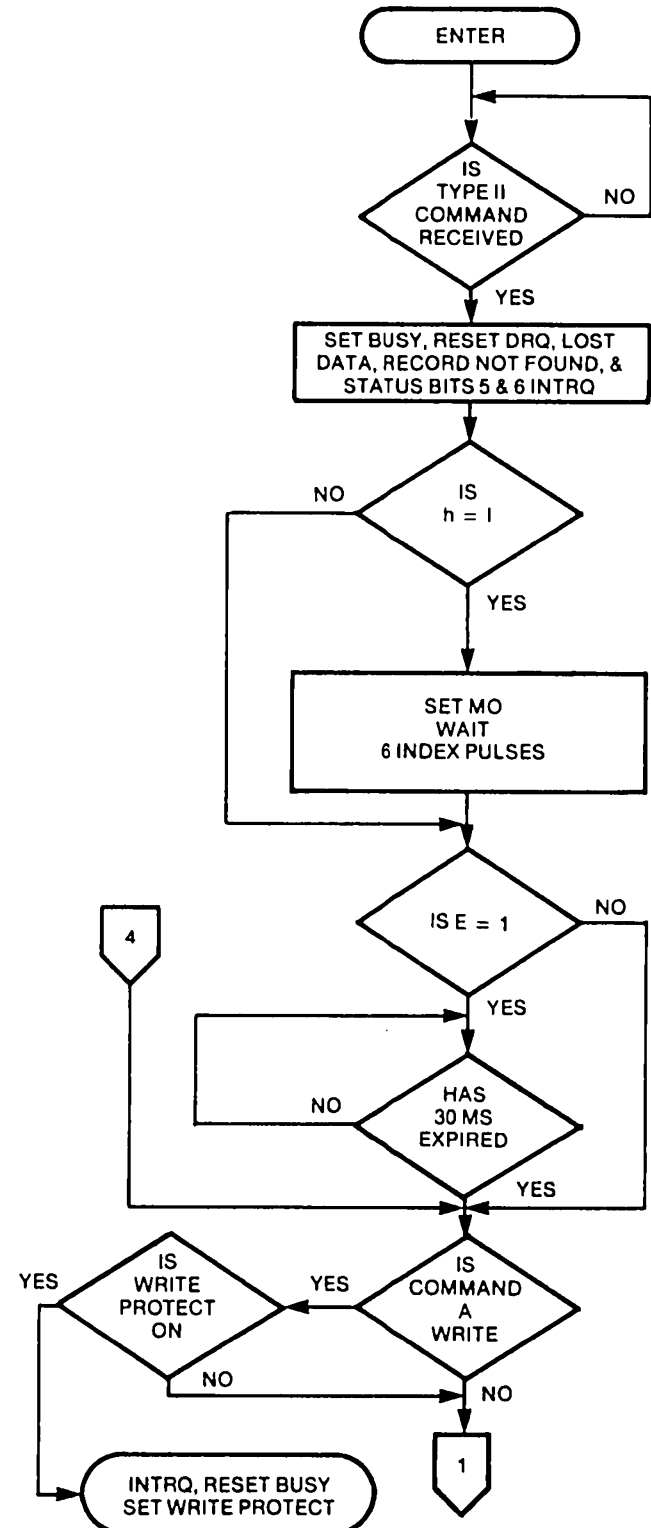


FIGURE 3. TYPE II COMMAND FLOWCHART



SEEK

This command assumes that the Track Register contains the track number of the current position of the read/write head and the Data Register contains the desired track number. The VL1772-02 will update the Track Register and issue stepping pulses in the appropriate direction until the contents of the Track Register are equal to the contents of the Data Register (the desired track location). A verification operation takes place if the V flag is on. The h bit allows the Motor On option at the start of the command. An interrupt is generated at the completion of the command. (Note: When using multiple drives, the track register must be updated for the drive selected before seeks are issued.)

STEP

Upon receipt of this command, the VL1772-02 issues one stepping pulse to the disk drive. The stepping motor direction is the same as in the previous step command. After a delay determined by the r1, r0 field, a verification takes place if the V flag is on. If the U flag is on, the Track Register is updated. The h bit allows the Motor On option at the start of the command. An interrupt is generated at the completion of the command.

STEP-IN

Upon receipt of this command, the VL1772-02 issues one stepping pulse in the direction towards track 76. If the U flag is on, the Track Register is incremented by one. After a delay is determined by the r1, r0 field, a verification takes place if the V flag is on. The h bit allows the Motor On option at the start of the command. An interrupt is generated at the completion of the command.

STEP-OUT

Upon receipt of this command, the VL1772-02 issues one stepping pulse in the direction towards track 0. If the U flag is on, the Track Register is decremented by one. After a delay determined by the r1, r0 field, a verification takes place if the V flag is on. The h bit allows the Motor On option at the start of the command. An interrupt is generated at the completion of the command.

TYPE II COMMANDS

The Type II Commands (see Figure 3)

are the Read Sector and Write Sector commands. Prior to loading the Type II Command into the Command Register, the computer must load the Sector Register with the desired sector number. Upon receipt of the Type II command, the busy status bit is set. If the E flag = 1, the command executes after a 15 ms delay.

When an ID field is located on the disk, the VL1772-02 compares the track number on the ID field with the Track Register. If there is not a match, the next encountered ID field is read and a comparison is again made. If there was a match, the sector number of the ID field is compared with the Sector Register. If there is not a sector match, the next encountered ID field is read off the disk and comparisons again made. If the ID field CRC is correct, the data field is then located and is either written into or read from depending upon the command. The VL1772-02 must find an ID field with a track number, sector number, and CRC within four revolutions of the disk; otherwise, the Record Not Found Status Bit is set (Status Bit 4) and the command is terminated with an interrupt (INTRQ).

Each of the Type II Commands contains an m flag that determines if multiple records (sectors) are to be read or written, depending upon the command. If m = 0, a single sector is read or written and an interrupt is generated at the completion of the command. If m = 1, multiple records are read or written with the sector register internally updated so that an address verification can occur on the next record. The VL1772-02 continues to read or write multiple records and update the sector register in numerical ascending sequence until the sector register exceeds the number of sectors on the track or until the Force Interrupt command is loaded into the Command Register, which terminates the command and generates an interrupt.

For example: if the VL1772-02 is instructed to read sector 27 and there are only 26 sectors on the track, the sector register exceeds the number available. The VL1772-02 will search for five disk revolutions, interrupt out, reset busy, and set the Record Not Found Status Bit.

READ SECTOR

Upon receipt of the Read Sector command, the Busy status bit is set, and when an ID field is encountered that has the correct track number, correct sector number, and correct CRC, the data field is presented to the computer. The data address mark (DAM) of the data field must be found within 30 bytes in single density and 43 bytes in double density of the last ID field CRC byte; if not, the ID field is searched for and verified again followed by the data address mark search. If, after five revolutions the DAM cannot be found, the Record Not Found Status Bit is set and the operation is terminated. When the first character or byte of the data field has been shifted through the DSR, it is transferred to the DR, and DRQ is generated. If the computer has not read the previous contents of the DR before a new character is transferred, that character is lost and the Lost Data Status bit is set. This sequence continues until the complete data field has been input to the computer. If there is a CRC error at the end of the data field, the CRC Error Status Bit is set, and the command is terminated (even if it is a multiple record command).

At the end of the read operation, the type of data address mark encountered in the data field is recorded in the Status Register (Bit 5) as shown:

STATUS BIT 5	
1	Deleted Data Mark
0	Data Mark

WRITE SECTOR

Upon receipt of the Write Sector command, the Busy status bit is set. When an ID field is encountered that has the correct track number, correct sector number, and correct CRC, a DRQ is generated. The VL1772-02 counts off 11 bytes in single density and 22 bytes in double density from the CRC field and the Write Gate (WG) output is made active if the DRQ is serviced (i.e., the DR has been loaded by the computer). If DRQ has not been serviced, the command is terminated and the Lost Data status bit is set. If the DRQ has been serviced, the WG is made active and six bytes of zeros in single density and 12 bytes in double density are then written on the disk. At this time, the data

FIGURE 3. TYPE II COMMAND FLOWCHART (Cont.)

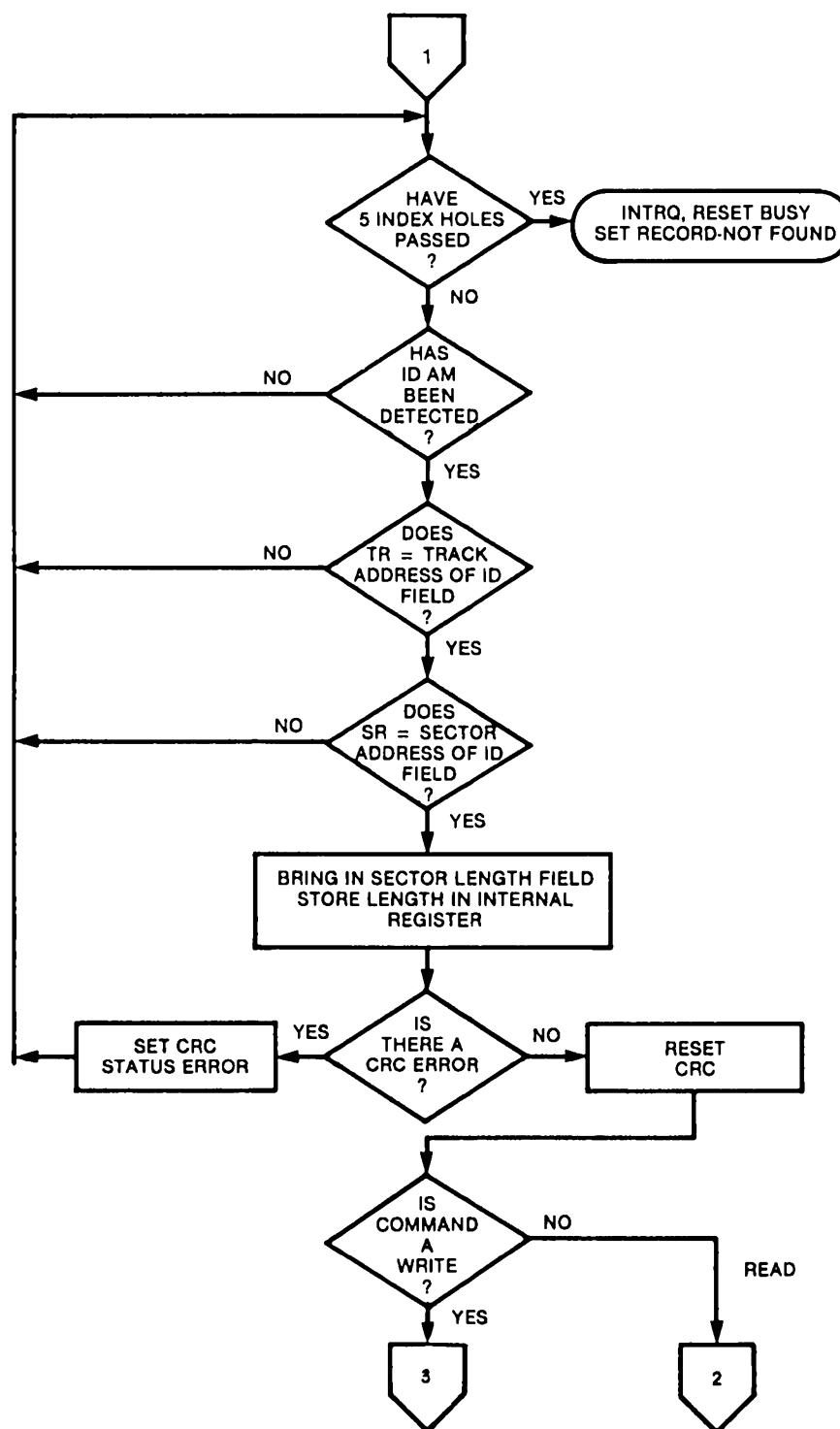


FIGURE 3. TYPE II COMMAND FLOWCHART (Cont.)

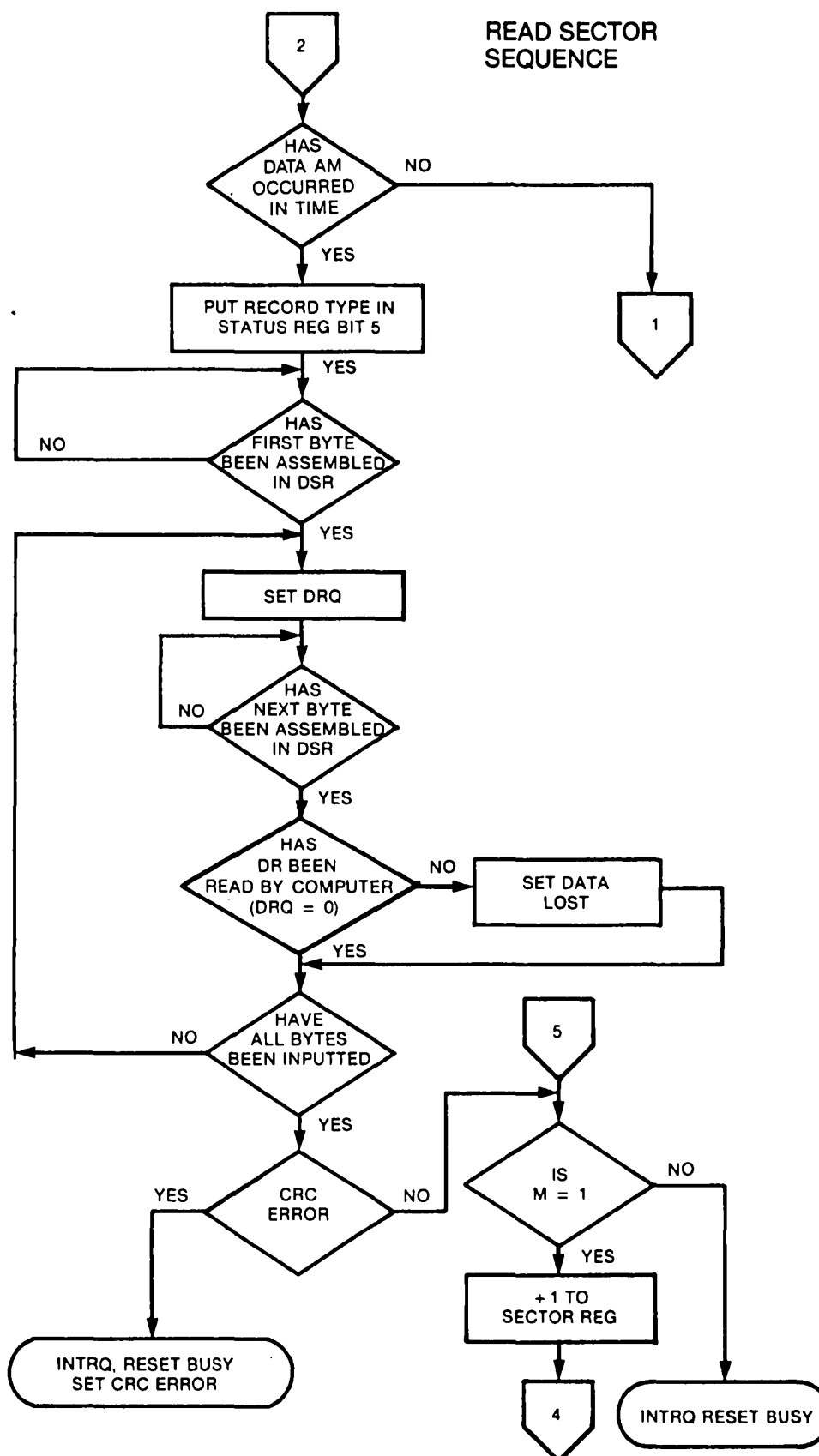
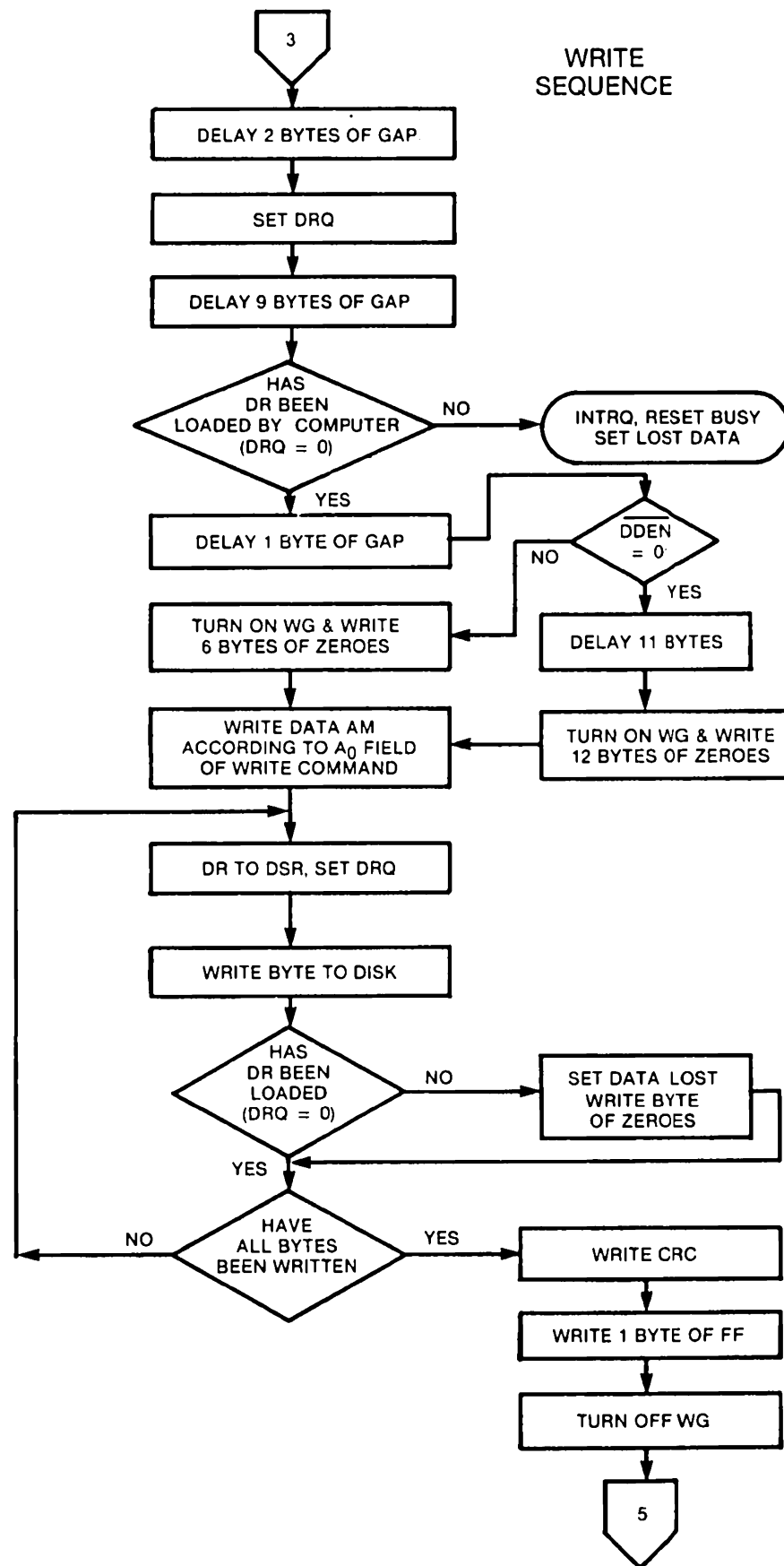


FIGURE 3. TYPE II COMMAND FLOWCHART (Cont.)





address mark is then written on the disk as determined by the a0 field of the command as shown below:

a ₀	DATA ADDRESS MARK (BIT 0)
1	Deleted Data Mark
0	Data Mark

The VL1772-02 then writes the data field and generates DRQs to the computer. If the DRQ is not serviced in time for continuous writing, the Lost Data Status Bit is set and a byte of zeros is written on the disk. The command is not terminated. After the last data byte has been written on the disk, the two-byte CRC is computed internally and written on the disk followed by one byte of logic ones in FM or in FMF. The WG output is then deactivated. INTRQ will set 24 μ s (MFM) after the last CRC byte is written. For partial sector writing, the proper method is to write data and fill the balance with zeros.

TYPE III COMMANDS

Read Address - Upon receipt of the Read Address command, the Busy Status Bit is set. The next-encountered ID field is then read in from the disk, and six data bytes of the ID field are assembled and transferred to the DR, and a DRQ is generated for each byte. The six bytes of the ID field are shown below:

TRACK ADDR	SIDE NUMBER	SECTOR ADDR	SECTOR LENGTH	CRC 1	CRC 2
1	2	3	4	5	6

Although the CRC characters are transferred to the computer, the VL1772-02 checks for validity and the CRC Error Status Bit is set if there is a CRC error. The track address of the ID field is written into the Sector Register

so that a comparison can be made by the user. At the end of the operation an interrupt is generated and the Busy status is reset.

Read Track - Upon receipt of the READ track command, the head is loaded and the Busy status bit is set. Reading starts with the leading edge of the first encountered index pulse and continues until the next index pulse. All gap, header, and data bytes are assembled and transferred to the Data Register and DRQs are generated for each byte. The accumulation of bytes is synchronized to each address mark encountered. An interrupt is generated at the completion of the command.

This command has several characteristics that make it suitable for diagnostic purposes. They are: no CRC checking is performed; gap information is included in the data stream; and the address mark detector is on for the duration of the command. Because the AM detector is always on, write splices or noise may cause the chip to look for an AM.

The ID AM, ID Field, ID CRC Bytes, DAM, Data and Data CRC Bytes for each sector will be correct. The Gap Bytes may be read incorrectly during write-splice time because of synchronization.

the \overline{RW} head over the desired track number and issuing the Write Track command.

Upon receipt of the Write Track command, the Busy Status Bit is set. Writing starts with the leading edge of the first encountered index pulse and continues until the next index pulse, at which time the interrupt is activated. The Data Request is activated immediately upon receiving the command, but writing will not start until after the first byte has been loaded into the Data Register. If the DR has not been loaded within three byte times, the operation is terminated, making the device Not Busy, the Lost Data Status Bit is set, and the interrupt is activated. If a byte is not present in the DR when needed, a byte of zeros is substituted.

This sequence continues from one index mark to the next index mark. Normally, whatever data pattern appears in the data register is written on the disk with a normal clock pattern. However, if the VL1772-02 detects a data pattern of F5 through FE in the data register, this is interpreted as a data address mark with missing clocks or CRC generation.

The CRC generator is initialized when any data byte from F8 to FE is about to be transferred from the DR to the DSR in FM or by receipt of F5 in MFM. An F7 pattern generates two CRC characters in FM or MFM. As a consequence, the patterns F5 through FE must not appear in the gaps, data fields, or ID fields. Also, CRCs must be generated by an F7 pattern.

Disks may be formatted in IBM 3740 or System 34 formats with sector lengths of 128, 256, 512, or 1024 bytes.

WRITE TRACK FORMATTING THE DISK

Data and gap information are provided at the computer interface. Formatting the disk is accomplished by positioning

TABLE 2. DATA PATTERN DECODE

DATA PATTERN IN DR (HEX)	IN FM ($\overline{DDEN} = 1$)	IN MFM ($\overline{DDEN} = 0$)
00 thru F4	Write 00 thru F4 with CLK = FF	Write 00 thru F4, in MFM
F5	Not Allowed	Write A1* In MFM, Present CRC
F6	Not Allowed	Write C2** In MFM
F7	Generate 2 CRC bytes	Generate 2 CRC bytes
F9 thru FB	Write F8 thru FB, CLK = C7, Preset CRC	Write F8 thru FB, in MFM
FC	Write FC with CLK = D7	Write FC In MFM
FD	Write FD with CLK = FF	Write FD In MFM
FE	Write FE, CLK = C7, Preset CRC	Write FE In MFM
FF	Write FF with CLK = FF	Write FF In MFM

*Missing clock transition between bits 4 and 5.

**Missing clock transition between bits 3 and 4.

**TYPE IV COMMANDS**

The Forced Interrupt Command is generally used to terminate a multiple sector read or write command or to ensure Type I status in the status register. This command can be loaded into the command register at any time. If there is a current command under execution (Busy Status Bit set) the command is terminated and the Busy Status Bit reset.

The lower four bits of the command determine the conditional interrupt as follows:

- I0 = Don't Care
- I1 = Don't Care
- I2 = Every Index Pulse
- I3 = Immediate Interrupt

The conditional interrupt is enabled when the corresponding bit positions of the command (I3-I0) are set to a 1. Then, when the condition for interrupt is met, the INTRQ line goes high signifying that the condition specified has occurred. If I3-I0 are all set to zero (HEX D0), no interrupt occurs but any command presently under execution is immediately terminated. When using the immediate interrupt condition (I3 = 1) an interrupt immediately is generated and the current command terminated. Reading the Status or writing to the Command Register does not automatically clear the interrupt. The HEX D0 is the only command that enables the immediate interrupt (HEX D8) to clear on a subsequent load command register or read status register operation. Follow a HEX D8 with D0 command.

Wait 16 μ s (double density) or 32 μ s (single density) before issuing a new command after issuing a forced interrupt. Loading a new command sooner than this nullifies the forced interrupt.

Force Interrupt Command stops any command at the end of an internal micro instruction and generates INTRQ when the specified condition is met. Force Interrupt waits until ALU operations in progress are complete (CRC calculations, compares, etc.).

Status Register - Upon receipt of any command, except the Force Interrupt command, the Busy Status Bit is set and the rest of the status bits are updated or cleared for the new command. If the Force Interrupt Command is received

when there is a current command under execution, the Busy status bit is reset, and the rest of the status bits are unchanged. If the Force Interrupt command is received when there is not a current command under execution, the Busy Status Bit is reset and the rest of the status bits are updated or cleared. In this case, Status reflects the Type I commands.

The user has the option of reading the status register through program control or using the DRQ line with DMA or interrupt methods. When the Data Register is read the DRQ bit in the Status Register and the DRQ line are automatically reset. A write to the Data Register also causes both DRQ's to reset.

The Busy Bit in the status may be monitored with a user program to determine when a command is complete, in lieu of using the INTRQ line. When using the INTRQ, a Busy status check is not recommended because a read of the Status Register to determine the condition of busy resets the INTRQ line.

The format of the Status Register is shown below:

(BITS)							
7	6	5	4	3	2	1	0
S7	S6	S5	S4	S3	S2	S1	S0

Because of internal synchronization cycles, certain time delays are observed when operating under program I/O as shown.

Operation	Next Operation	Delay Req'd.	
		FM	MFM
Write to Command Reg.	Read Busy Bit (Status Bit 0)	48 μ sec	24 μ sec
Write to Command Reg.	Read Status Bits 1-7	64 μ sec	32 μ sec
Write Register	Read Same Register	32 μ sec	16 μ sec

RECOMMENDED - 126 BYTES/SECTOR

Shown below is the recommended single-density format with 126 bytes/sector. In order to format a diskette, the user must issue the Write Track command, and load the data register with the following values. For every byte

NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
40	FF (or 00)
6	00
1	FE (ID Address Mark)
1	Track Number
1	Side Number (00 or 01)
1	Sector Number (1 thru 1A)
1	00 (Sector Length)
1	F7 (2 CRC's written)
11	FF (or 00)
6	00
1	FB (Data Address Mark)
128	Data (IBM uses E5)
1	F7 (2 CRC's written)
10	FF (or 00)
369**	FF (or 00)

to be written, there is one Data Request.

**Continue writing until VL1772-02 interrupts out. Approximately 369 bytes.

256 BYTES/SECTOR

Shown below is the recommended dual-density format with 256 bytes/sector. In order to format a diskette the user must issue the Write Track command and load the data register with the following values. For every byte to be written, there is one data request.

NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
60	4E
12	00
3	F5 (Writes A1)
1	FE (ID Address Mark)
1	Track Number (0 thru 4C)
1	Side Number (0 or 1)
1	Sector Number (1 thru 1A)
1	01 (Sector Length)
1	F7 (2 CRC's written)
22	4E
12	00
3	F5 (Writes A1)
1	FB (Data Address Mark)
256	DATA
1	F7 (Data Address Mark)
24	4E
668**	4E

** Continue writing until VL1772-02 interrupts out. Approximately 668 bytes.

Non-Standard Formats - Variations in the recommended formats are possible to a limited extent, if the following requirements are met:

- 1) Sector size must be 126, 256, 512 or 1024 bytes.
- 2) Gap 2 cannot be varied from the recommend format.
- 3) Three bytes of A1 must be used in MFM.



In addition, the Index Address Mark is not required for operation by the VL1772-02. Gap 1, 3, and 4 lengths can be as short as two bytes for VL1772-02 operation; however, PLL lock up time, motor speed variation, write-splice area, etc. add more bytes to each gap to achieve proper operation. For highest system reliability, use the recommended format.

	FM	MFM
Gap I	16 bytes FF	32 bytes 4E
Gap II	11 bytes FF	22 bytes 4E
*	6 bytes 00	12 bytes 00
*		3 bytes A1
Gap III**	10 bytes FF	24 bytes 4E
	4 bytes 00	8 bytes 00
		3 bytes A1
Gap IV	16 bytes FF	16 bytes 4E

*Byte counts must be exact.

**Byte counts are minimum, except exactly 3 bytes of A1 must be written.

TABLE 3. STATUS REGISTER

BIT NAME	MEANING
S7 MOTOR ON	This bit reflects the status of the Motor On output.
S6 WRITE PROTECT	On Read Record: Not Used. On Read Track: Not Used. On any Write: It indicates a Write Protect. This bit is reset when updated.
S5 RECORD TYPE/SPIN-UP	When set, this bit indicates that the Motor Spin-Up sequence has completed (5 revolutions) on Type I commands. Type 2 & 3 commands, this bit indicates record Type. 0 = Data Mark. 1 = Deleted Data Mark.
S4 RECORD NOT FOUND (RNF)	When set, it indicates that the desired track, sector, or side were not found. This bit is reset when updated.
S3 CRC ERROR	If S4 is set, an error is found in one or more ID fields; otherwise it indicates error data field. This bit is reset when updated.
S2 LOST DATA/ BYTE	When set, it indicates the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated. On Type I commands, this bit reflects the status of the TR00 signal.
S1 DATA REQUEST INDEX	This bit is a copy of the DRQ output. When set, it indicates the DR is full on a Read Operation or the DR is empty on a Write operation. This bit is reset to zero when updated. On Type 1 commands, this bit indicates the status of the IP signal.
S0 BUSY	When set, command is under execution. When reset, no command is under execution.

FIGURE 4. TYPE III COMMAND WRITE TRACK FLOWCHART

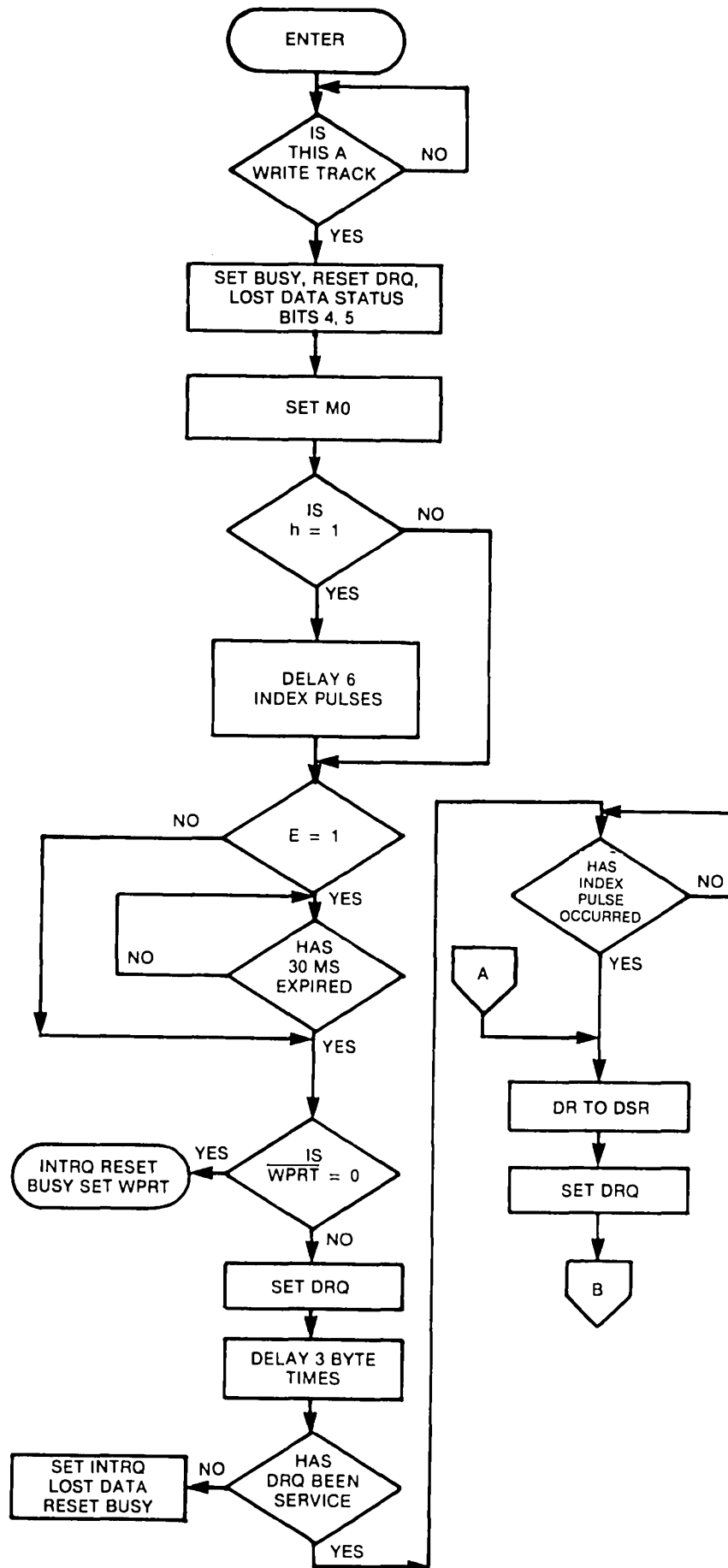


FIGURE 4. TYPE III COMMAND WRITE TRACK FLOWCHART (Cont.)

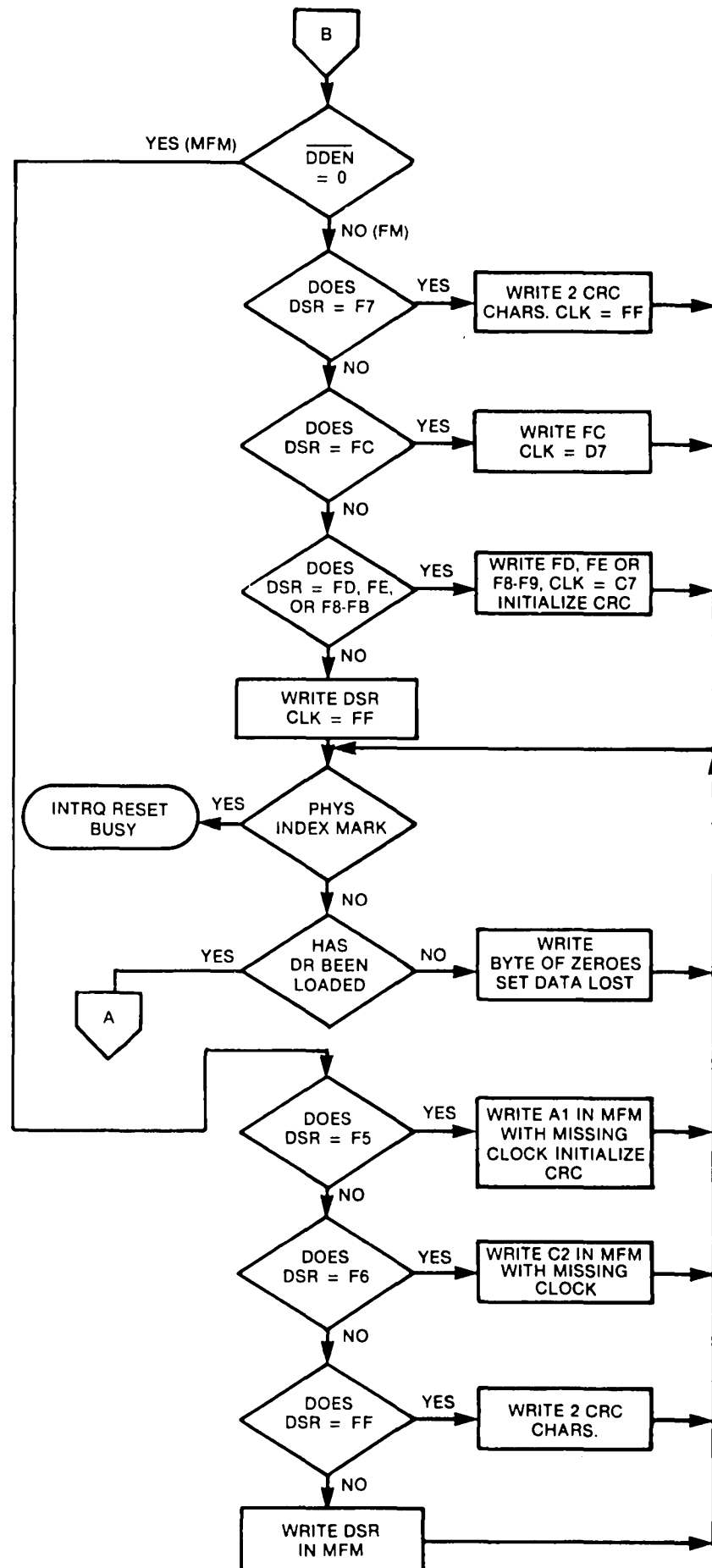


TABLE 4. READ DATA TIMING

CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
Raw Read Pulse Width	.200 .400		3 3	μsec	MFM FM
Raw Read Cycle Time	3			μsec	

TABLE 5. READ ENABLE TIMING

READ ENABLE TIMING – $\overline{\text{RE}}$ such that: $\text{R}/\overline{\text{W}} = 1$, $\text{CS} = 0$.

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
t_{RE}	$\overline{\text{RE}}$ Pulse Width of $\overline{\text{CS}}$	200			nsec	$C_L = 50 \text{ pf}$
t_{DRR}	DRQ Reset from $\overline{\text{RE}}$		200	300	nsec	
t_{DV}	Data Valid from $\overline{\text{RE}}$		100	200	nsec	$C_L = 50 \text{ pf}$
t_{DOH}	Data Hold from $\overline{\text{RE}}$	20		150	nsec	$C_L = 50 \text{ pf}$
	INTRQ Reset from $\overline{\text{RE}}$			8	μsec	

Note: Worst case service time for DRQ is 23.5 μsec for MFM and 47.5 μsec for FM.

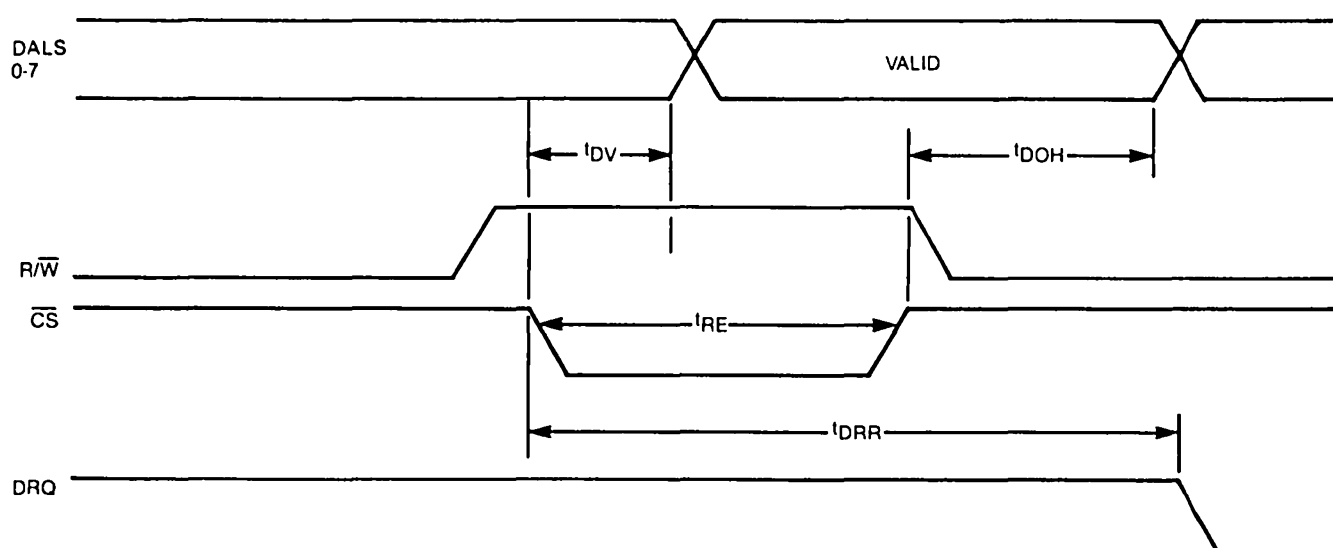
FIGURE 5. READ ENABLE TIMING


TABLE 6. WRITE ENABLE TIMING

WRITE ENABLE TIMING - \overline{WE} such that: $R/\overline{W} = 0$, $\overline{CS} = 0$.

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
t_{AS}	Setup ADDR to \overline{CS}	50			nsec	
t_{SET}	Setup R/\overline{W} to \overline{CS}	0			nsec	
t_{AH}	Hold ADDR from \overline{CS}	10			nsec	
t_{HLD}	Hold R/\overline{W} from \overline{CS}	0			nsec	
t_{WE}	\overline{WE} Pulse Width	200			nsec	
t_{DRW}	DRQ Reset from \overline{WE}		100	200	nsec	
t_{DS}	Data Setup to \overline{WE}	150			nsec	
t_{DH}	Data Hold from \overline{WE}	0			nsec	
	INTRQ Reset from \overline{WE}			8	μ sec	

FIGURE 6. WRITE ENABLE TIMING

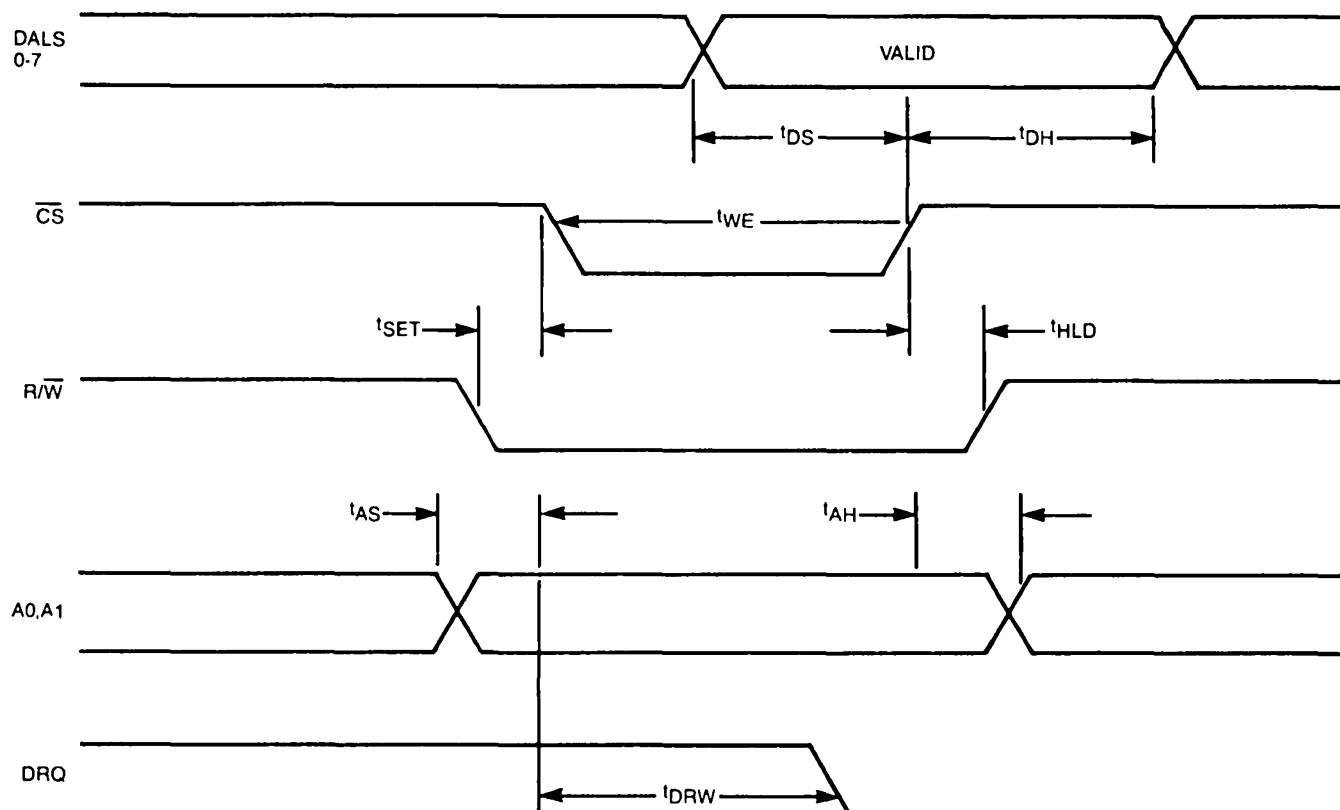


TABLE 7. WRITE DATA TIMING

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
t_{WP}	Write Gate to Write Data		4		μsec	FM
			2		μsec	MFM
	Write Data Cycle Time		4,6,8		μsec	
	Write Gate off from WD		4		μsec	FM
			2		μsec	MFM
	Write Data Pulse Width		820		nsec	Early MFM
			690		nsec	Nominal MFM
			570		nsec	Late MFM
			1.38		μsec	FM

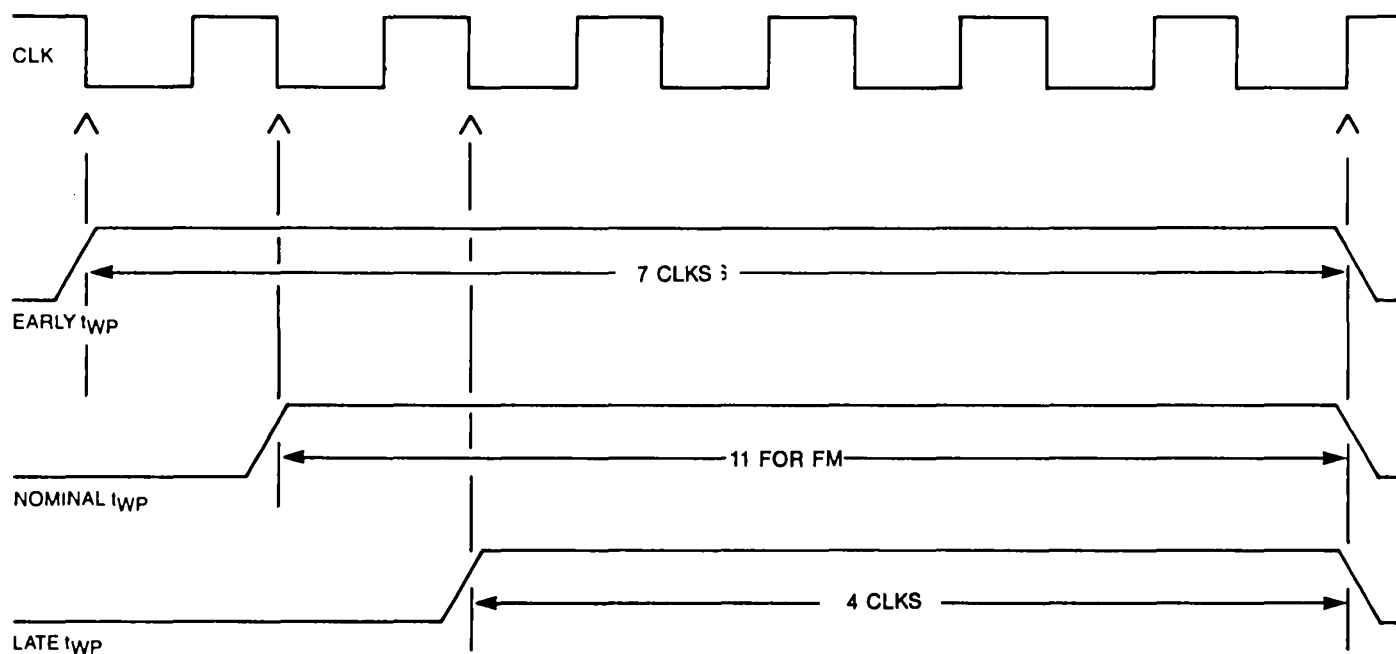
FIGURE 7. WRITE DATA TIMING


TABLE 8. MISCELLANEOUS TIMING

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
t _{CD1}	Clock Duty (low)	50	67		nsec	MFM FM MFM FM
t _{CD2}	Clock Duty (high)	50	67		nsec	
t _{STP}	Step Pulse Output		4		μsec	
			8			
t _{DIR}	Dir Setup to Step		24		μsec	
			48			
t _{MR}	Master Reset Pulse Width	50			μsec	
t _{IP}	Index Pulse Width	20			μsec	

FIGURE 8. MISCELLANEOUS TIMING

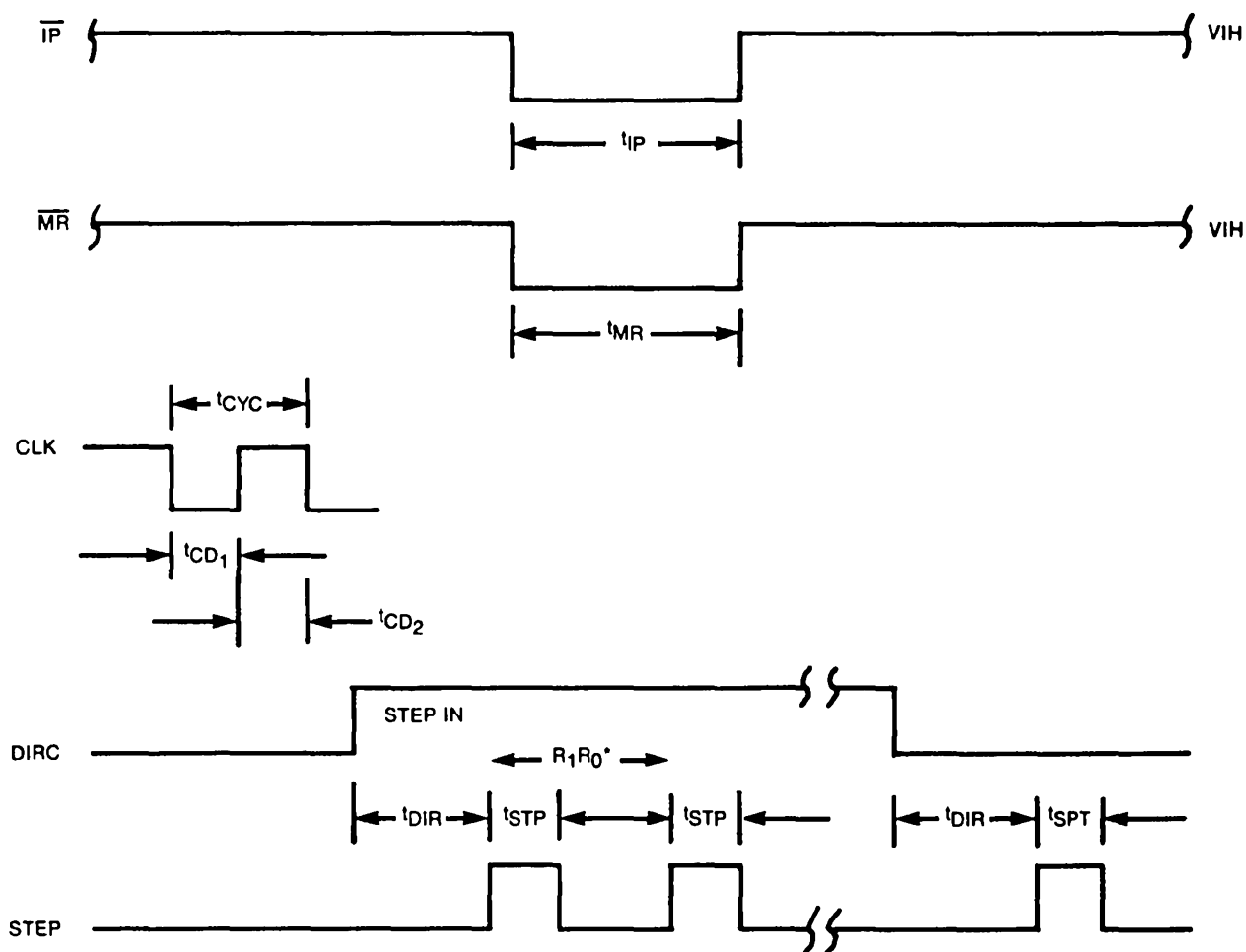
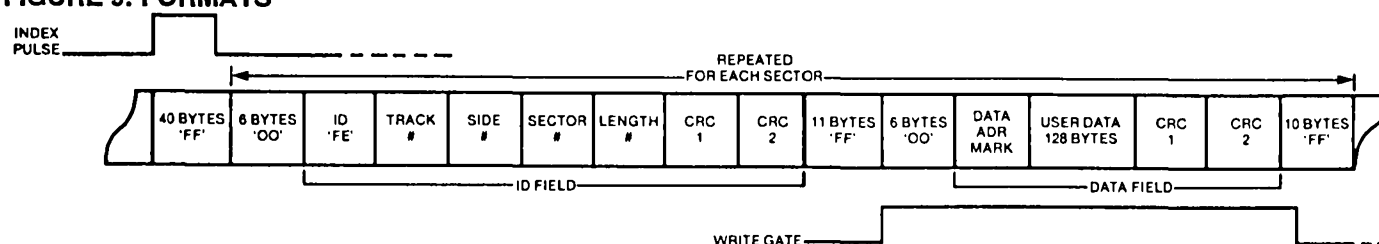
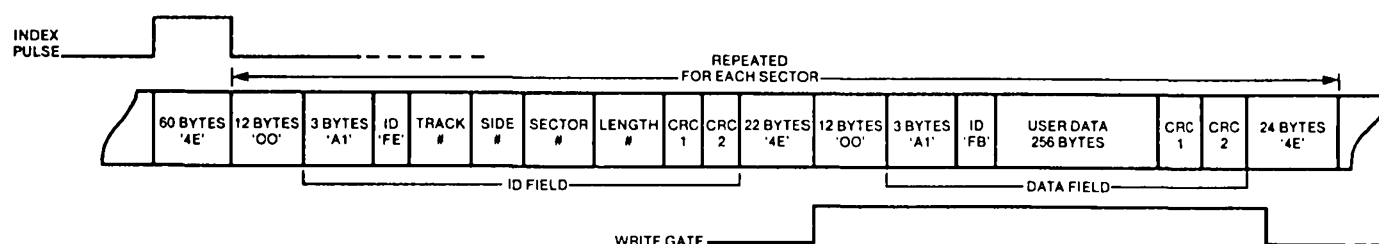


FIGURE 9. FORMATS

SINGLE DENSITY FORMAT

DOUBLE DENSITY FORMAT

ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	-10°C to +80°C
Storage Temperature	-65°C to +140°C
Supply Voltage to Ground Potential	-0.5 V to +7.0 V
Applied Output Voltage	-0.5 V to +7.0 V
Applied Input Voltage	-0.5 V to +7.0 V
Power Dissipation	800 mW

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or other conditions above those indicated in the

operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS $T_A = 0^\circ\text{C to } 70^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 5\%$

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
VOH	Output High Voltage	2.4			V	IO = -100 μA
VOL	Output Low Voltage			0.4	V	IO = 1.6 mA
VIH	Input High voltage	2.0			V	
VIL	Input Low Voltage			0.8	V	
IIL	Input Leakage Current			10	μA	VIN = VCC
IOL	Output Leakage Current			10	μA	VOU = VCC
RPU	Internal Pull-up	100		1700	μA	VIN = 0 V
ICC	Operating Supply Current		75	150	mA	
PD	Power Dissipation		780		mW	

APPLICATION INFORMATION

VL1772-02: AN IMPROVED VERSION OF THE 1770-00

The 177X family of flexible disk controllers has attracted a great deal of interest from system designers. Allowing compactness and superior performance, this family of advanced ICs has proven to be a success in the marketplace. The original 1770-00 won much approval with its 28-pin package. Its digital data separator allowed consistent operation over temperature, but more was required. The error rate of this data recovery circuit was too high, and a reliable data separator with lower error rates was seen as an important need for computer systems of all types. In addition, a small change of step rate

selections could ensure faster throughput, while maintaining compatibility with existing designs.

Thus began the design of a new concept in flexible disk controllers. An important need was to maintain compatibility with existing designs using the 1770-00, while extending the capabilities of the 177X family to include higher-performance drives. These criteria have been satisfied with the VL1772-02.

IMPROVING THE DATA SEPARATOR

The improvement of the data separator, or data recovery circuit, as it is called, is an important enhancement to the reliability of the VL1772-02. The

operation of this part of the circuit, although critical to system reliability, is simple to understand. Figure 10 shows a train of read data pulses coming from a floppy drive. The clock and data pulses are both in this signal, combined in a simple encoding format. In each bit cell, the data separator chooses a time period within which pulses are recognized as data pulses. The better the resolution for defining this window for the data pulses, the greater the jitter in the signal can be before ones and zeros are incorrectly recognized. This incorrect recognition, and the resultant soft errors, are the basic limiting factor in floppy drive error rates. The VL1772-02, with a wider data window, has a lower chance of incorrect recognition, resulting in lower error rates. This effect will be particularly evident as the user's media degrades with use and jitter increases. This increased reliability of the VL1772-02 can result in fewer returns and greater user satisfaction.

FIGURE 10. WINDOWING READ DATA

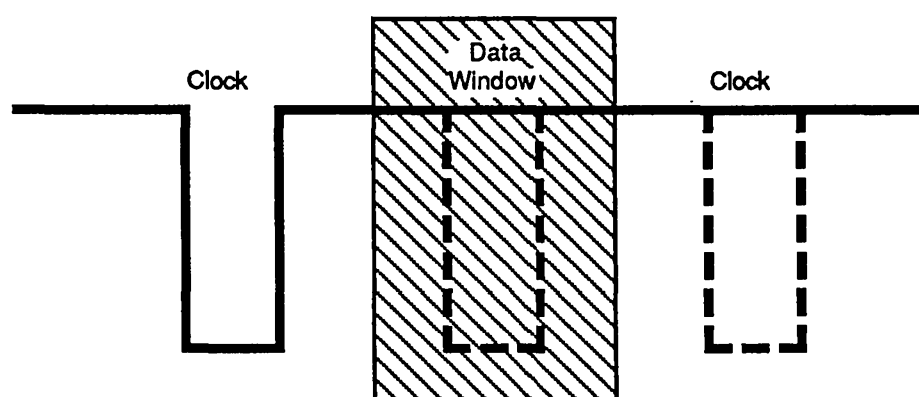


TABLE 9. STEP RATE SELECTION: 1770-00 AND VL1772-02

Step Rate Select Bits		Step Rate (ms)	
r1	r0	1770-00	VL1772-02
0	0	6	6
0	1	12	12
1	0	20	2
1	1	30	3

STEP RATES

With a different selection of step rates than the 1770-00 (see table 9), the VL1772-02 allows the use of drives with minimum settle times up to 12 ms. At the same time, performance is enhanced to take advantage of floppy drives that require only 2 or 3 ms of delay. If a design is currently using head settle times of 6 or 12 ms (as most are), no modifications are required to use the VL1772-02 in the 1770-00 socket. If the current choice of r1 and r0 calls for 20 or 30 ms of delay, use of the VL1772-02 requires:

- the selection of drives that have head settle time under 12 ms, and modified software to allow correct r1, r0 choice, or
- implementation of head settle time in hardware, with an external interrupt.

Fortunately, almost all modern flexible disk drives have head settle times well under 12 ms, and current 1770 applications have taken this into account, using 6 or 12 ms as the head settle time. Where this change is required, it will mean less waiting for the drives to finish each seek. This will certainly produce higher user satisfaction with the system, as well as appreciably higher performance against most benchmarks.

SYNCHRONOUS DATA LINE CONTROLLER

FEATURES

- HDLC, SDLC, ADCCP and CCITT X.25 Compatible
- SDLC Loop Data Link Capability
- Full or Half Duplex Operation
- DC to 2.0 Mbits/Sec Data Rate
- Programmable/Automatic FCS (CRC) Generation and Checking
- Programmable NRZI Encode/Decode
- Full Set of Modem Control Signals
- Digital Phase Locked Loop
- Fully Compatible with Most CPU's
- Error Detection: CRC, Underrun, Overrun, Aborted or Invalid Frame Errors
- Straight Forward CPU Interrupts
- Programmable Modem Control Interrupts
- Double Buffering of Data
- Variable Character Length (5, 6, 7 or 8 Bits)
- Residual Character Capability
- Address Compare

- Global Address Recognition
- Extendable Address Field
- Extendable Control Field
- Automatic Zero Insertion and Deletion
- Maintenance Mode for Self-Testing
- Pin-Compatible Replacement for WD 1933 and WD1935

DESCRIPTION

The VL1935 is a MOS/LSI microcomputer peripheral device which performs the functioning of interfacing a parallel digital system to a synchronous serial data communication channel employing ISO's HDLC, IBM's SDLC or ANSI's ADCCP line protocol. These protocols are referred to as Bit-Oriented Protocols (BOP).

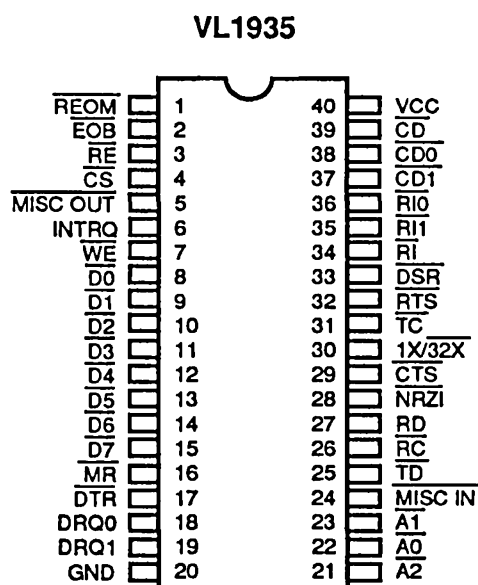
The chip is fabricated in N-channel depletion load MOS technology and is TTL compatible on all inputs and outputs. This controller requires a minimum of CPU software by supporting a comprehensive frame-level instruction set and by hardware

implementation of the low level tasks associated with frame assembly/disassembly and data integrity. It can be programmed to encode/decode NRZI data. The internal clock is then derived from the NRZI data using a digital phase locked loop.

The receiver and transmitter logic operates as two total independent sections with a minimum of common logic. The frames are automatically checked for errors during reception by verifying correct Frame Check Sequence (FCS). In transmit mode, the FCS is automatically generated by this controller and sent before the final Flag. It also continuously checks for other errors. In case of an error, the CPU is interrupted.

The controller recognizes and can generate Flag, Abort, Idle and GA characters. VL1935 can be used in an SDLC Loop configuration. An End of Block option is supplied to minimize CPU time. A full set of modem control signals are supplied to minimize external hardware.

PIN DIAGRAM



ORDER INFORMATION

Part Number	Clock Frequency	Package
VL1935-10PC	0.5 MHz	Plastic DIP
VL1935-10QC		Plastic Leaded Chip Carrier (PLCC)
VL1935-10CC		Ceramic DIP
VL1935-11PC	1.0 MHz	Plastic DIP
VL1935-11QC		Plastic Leaded Chip Carrier (PLCC)
VL1935-11CC		Ceramic DIP
VL1935-12PC	1.5 MHz	Plastic DIP
VL1935-12QC		Plastic Leaded Chip Carrier (PLCC)
VL1935-12CC		Ceramic DIP
VL1935-13PC	2.0 MHz	Plastic DIP
VL1935-13QC		Plastic Leaded Chip Carrier (PLCC)
VL1935-13CC		Ceramic DIP

Note: Operating temperature range is 0°C to +70°C.

PIN DESCRIPTION

PIN NUMBER	MNEMONIC	SIGNAL NAME	FUNCTION
1	$\overline{\text{REOM}}$	$\overline{\text{Received End of Message}}$	Received End of Message with no Errors. This output signal is the inverse of IR7, bit 7 of the Interrupt Register.
2	$\overline{\text{EOB}}$	$\overline{\text{End of Block}}$	This input, when low, function as an FCS command. Is independent of $\overline{\text{CS}}$.
3	$\overline{\text{RE}}$	$\overline{\text{Read Enable}}$	This input, when low (and $\overline{\text{CS}}$ is active), gates the content of addressed register onto the Data bus.
4	$\overline{\text{CS}}$	$\overline{\text{Chip Select}}$	This input, when low, selects the VL1935 for a read or write operation to/from the Data bus.
5	$\overline{\text{MISC OUT}}$	$\overline{\text{Misc Output}}$	This output is an extra programmable output signal for the convenience of the user. Is controlled by the CR10 bit.
6	INTRQ	Interrupt Request	This output is high whenever any of the interrupt register bits IR7-IR3 are set. $\overline{\text{TC}}$ must be asserted to assert INTRQ.
7	$\overline{\text{WE}}$	$\overline{\text{Write Enable}}$	This input when low (and $\overline{\text{CS}}$ is active), gates the content of the Data bus into the addressed register.
8 thru 15	$\overline{\text{D0-D7}}$	$\overline{\text{Data Bus}}$	Bidirectional three-state Data Bus. Bit 7 is MSB.
16	MR	Master Reset	This input, when low, initializes all the registers, and forces the VL1935 into an idle state. The VL1935 will remain idle until a command is issued by the CPU.
17	$\overline{\text{DTR}}$	$\overline{\text{Data Terminal Ready}}$	Modem Control Signal. This output, when low, indicates to the Data Communication Equipment (DCE) that the VL1935 is ready to transmit or receive data.
18	DRQO	Data Request Output	This output, when high, indicates that the Transmitter Holding Register (THR) is empty and ready to receive a data character from the Data bus for a transmit operation.
19	DRQI	Data Request Input	This output, when high, indicates that Receiver Holding Register (RHR) contains a newly received data character, available to be read onto the Data bus.
20	V _{SS}	V _{SS}	Ground
21 thru 23	$\overline{\text{A2}}, \overline{\text{A0}}, \overline{\text{A1}}$	$\overline{\text{ADDRESS}}$	These inputs are used to address the CPU interface registers for read/write operations.
24	$\overline{\text{MISC IN}}$	$\overline{\text{Misc Input}}$	This input is an extra input signal for the convenience of the user. The state is shown by the SR4 bit.
25	TD	Transmitted Data	This output transmits the serial data to the Data Communications Equipment/Channel.
26	$\overline{\text{RC}}$	$\overline{\text{Receive Clock}}$	This input is used to synchronize the received data.
27	RD	Received Data	This input receives the serial data from the Data Communication Equipment/Channel.
28	$\overline{\text{NRZI}}$	$\overline{\text{NRZI}}$	This input, when low, sets the VL1935 in NRZI mode.
29	$\overline{\text{CTS}}$	$\overline{\text{Clear to Send}}$	Modem Control Signal. This input when low, indicates that the DCE is ready to accept data from the VL1935.
30	1X/32X	DPLL Select	This input controls the internal clock. When high (1X clock), the external clock has the same frequency as the internal clock. When low (32X clock), the external clock is 32 times faster than the internal clock and the DPLL Logic is enabled.
31	$\overline{\text{TC}}$	$\overline{\text{Transmit Clock}}$	This input is used to synchronize the transmitted data, as well as generating either Receive or Transmit INTRQ's.

PIN DESCRIPTION (continued)

PIN NUMBER	MNEMONIC	SIGNAL NAME	FUNCTION
32	RTS	Request to Send	Modem Control Signal. This output, when low, indicates to the DCE that the VL1935 is ready to transmit data.
33	$\overline{\text{DSR}}$	Data Set Ready	Modem Control Signal. This input, when low, indicates that the DCE is ready to receive or transmit data.
34	$\overline{\text{RI}}$	Ring Indicator	Modem Control Signal. This input, when low, indicates a ringing signal being received on the communication channel.
35	$\overline{\text{RI1}}, \overline{\text{RI0}}$	Ring Indicator	These inputs are used to program Ring Indicator interrupts.
36		Interrupt Control	
37	$\overline{\text{CD1}}, \overline{\text{CD0}}$	Carrier Detect	These inputs are used to program Carrier Detect Interrupts.
38		Interrupt Control	
39	$\overline{\text{CD}}$	Carrier Detect	Modem Control Signal. This input, when low, indicates there is a carrier signal received by the local DCE from a distant DCE.
40	V_{CC}	V_{CC}	+5VDC

TABLE 1. VL1935 GLOSSARY

TERM	DEFINITION/DESCRIPTION
BOP	Bit-oriented protocols: SDLC, HDLC, and ADCCP
ABORT	11111111 (seven or more contiguous 1's)
GA	Go-ahead pattern. 01111111 (0(LSB) followed by seven 1's)
LSB	First transmitted bit and first received bit. (Least significant bit)
MSB	Last transmitted bit and last received bit. (Most significant bit)
IDLE	11111111 11111111 (15 or more contiguous 1's)
FLAG	01111110. Starts and ends a Frame.
A-FIELD	Address-field in the Frame. Consists of one or more 8-bit characters. Defines the address of a particular station.
C-FIELD	Control field in the Frame. Consists of one or two 8-bit characters.
I-FIELD	Information field in the Frame. Consists of any number of bits.
FCS	Frame Check Sequence. A 16-bit error checking field sequence.
FRAME	A communication element, consisting of a minimum of 32 bits, and delimited by FLAGS.
GLOBAL ADDRESS	An A-field character of eight 1's. When this is compared and matched in the Address comparator, the DRQI will be set, indicating a valid address
RESIDUAL CHARACTER	The last I-field character, consisting of a lesser amount of bits than the other I-field characters in the Frame.
DATA SET	Data Communication Equipment (DCE). May be a modem.
BIT TIME	Length in time of a serial data bit.

APPLICATIONS

COMPUTER COMMUNICATIONS

TERMINAL COMMUNICATIONS

COMPUTER TO MODEM INTERFACING

LINE CONTROLLERS

FRONT END COMMUNICATIONS

NETWORK PROCESSORS

TELECOMMUNICATION SWITCHING NETWORKS

MESSAGE SWITCHING

PACKET SWITCHING

MULTIPLEXING SYSTEMS

DATA CONCENTRATOR SYSTEMS

SDLC LOOP DATA LINK SYSTEMS

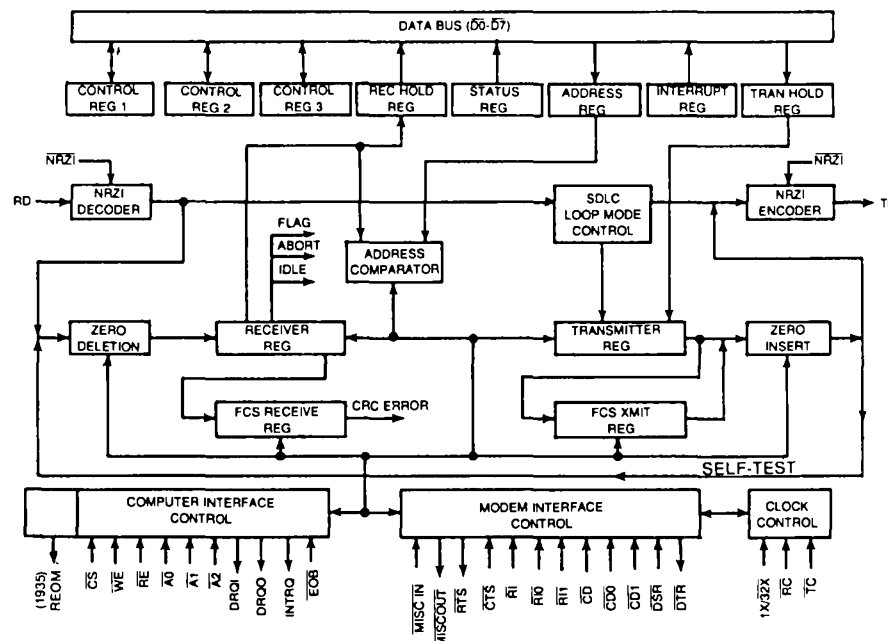
DMA APPLICATIONS

COMMUNICATION TEST EQUIPMENT

LOCAL NETWORKS

MULTIDROP LINE SYSTEMS

FIGURE 1. VL1935 BLOCK DIAGRAM



A BRIEF DESCRIPTION OF HDLC, SDLC AND ADCCP PROTOCOLS

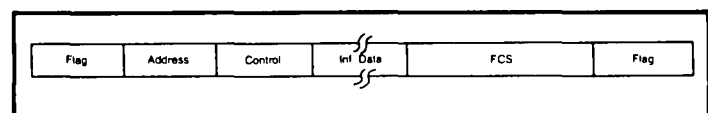
The VL1935 is compatible with HDLC, SDLC and ADCCP standard communication Link Protocols. These are bit-oriented, code independent, and ideal for full duplex communication. A single communication element is called a FRAME, which can be used for both link control and data transfer purposes.

The elements of a frame are the beginning eight bit FLAG (F) consisting of one logical "0" six 1's and a 0, an eight bit ADDRESS-FIELD(A), an eight bit CONTROL-FIELD (C), a variable (N bits) INFORMATION-FIELD, a sixteen bit FRAME-CHECK-SEQUENCE (FCS), and an eight bit end FLAG (F), having the same bit-pattern as the beginning flag.

In HDLC, the address (A) and control (C) characters are extendable (more than one character). An important characteristic of a frame is that its contents are made code transparent by use of a zero bit insertion and deletion technique. Thus, the user can adapt any format or code suitable for his system. The frame is bit-oriented, meaning that, bits not

characters in each field have specific meanings. The Frame Check Sequence (FCS) is an error detection scheme similar to the Cyclic Redundancy Checkword (CRC) widely used in magnetic disk storage devices. The frame format is shown in Figure 3.

FIGURE 3. VL1935 SDLC/HDLC/ADCCP FRAME FORMAT



Where:

FLAG = 01111110

Address field—One or more 8-bit characters defining the particular station

Control field—One or two 8-bit characters

Information field—Any number of bits (may be zero bits)

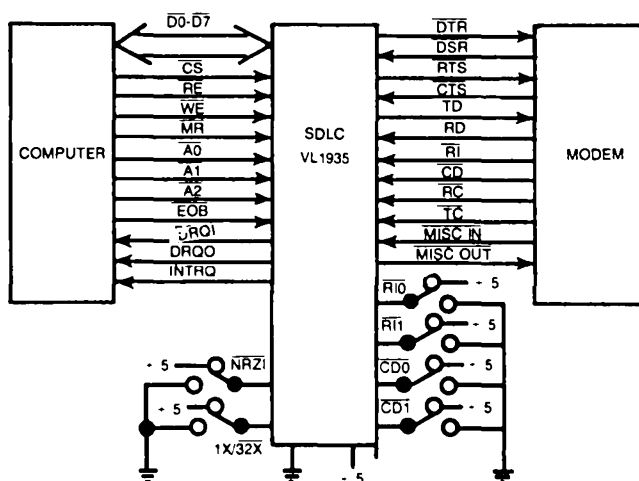
Frame Check Sequence—16-bit error checking field

The following features are also part of these protocols.

ZERO INSERTION/ZERO DELETION—Zero insertion/deletion is performed within the 2 Flags of a frame. If there are more than five 1's in a row, a 0 is automatically inserted after the fifth 1 and it is deleted upon reception by the receiver.

FRAME CHECK SEQUENCE (FCS)—A 16 bit cyclic redundancy check (CRC) calculation is performed during transmission of the data in between the I-field and before the final FLAG. Upon reception the receiver also performs a CRC calculation on the incoming data. If there were no transmission error, the Receiver CRC equals F0B8 (hex).

Figure 2. VL1935 TYPICAL SYSTEM INTERFACE



HARDWARE ORGANIZATION

The VL1935 block diagram is illustrated in Figure 1 and described below.

CPU Interface Registers

All of these registers are addressable and to be read from and/or written into by the CPU via the Data bus. These are 8-bit registers and have to be enabled via Chip Select (\overline{CS}) before any data transfer can be done.

CONTROL REGISTER 1, 2, 3 (CR1, 2, 3) Operations are initiated by writing the appropriate commands into these registers. CR1 should be programmed last.

RECEIVER HOLDING REGISTER (RHR) When Data Request Input is set ($DRQI=1$), contains received assembled character.

ADDRESS REGISTER (AR) Contains the address of the accessed VL1935, which is to be compared to the received address character (A-field).

INTERRUPT REGISTER (IR) Contains the cause of the current interrupt request.

TRANSMITTER HOLDING REGISTER (THR) Is to be loaded with the next in line character to be transmitted, when Data Request Output is set ($DRQO=1$).

STATUS REGISTER (SR) Contains the overall status of the VL1935 plus some information of the last received frame.

Non-Addressable, Internal Registers

These registers are transparent to the user, but is mentioned in these data sheets to help the understanding of the VL1935.

TRANSMITTER REGISTER (TR) This 8-bit register functions as a buffer between the THR and the TD output. It is loaded from the THR (if Data Command) with the next character to be transmitted. A FLAG character may also be loaded into this register under program control. This character is automatically shifted out to the Transmit Data output. When the last bit of the current transmitted character has left the TR register, a new character will be loaded into this register, setting $DRQO$ (Data command) or $INTRQ$ (Abort, Flag or FSC command). If at the time when only one bit remains left in the TR register, and the THR is not loaded or a new command is not programmed (Data command), an underrun error will occur.

RECEIVER REGISTER (RR) The received data is, via the Zero-Deletion logic shifted into this 8-bit register. The data is here assembled to a 5, 6, 7 or 8-bit character length and then, under the right conditions, parallel transferred to the RHR register.

FCS RECEIVE REGISTER AND FCS XMIT REGISTER The VL1935 contains a 16-bit CRC check register (FCS REC. REG.) and a 16-bit CRC generation register (FCS XMIT REG.). The generating polynomial is:

$$G(X) = X^{16} + X^{12} + X^5 + 1$$

The transmitter and receiver initialize the remainder value to all ones before CRC accumulation starts. The data is multiplied by X^{16} and is divided by $G(X)$. Inserted 0's are not included in the accumulation. Under program control, the complement called the frame check sequence (FCS) is sent with high order bit first.

Various Internal Circuits

ADDRESS COMPARATOR This 8-bit comparator is used to compare the contents of the Address Register with the first address character of the incoming frame. This feature is enabled by a bit in the Command Register. If enabled and there is a match, the received frame is valid and $DRQIs$ are generated for every character received (including the A-field). If enabled and there is not a match or there is no Global Address, the received frame is discarded. If not enabled, all received frames are valid and $DRQIs$ are generated.

ZERO INSERTION The transmitted data stream is continuously monitored by this logic. A zero is automatically inserted following five contiguous 1 bits anywhere between the beginning FLAG and the ending FLAG of a frame. The insertion of the zero bit thus applies to the contents of the Address, Control, Information Data, and the FCS field.

ZERO DELETION The received data stream is continuously monitored by this logic. Upon receiving five contiguous 1 bits, the sixth bit is inspected. If the sixth bit is a 0, it is automatically deleted from the data stream. If the sixth bit is a 1, the seventh bit inspected; if it is a 0, a FLAG is recognized; if it is a 1 an ABORT or GO AHEAD is recognized.

DATA BUS ($\overline{D7-D0}$) This is an inverted 8-bit bidirectional data bus.

SDLC LOOP-MODE CONTROL This logic supervises the VL1935 running in SDLC Loop mode. It monitors the received data for a GO-AHEAD pattern in the case when SDLC LOOP MODE bit ($CR22$) and ACT TRAN bit ($CR16$) are set. When GO-AHEAD pattern is received, this logic suspends the repeater function and initiates the transmitter function. For more details, see functional description of SDLC Loop Mode.

NRZI ENCODER/DECODER When this mode is selected, the NRZI Encoder encodes the "normal" transmitted data to NRZI formatted data and the NRZI Decoder decodes the received NRZI data to "normal" data.

A binary 1 for "normal data" is $TD = \text{high}$.

A binary 1 for NRZI data is $TD = \text{no change}$.

A binary 0 for "normal data" is $TD = \text{low}$.

A binary 0 for NRZI data is $TD = \text{change of state}$.

COMPUTER INTERFACE CONTROL This logic interfaces the CPU, to the VL1935. It supervises the read and write functions to the addressable registers, generates data requests and interrupts, decodes and initiates commands, monitors the status of VL1935, etc.

MODEM INTERFACE CONTROL This logic interfaces and supervises the modem control signals to/from the VL1935. It provides both dedicated (EIA Standard) and user defined control functions.

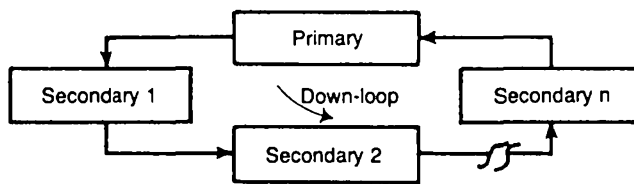
CLOCK CONTROL This logic interfaces the transmit and receive clocks to the VL1935. It converts the external clocks to the necessary internal clocks.

FUNCTIONAL DESCRIPTION

SDLC Loop Mode

The diagram below shows an SDLC Loop Data Link System. VL1935 can be used in any of these stations.

FIGURE 4. VL1935 SDLC LOOP DATA LINK



Each secondary station is normally a repeater in Receive mode (ACT REC bit on). The primary station is the loop controller. Signals sent out on the loop by the primary station are relayed from station to station, then back to the Primary. Any secondary station finding its address in the A-field captures the frame for action at that station. All received frames are relayed to the next station on the loop.

If a secondary station wants to transmit a message, it sets the ACT TRAN bit ($\overline{\text{CTS}}$ must be low) and waits for a GO AHEAD (GA) pattern. The ACT REC bit must be asserted for detection of the GA and other existing patterns. Until the GA pattern is received, this secondary station continues operating as a repeater. The primary station has the responsibility to generate the first GA pattern which can be accomplished by a flag followed by continuous 1's. The primary station must continue to send 1's until the GA has circulated through the entire loop. The first secondary station with its ACT TRAN bit set detects the GA and changes the last 1 bit of the GA pattern to a 0, thus generating the start flag of the frame it wants to transmit and preventing the GA pattern from propagating down the loop. The repeater function is then suspended by this secondary station and it goes into the transmit mode. When this secondary station completes its transmission frames, it resets the ACT TRAN bit and reverts back to the repeater mode. It repeats the 1's generated by the primary station to form another GA pattern from the final 0 of its end-

ing flag. The GA pattern propagates through the loop until a secondary station down the loop, that wants to transmit (ACT TRAN bit is set), intercepts the GA pattern and starts to transmit as described, or until the primary station receives the idles (continuous 1's), indicating that the GA pattern has circulated through the entire loop. The primary station then generates another GA pattern or terminates its final data frame with continuous 1's.

Repeaters (Secondary stations) delay the received data by 4 bits (NRZ1 = 5 bits) before transmission.

The $\overline{\text{RC}}$ and $\overline{\text{TC}}$ clocks must be tied together. The internal DPLL will not function in the loop mode.

1X/32X Clock Option

When 1X clock is selected, the data rate equals the external clock (receiver and transmitter).

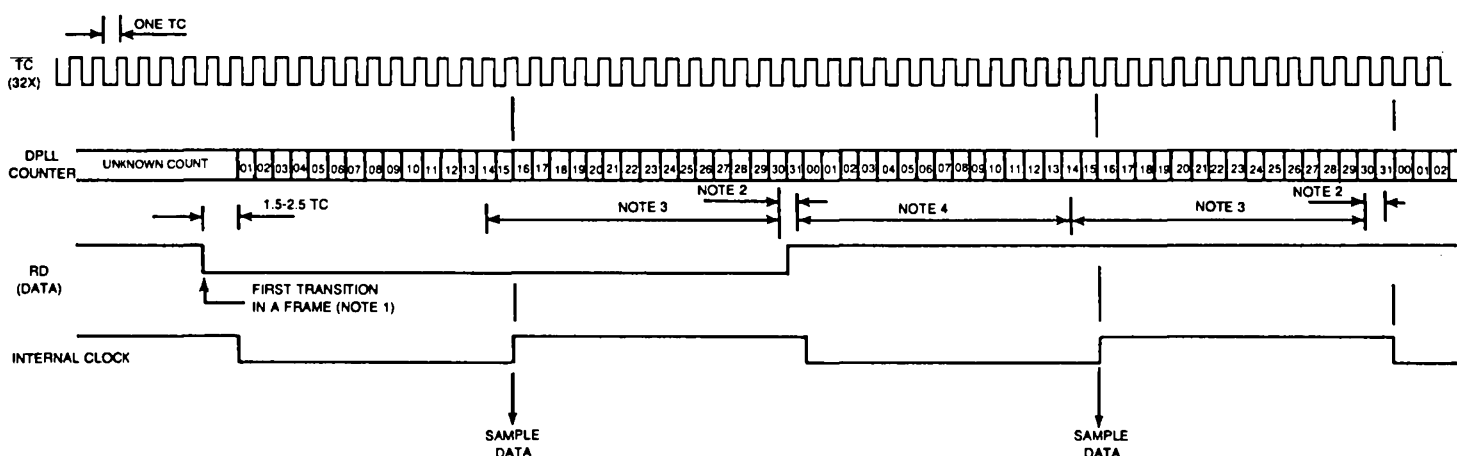
When 32X clock is selected, the external clock rate is 32 times faster than the data rate.

Digital Phase Locked Loop (DPLL)

This feature is particularly useful in NRZI mode and/or when asynchronous modem is used. The purpose of the DPLL is to synchronize the internal 1X clock to the received data, thus insuring that this data is sampled in the middle of the incoming serial data bit. DPLL is automatically in operation when 32X clock is selected.

The DPLL Logic is initiated at the first received data transition in a frame. Corrections, if needed, are then made for each received data transition. A 32-counter is used for this operation. At the beginning of each frame and at the first received data transition, this 32 counter is reset. From this time on, the counter increments with one count for each external clock pulse. At count 16 the internal 1X clock is forced to change state to high (this transition = sampling time). At count 32, the counter resets itself. This forces the internal 1X clock again to change state back to low.

FIGURE 5. VL1935 DPLL TIMING DIAGRAM



NOTE 1. FIRST DATA TRANSITION (FIRST FLAG) SETS THE DPLL COUNTER TO 01.

NOTE 2. DATA TRANSITION IN BETWEEN HERE, OR NO DATA TRANSITION AT ALL, CAUSES NO CORRECTION OF THE DPLL COUNTER.

NOTE 3. DATA TRANSITION IN BETWEEN HERE, WILL INCREMENT ONE COUNT TO THE DPLL COUNTER (ADD 01 TO WHAT IS SHOWN).

NOTE 4. DATA TRANSITION IN BETWEEN HERE, WILL DECREMENT ONE COUNT TO THE DPLL COUNTER (SUBTRACT 01 TO WHAT IS SHOWN).

At each received data transition, if the internal clock and the received data is out of synchronization, a correction is automatically made by ± 1 external clock period. See DPLL Timing Diagram in Figure 5.

End Of Block (EOB)

This is an FCS command. The main purpose of EOB is to allow the user to initiate FCS and FLAG without the need of using extra computer time. This is particularly practical in DMA applications. At the end of a frame, when the last information data character has already been loaded into the THR and once again DRQO is set, either a regular FCS command is written into CR1 Register, or $\overline{\text{EOB}}$ is to be activated. At the end of FCS, when INTRQ is set (XMIT OPCOM), the $\overline{\text{EOB}}$ if activated is to be reset again.

Serial Data Synchronization

The serial data is synchronized by the externally supplied Transmit Clock ($\overline{\text{TC}}$) and Receive Clock ($\overline{\text{RC}}$). When 1X clock is selected, the falling edge of $\overline{\text{TC}}$ generates new transmitted data and the rising edge of $\overline{\text{RC}}$ is used to sample the received data. When 32X clock is selected, a 32-counter (in the DPLL Logic) is used to synchronize the internal clock. At time 0, when the counter is reset to 0, the new transmitted data is generated. At time 16 (counter = 16) the received data is sampled, insuring that sampling is done in the middle of the received serial data bit. At count 32, the counter is reset to 0 again.

Self Test (Diagnostic) Mode

This feature is a programmable Loop back of data, enabling the user to make a complete test of the VL1935 with a minimum of external circuitry. In this mode, transmitted data to the TD pin, is internally routed to the received data input circuitry, thus allowing a CPU to send a message to itself to verify proper operation of the VL1935. The modem control signals $\overline{\text{DTR}}$ and $\overline{\text{RTS}}$ are deactivated (off) to insure no interference to/from the Data Communication Equipment (DCE). $\overline{\text{DSR}}$ and $\overline{\text{CTS}}$ are internally activated for proper input conditions. $\overline{\text{TC}}$ and $\overline{\text{RC}}$ should be supplied by the same source if 1X clock is selected.

Auto Flag

If this is selected and Data Command is executed, continuous Flags will be sent between frames. This eliminates the need to execute the Flag Command. In DMA applications in particular, this is very practical.

Extended Addressing

This type of addressing means, that there is more than one address character in the A-field. In receive mode, the first address character is compared in the Address Comparator of the VL1935. The other address character/s is to be compared by the CPU. The last address character is recognized by the fact that the LSB (bit 2°) is a 1.

PROGRAMMING

Controlling Operation

Prior to initiating data transmission or reception, CONTROL REGISTER 1-3 (CR1-3) must be loaded with control information from the CPU. The contents of these registers

will configure the VL1935 for the user's specific data communication environment. These registers should be loaded during power-on initialization and after a reset operation. They can be changed at any time that the respective transmitter or receiver is deactivated. The CR1-3 dictate what the transmitter will send: the type of character (DATA, ABORT, FLAG or FCS), the number of bits per character, and the number of bits in the residual character. Similarly, they tell the receiver the types of frames to look for: the number of bits per I-field character, whether to perform an address compare, and whether to watch for an extended address. The Control Register also control Data Terminal Ready ($\overline{\text{DTR}}$), Misc Out and the activation of both the transmitter and the receiver. For more detailed information, see Register Formats.

Monitoring Operation

Monitoring is done by use of the Interrupt Register (IR) and Status Register (SR). The IR register indicates when a frame is completed (transmitted or received), if there was an error and if there is a Data Set Change. It also monitors the states of INTRQ, DRQO and DRQI.

The SR register indicates if an error is recognized by IR, what type of error. It also monitors the modem control signals; Ring Indicator ($\overline{\text{RI}}$), Carrier Detect ($\overline{\text{CD}}$), Data Set Ready ($\overline{\text{DSR}}$) and Misc In.

Furthermore, the SR register monitors if the Receiver is idle, and also if in receive mode if the user has programmed the Receiver Character Length to be 8 bits per character, this register indicates the number of residual bits received. For more detailed information, see Register Formats.

Read/Write Control Of CPU Interface Registers

These registers are directly accessible from the CPU bus ($\overline{\text{D7-D0}}$) by a read and/or write operation by the CPU.

The CPU must set up the VL1935 register address ($\overline{\text{A2-A0}}$), Chip Select ($\overline{\text{CS}}$), Write Enable ($\overline{\text{WE}}$) or Read Enable ($\overline{\text{RE}}$) before each data bus transfer operation.

During a write operation, the falling edge of $\overline{\text{WE}}$ will initiate a VL1935 write cycle. The addressed register will then be loaded with the content of the Data Bus ($\overline{\text{D7-D0}}$). During a read operation, the falling edge of $\overline{\text{RE}}$ will initiate a VL1935 read cycle. The addressed register will then place its content onto the Data Bus ($\overline{\text{D7-D0}}$). The read/write operation is completed, when $\overline{\text{CS}}$ or $\overline{\text{RE/WE}}$ is brought high.

See Read/Write Timing diagram for more detailed information.

For read and write operation, the CR1-3 registers normally need no external clock. After reset of CR1-3, $\overline{\text{TC}}$ clock is required. The AR and THR registers need no external clock, and can only be written into. The RHR, IR and SR registers need Transmit Clock ($\overline{\text{TC}}$) or Receive Clock ($\overline{\text{RC}}$) to set various bits, and are read-only.

All these registers will get initialized by a Master Reset. A read operation of RHR resets the DRQI. A write operation to THR, resets the DRQO. A read operation of IR, resets IR bits 0 and 3-7. A read operation of SR, resets SR bits 0-2. For addressing and external clocks needed, see TABLE 2.

A more detailed description is shown in Figure 6 of each bit location. It should be known, that because the Data Bus Lines ($\overline{\text{D7-D0}}$) have inverted logic, a logic 1, asserted means low state. Also, a modem control signal which is inverted (example $\overline{\text{DTR}}$), is in on-state (asserted) when low.

TABLE 2. DEVICE ADDRESS CODES

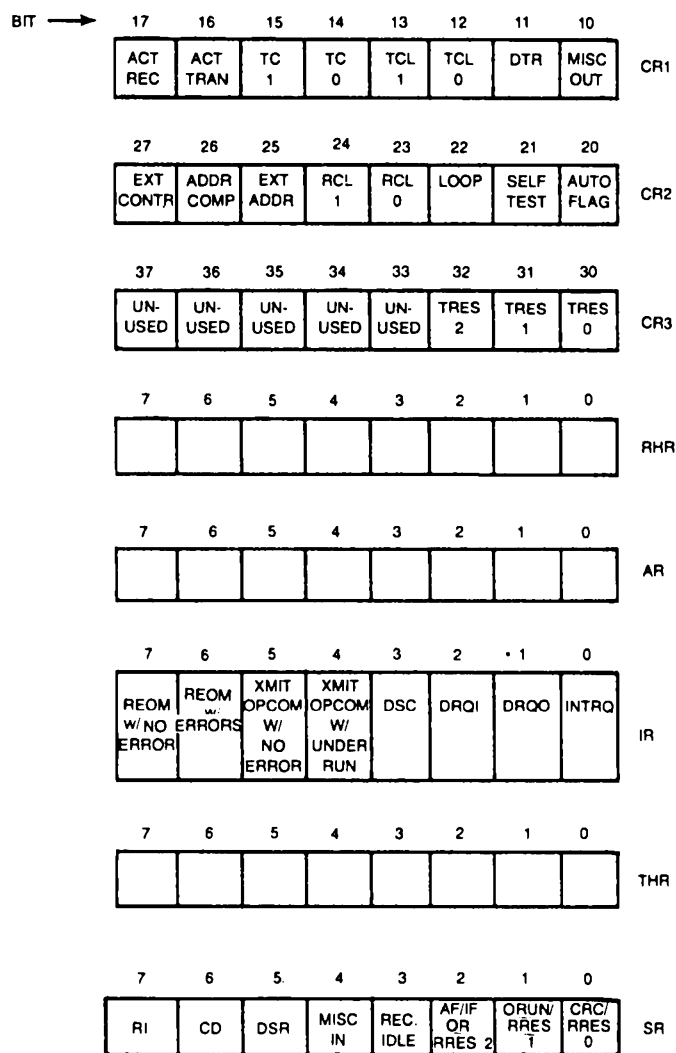
\overline{CS}	$\overline{A2}$	$\overline{A1}$	$\overline{A0}$	Read	Write	External Clock
L	H	H	H	CR1	CR1	None*
L	H	H	L	CR2	CR2	None*
L	H	L	H	CR3	CR3	None*
L	H	L	L	RHR	AR	RHR= \overline{RC} . AR=None
L	L	H	H	IR	THR	IR= \overline{TC} . THR=None
L	L	H	L	SR	—	SR0-3= \overline{RC} . SR4-7=None.
H	X	X	X	X	X	

L = V_{IL} at pins
H = V_{IH} at pins
X = Don't care

* 2.5 \overline{TC} clock cycles are required after a Master Reset to be able to read and write.

REGISTER FORMATS

Below shows a short form register format.


FIGURE 6. VL1935 BIT ASSIGNMENTS
Control Register 1 (CR1)

When initiating a transmit/receive operation, this should be the last register programmed.

Miscellaneous Output (CR10) This bit controls the Miscellaneous Output signal to the data set. When CR10 is a logical 0, Misc Out is off, when it is a logical 1, Misc Out is on.

DTR Command (CR11) This bit controls the data Terminal Ready (\overline{DTR}) signal to the data set. When CR11 is a logical 0, \overline{DTR} is off. When CR11 is a logical 1, \overline{DTR} is on. When the Self-Test mode is selected, \overline{DTR} signal is forced to an off state.

Transmitter Character Length (CR13, 12) These bits control the transmitted I-field data character length. The data character may be 5, 6, 7 or 8 bits long.

TABLE 3. TRANSMITTER CHARACTER LENGTH

CR13 (TCL1)	CR12 (TCL0)	Bits Per Character
0	0	8
0	1	7
1	0	6
1	1	5

Transmitter Commands (CR15, 14) These bits control the transmission of DATA (A-field, C-field and I-field), ABORT, FLAG, and FCS (FCS plus FLAG). When these commands are programmed, the previous command currently still in progress, will complete the transmission of its character. When this is done, a new character generated by this new command, will be transmitted.

CR 14, 15 can be programmed as follows:

- If DATA is programmed, the new character to be transmitted will be the character loaded (or still to be loaded) in the THR REGISTER.
- If ABORT is programmed, the new character will be eight logical 1's.
- If FLAG is programmed, the new character will be 01111110.
- If FCS is programmed, the new character which will be transmitted consists of the residual byte (which was automatically transferred to the XMIT REGISTER, provided that CR30-32 and are set correctly), followed by the 16-bit content of the FCS XMIT REGISTER and the FLAG.

One serial bit ahead of this new character (for FCS command the FLAG character), the CPU is signalled by DRQO or INTRQ that the VL1935 is again ready to receive a new command. DRQO is asserted by a DATA command and INTRQ (XMIT OPCOM) is asserted by an ABORT, FLAG or FCS command.

TABLE 4. TRANSMITTER COMMANDS

CR15 (TC1)	CR14 (TC0)	Command	Character/s Transmitted	Signal to CPU
0	0	DATA	Content of THR	DRQO
0	1	ABORT	1111 1111	INTRQ
1	0	FLAG	0111 1110	INTRQ
1	1	FCS	FCS + 01111110	INTRQ

In the case of the DATA command the user has two choices; 1. Change the command. 2. Keep the DATA command and load a new character into the THR register. For more information, please see the Transmission Timing diagram, Figure 7. See Table 4 for programming information.

Activate Transmitter (CR 16) This bit when set, enables the transmitter and sets RTS signal. If in SDLC Loop Mode (CR22 = set), the transmitter waits for a Go-Ahead pattern before the transmitter is enabled.

Activate Receiver (CR 17) This bit when set activates the receiver, which begins shifting in frames one character at a time into RR register for inspection.

CONTROL REGISTER 2 (CR2)

Auto Flag (CR20) When set, Flags (without INTRQs) will be continuously transmitted in between frames, when otherwise the transmitter would be in idle state.

Self-Test Mode (CR21) When set, the Transmitter Data Output is internally connected to the Receiver Data input circuitry. The modem control output signals are deactivated (off state). The modem control input signals are internally activated. This mode allows off-line diagnostic.

SDLC Loop Mode (CR22) When set, the VL1935 is conditioned to operate in an SDLC Loop Data Link system (see SDLC Loop Mode).

Receiver Character Length (CR24, 23) These bits indicate to the receiver how many bits per character there are to assemble for the I-field. The I-field characters may be 5, 6, 7 or 8 bits long. The unused bits read from RHR will be logical 0.

TABLE 5. RECEIVER CHARACTER LENGTH

CR24 (RCL1)	CR23 (RCL0)	Bits Per Character
0	0	8
0	1	7
1	0	6
1	1	5

TABLE 6. TRANSMITTER RESIDUAL COMMANDS

CR32 (TRES 2)	CR31 (TRES 1)	CR30 (TRES 0)	Residual Char. Length
0	0	0	No residual char. sent
0	0	1	1 bit
0	1	0	2 bits
0	1	1	3 bits
1	0	0	4 bits
1	0	1	5 bits
1	1	0	6 bits
1	1	1	7 bits

Extended Address (CR25) When set, this bit indicates to the receiver that there is more than one address character in the A-field. The receiver will expect another address character if the LSB in the current address character is a logical 0. The purpose of this bit: If a non-8-bit field character length is expected, the DRQIs will get out of synchronization if the VL1935 does not know exactly when the I-field will start. Not used in transmit mode.

Address Compare (CR26) When set, the first address character will be inspected in the Address Comparator. If there is a match with the AR register, or if the address compared is a Global Address (eight 1's) the frame is considered valid, causing DRQIs to be generated. Otherwise, the receiver does not react, and will continue comparing for a new valid address. If not set, all frames are considered valid.

Extended Control (CR27) When set, indicates that there are two control characters per frame. If not set, there is only one control character per frame. The purpose of this bit: If a non-8-bit I-field character length is to be received, the DRQIs will get out of synchronization if the VL1935 does not know when the I-field will start. Not used in transmit mode.

CONTROL REGISTER (CR3)

Transmit Residual Character Length (CR32, 31, 30) (Table 6) These bits inform the transmitter what bit-length the residual character will be. If no residual character is to be sent, these bits must be set to logical 0. (See Transmitter Commands).

Unused (CR33-37) These bits are not used, and are always a logical 0.

INTERRUPT REGISTER (IR)

This register contains the information why an interrupt INTRQ was generated. An IR register read operation, will reset bits 0, and 3-7. The Transmitter clock must be active to generate an interrupt.

Loading the THR register, will reset DRQO (bit 1). Reading the RHR register, will reset DRQI (bit 2). A new interrupt will occur if one is pending.

TABLE 7. DATA SET CHANGE PROGRAMMING

$\overline{CD1}$	$\overline{CD0}$	Interrupting edge of \overline{CD}	$\overline{RI1}$	$\overline{RI0}$	Interrupting edge of \overline{RI}
LO	LO	Rising and falling	LO	LO	Rising and falling
LO	HI	Falling	LO	HI	Falling
HI	LO	Rising	HI	LO	Rising
HI	HI	None	HI	HI	None

If a new interrupt is generated while the CPU is reading the IR register, this new interrupt will set the respective bit in the IR register one bit time later (this to avoid losing any interrupt). The status of bits 3–7 will accumulate until the IR register is read by CPU.

INTRQ (IR0) When set, indicates an interrupt and that there are one or more bits set in positions 3 through 7 of this register. This bit is a mirror image of INTRQ signal (pin 6).

When pin 6 (INTRQ) is not used for pending interrupts information and only the IR register is read to obtain the status of the interrupt bits (polling method), a minimum of two (2) bits times must be allowed between IR registers "read's" to insure an orderly flow of pending interrupts.

DRQO (IR1) When set, indicates a Data request output. This bit is a mirror image of DRQO signal (pin 18).

DRQI (IR2) When set, indicates a Data Request input. This bit is a mirror image of DRQI signal (pin 19).

Data Set Change (IR3) When set, indicates a change of state of the Data Set (Data Communication Equipment). This is a change of state of \overline{DSR} , \overline{CD} or \overline{RI} . The type of change of \overline{CD} and \overline{RI} that this bit will react to, is programmed by use of input signals $\overline{CD1/CD0}$ and $\overline{RI1/RI0}$ (Table 7).

XMIT Operation Complete with Underrun Error (IR4) When set, indicates that the transmitter command has been completed and there was an Underrun error. An Underrun error occurs when the Data Request Output (DRQO) is set, but THR register is not loaded in time.

XMIT Operation with No Error (IR5) When set, indicates that the transmitter command has been completed and there was no error.

Received End of Message With Errors (IR6) When set, indicates that a Received End of Message is detected, and there was an error. Errors include CRC, Overrun, Invalid Frame and Aborted Frame.

The SR Register bits 0–2 will indicate the exact type of error.

Received End of Message With No Error (IR7) When set, indicates that a Received End of Message is detected, and there was no error. The IR7 bit is the inverse of the REOM output signal.

STATUS REGISTER (SR)

This register contains the status of the receiver and some modem control signals. It also indicates (if REOM w/Errors) exactly what type of errors. If the Receiver Character Length is 8 bits, this register indicates the amount of Residual bits that was received. A read operation will reset bits 0–2.

Received Error/Received Residual Character Length (SR2-0) If REOM w/NO ERROR (IR7) is set, these bits (SR2-0), indicate the number of residual bits received (Table 8).

If REOM WITH ERROR (IR 6) is set, these bits indicate the type of error that occurred (Table 9).

TABLE 8.

CHAR. LENGTH	RES. BITS	S R 0	S R 1	S R 2
8 Bits/Char.	0	0	0	0
	1	0	0	1
	2	0	1	0
	3	0	1	1
	4	1	0	0
	5	1	0	1
	6	1	1	0
7 Bits/Char.	7	1	1	1
	0	0	1	0
	1	0	1	1
	2	1	0	0
	3	1	0	1
	4	1	1	0
	5	1	1	1
6 Bits/Char.	6	0	0	1
	0	1	0	0
	1	1	0	1
	2	1	1	0
	3	0	0	1
	4	0	1	0
5 Bits/Char.	5	0	1	1
	0	0	0	1
	1	0	1	0
	2	0	1	1
	3	1	0	0
4 Bits/Char.	4	1	0	1

TABLE 9.

Bit Set	Error
SR0	CRC
SR1	Overrun
SR2	Aborted or Invalid frame

Receiver Idle (SR 3) When set, indicates that the receiver is currently IDLE.

Miscellaneous Input (SR4) This is a mirror image of MISC IN signal. When this signal is set, SR4 bit is set.

Data Set Ready (SR5) This is mirror image of \overline{DSR} signal. When this signal is set, SR5 bit is set.

Carrier Detect (SR6) This is a mirror image of \overline{CD} signal. When this signal is set, SR6 bit is set.

Ring Indicator (SR7) This is the inverse of the \overline{RI} signal. When SR7 bit is set, a ringing signal has been received on the communication channel.

TRANSMITTER OPERATION

Prior to this operation, the programmable inputs and the transmit mode related register bits need to be programmed according to the user's specific data communications environment. The last bit to be set is always the ACT TRAN (CR16) bit.

Before this, the INTRQ has to be cleared, which can be done by reading the IR register. For more detailed information how to program the VL1935 see Programming.

As an example of how to program the VL1935 let's assume a 24-bit information is to be transmitted. The I-field would then consist of three 8-bit characters with no residual bits. CR3 should then be 00 (Hex).

Bits CR23-CR27 are for reception only (see Receiver Operation). The last register to be programmed is CR1. If MISC OUT is not used, this may be ignored. If a modem is used, DTR (CR11) is to be set. CR13 and CR12 should be logical 0's (8-bit char. length). CR15 and CR14 should be logical 0's (Data Command). ACT TRAN (CR16) bit is to be set. The ACT REC (CR17) is for reception only.

The DTR bit, when set, activates the \overline{DTR} signal, indicating to the modem to prepare for communication. When the modem is ready, it sends back a Data Set Ready (\overline{DSR}) to the VL1935. This causes the DSC (IR3) bit to set, which in turn activates INTRQ. The IR register is now read. Simultaneously, when the ACT TRAN (CR16) bit is set, this activates the Request to Send (RTS) signal, instructing the modem to enter into transmit mode. When the modem is ready to transmit data, it responds by activating the Clear to Send (CTS) signal.

The VL1935 is now conditioned to transmit. Now DRQO gets set, indicating to the CPU (or DMA) to load the first character (Address) into the THR. When this is done, DRQO will reset. As soon as the VL1935 is ready to be loaded with the next character to be transmitted, DRQO is again set. When the THR register is again loaded with a character, DRQO will again reset.

This same sequence continues until the last I-field character to be transmitted is loaded into the THR. If CRC checking is to be used, the next time when DRQO is set, an FCS command has to be programmed. This is accomplished by either setting CR15, 14 to both logical 1's or by activating the \overline{EOB} signal.

At the end of the FCS being transmitted, INTRQ will set indicating XMIT Operation Complete. The IR register is to be read to find out whether the frame was sent with or without error. Also the FCS Command which was used as described above has to be changed. If CR15, 14 were set, these have to be reset (to Data Command), or if \overline{EOB} was activated, this signal has to be deactivated. At this same time, the ACT TRAN bit is allowed to be reset, causing the TD output to go idle after the end Flag is sent. If the ACT TRAN bit is kept set, continuous Flags will be sent following the FCS.

If a new frame is to be sent right after this first frame, only one Flag is needed in between frames, meaning the frames have one common Flag character. In this case, the second frame Address character may be loaded at the same time the FCS command is programmed during the first frame.

Also, the ACT TRAN bit should be kept set in between frames. Every time DRQO gets set, the user must load the THR register before the last loaded character only has 1.5 bits left to be transmitted. In other words, when DRQO gets set, the user may wait (if 8-bit characters) up to 7.5 serial data bits before loading the THR. If THR is not loaded within this time, an Underrun error will occur.

If Auto Flag is not selected (CR20 = logical 0) the sequence will be a little different than described below. When the first DRQO is set, and after the Address character is loaded into THR, a Flag command is also programmed (CR15, 14 = 10).

This will set an interrupt (INTRQ), which indicates that the IR register must be read. Now, the Data Command is reprogrammed (CR15, 14 = 00).

For more information, see Transmission Timing diagram.

ABORT CONDITIONS

The function of prematurely terminating a data-link is called an "Abort." The transmitting station aborts by sending eight consecutive 1's. Unintentional Abort caused by 1's in the A-C- or I-field is prevented by zero insertion. Intentional Abort may be sent by programming an Abort command. Abort will also be sent in the case where THR is not loaded in time or FCS command is not programmed in time (= underrun). This means that after the DRQO is set, to avoid Abort; THR must be loaded, \overline{EOB} activated or FCS command programmed before there is only 1.5 bits left of the last character to be transmitted.

If this is not done, INTRQ (XMIT OPCOM w/underrun) is set and Aborts are transmitted until, either the command is changed or the THR is loaded. If in this same case, Auto Flag was programmed, one Abort (with INTRQ) would be generated, and thereafter continuous Flags (with no INTRQs) will be sent.

RECEIVER OPERATION

Prior to this operation, the programmable inputs and the receive mode related register bits have to be programmed according to the user's specific data communication environment. Also, the INTRQ has to be cleared. The last bit to be set is always the ACT REC (CR17) bit.

For more detailed information how to program the VL1935 see Programming. As an example, let's assume a 26-bit information is to be received, and the I-field is made up by 8-bit characters. The CR3 register is only for transmit mode, and may be ignored here. CR20 and CR 12-16 bits are also for transmit mode only, and therefore may also be ignored. CR21 and CR22 are to be logical 0s (no Self-Test and no SDLC Loop Mode). CR24, 23 are to be logical 0's (8-bit character I-field). If only one A-field and one C-field character is expected, and this VL1935 has a specific address, CR25 should be a logical 0, CR26 should be a 1, and CR27 should be a 0. The address to which the A-field should compare should be loaded into the AR register.

The status of the modem is monitored by the SR register, and it may be useful to read it at this time. CR1 is loaded as the last register. CR10 (Misc In) bit is optionable to the user. CR11 (DTR) is to be set if modem is used. CR17 (ACT REC) is now set, starting the input of frame characters into the Receiver Register (RR). When a Flag is detected, the next

8-bit character (address-character), when received, is compared to the character in the AR register. If these match, or if the received character is a Global address, this frame is valid, and the DRQI gets set. If the Address Comparator (CR26) bit is not set, all frames would be considered valid and generate DRQIs. When the RHR register is read, DRQI will be reset. All characters in a valid frame which are input into the RR register will set DRQI, and every time RHR is read by the CPU, DRQI will be reset.

During reception, the receiver also performs a CRC calculation on the incoming data. When the end Flag is received, INTRQ will get set, indicating Received End of Message. If the reception is completed with no error, IR7 (REOM w/no Error) bit will be set. When 8-bit characters are received SR 0-2 bits indicate the number of residual bits, in this case two. If IR6 (REOM w/Error) was set, SR 0-2 bits indicate the type of errors (see Receiver Error Indication).

When all characters including the A-field and the FCS-field are read, and when the REOM interrupt is recognized, it is up to the user to disassemble these mentioned characters from the received data. If non-8-bit characters are received, the amount of residual bits have to be calculated by the CPU after masking out the part of the ending Flag showing up in the last read character.

After end of frame, the receiver begins searching for a new frame.

(For more information, see Figure 8.)

RECEIVER ERROR INDICATION

When a frame is received, and REOM w/Error (IR6) is set, the type of error is indicated by the SR bits 0-2.

CRC Error (SR0) If the CRC calculation performed on the incoming data does not equal to F0B8 (HEX), this bit will be set.

Overrun Error (SR1) After DRQI is set, if the RHR is not read within one character minus one bit time, this bit will be set.

Aborted or Invalid Frame Error (SR2) If the frame is aborted or if in a frame the number of bits between flags are less than the required minimum (see Table 10), this bit will be set.

NOTES

1. TC-command—If two or more contiguous ABORTS or FLAGS are executed, the ACT TRAN (CR16) bit has to be reset before DATA-command can be executed.
2. Master Reset (\overline{MR})—Needs no clock during activation of MR. However, 2.5 clock cycles are required to reset the VL1935 after the falling edge of \overline{MR} .
3. IR-register—Immediately when IR register is read, bit 0 will reset. Bits 3-7 are reset one bit time later.
4. SR-register—Bits 0-2 are reset one bit time after SR register is read.
5. SDLC Loop mode—Go-ahead pattern may be sent by either sending IDLE or ABORT after Flag.
6. \overline{TC} and \overline{RC} clocks are completely independent of each other.
7. It is recommended to verify that the INTRQ signal (pin 6) is set prior to reading the IR register.
8. End Of Block (EOB) — Minimum activated time must be one (1) character time. It can be activated indefinitely using IDDLE or AUTO FLAG (CR20).

TABLE 10.

Receiver Programmed for	Valid Frame For VL1935			
	8 bit char	7 bit char	6 bit char	5 bit char
1 address, 1 control	≥25 bits	≥23 bits	≥21 bits	≥19 bits
2 addresses, 1 control	≥25 bits	≥24 bits	≥23 bits	≥22 bits
1 address, 2 controls				
3 addresses, 1 control	≥25 bits	≥25 bits	≥25 bits	≥25 bits
2 addresses, 2 controls				

[illegible]

NOTE 3. INF. DATA MAY CONSIST OF ANY NUMBER OF BITS.

[illegible]

NOTE 3. CPU DOES NOT KNOW UNTIL RECEIVED END OF MESSAGE (REOM) THAT THIS IS AN FCS CHARACTER.

SPECIFICATIONS
ELECTRICAL CHARACTERISTICS
Absolute Maximum Ratings

Storage Temperature	-55°C to +125°C (plastic package)
Storage Temperature	-65°C to +150°C (ceramic package)
Voltage on any pin with respect to GND (V_{SS})	-0.3 to +7.0 V
Power Dissipation	1W

DC Characteristics
 $T_A = 0^\circ\text{C to } +70^\circ$ $V_{SS} = 0\text{ V}, V_{CC} = +5 \pm 0.25\text{ V}$
TABLE 11. VL1935 DC CHARACTERISTICS

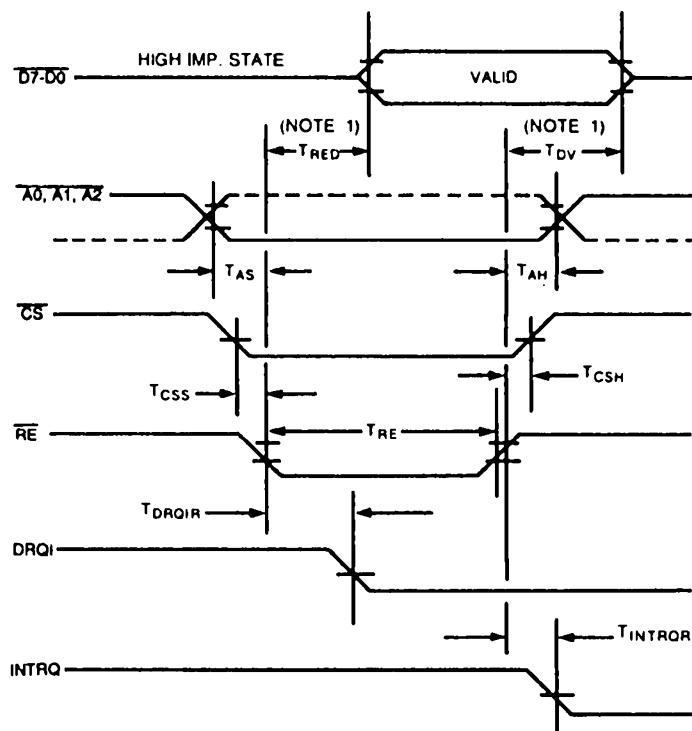
Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{LI}	Input Leakage			10	μA	$V_{IN} = V_{CC}$
I_{LO}	Output Leakage			10	μA	$V_{OUT} = V_{CC} \text{ or } V_{SS}$
V_{IH}	Input High Voltage	2.4			V	
V_{IL}	Input Low Voltage			0.8	V	All Inputs
V_{OH}	Output High Voltage	2.4			V	$I_O = -100\mu\text{A}$
V_{OL}	Output Low Voltage			0.4	V	$I_O = 1.6\text{mA}$
I_{CC}	Supply Current		70	210	ma	

AC Characteristics
 $T_A = 0^\circ\text{C to } +70^\circ$ $V_{SS} = 0\text{ V}, V_{CC} = +5 \pm 0.25\text{ V}$
TABLE 12. VL1935 AC CHARACTERISTICS

Symbol	Parameter	- 10		- 11		- 12		- 13		Units	Conditions
		Min	Max	Min	Max	Min	Max	Min	Max		
	READ & WRITE (Fig. 9, 10)										
T_{AS}	Address Set-Up	20		20		20		20		ns	
T_{AH}	Address Hold	20		20		20		20		ns	
T_{CSS}	Chip Select Set-up	20		20		20		20		ns	
T_{CSH}	Chip Select Hold	20		20		20		20		ns	
	READ (Fig. 9)										
T_{RED}	Data Delay from \overline{RE} Asserted		315		290		265		240	ns	
T_{DV}	Date Valid from \overline{RE} Deasserted	0	140	0	140	0	140	0	140	ns	
T_{DRQIR}	DRQI Reset Delay		280		280		280		280	ns	
T_{INTRQR}	INTRQ Reset Delay		280		280		280		280	ns	
T_{RE}	\overline{RE} Pulse width	325		300		275		250		ns	
	WRITE (Fig. 10)										
T_{DS}	Data Set-up	200		180		160		140		ns	
T_{DH}	Data Hold	20		20		20		20		ns	
T_{DRQOR}	DRQO Reset Delay		330		330		330		330	ns	
T_{WE}	\overline{WE} Pulse width	200		180		160		140		ns	
	TRANSMIT & RECEIVE (Fig.11)										
T_{RDS}	Receive Data Set Up	150		150		150		150		ns	
T_{RDH}	Receive Data Hold	150		150		150		150		ns	
T_{TDO}	Transmit Data Out Delay		125		125		125		125	ns	
$1 \times F_C$	1X Clock		.5		1.0		1.5		2.0	MHz	at 50% duty cycle
$32 \times F_C$	32X Clock		1.0		1.5		2.0		2.5	MHz	at 50% duty cycle
	RISE & FALL (Fig. 12)										
T_R	Rise Time		20		20		20		20	ns	See figure 1
T_F	Fall Time		20		20		20		20	ns	

NOTE: All A.C. Timing Measurements made at 0.8 V and 2.0 V.

FIGURE 9. VL1935 READ TIMING DIAGRAM



NOTE 1. T_{RED} and T_{DV} starts from where both \overline{CS} and \overline{RE} are active.

FIGURE 10. VL1935 WRITE TIMING DIAGRAM

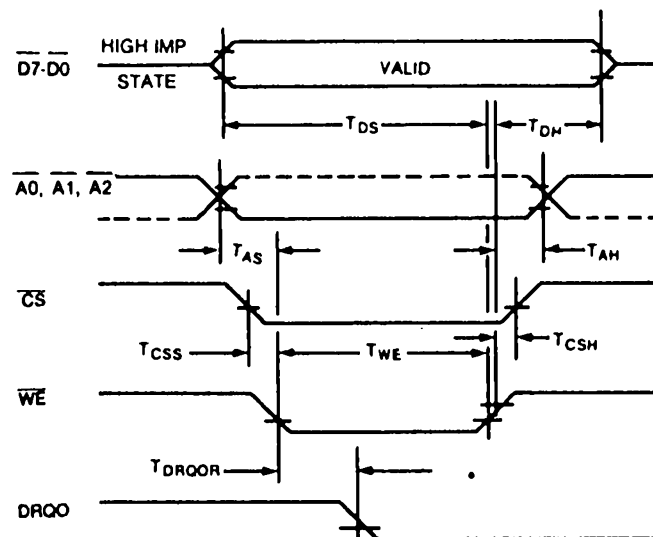


FIGURE 11. RECEIVER AND TRANSMITTER TIMING

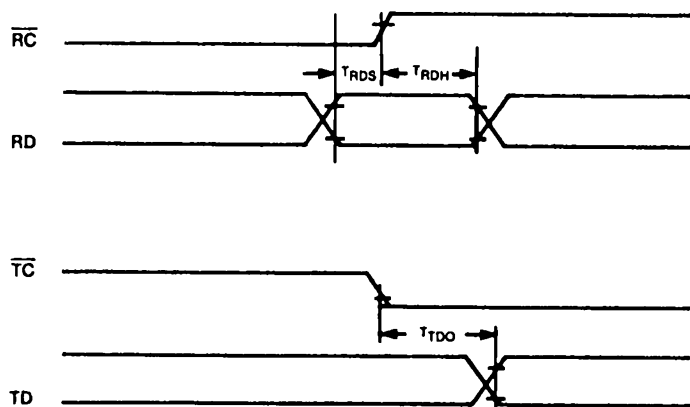


FIGURE 12. VL1935 RISE AND FALL TIMING DIAGRAM

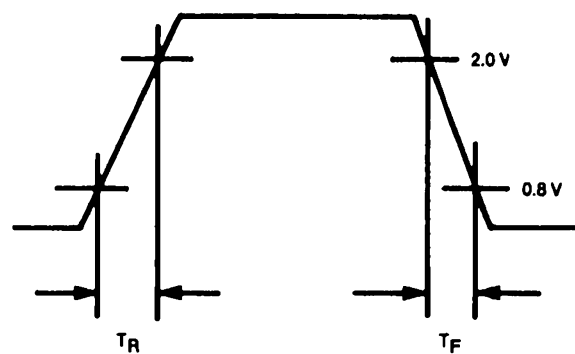


FIGURE 13. VL1935 TRANSMITTER FLOW CHART

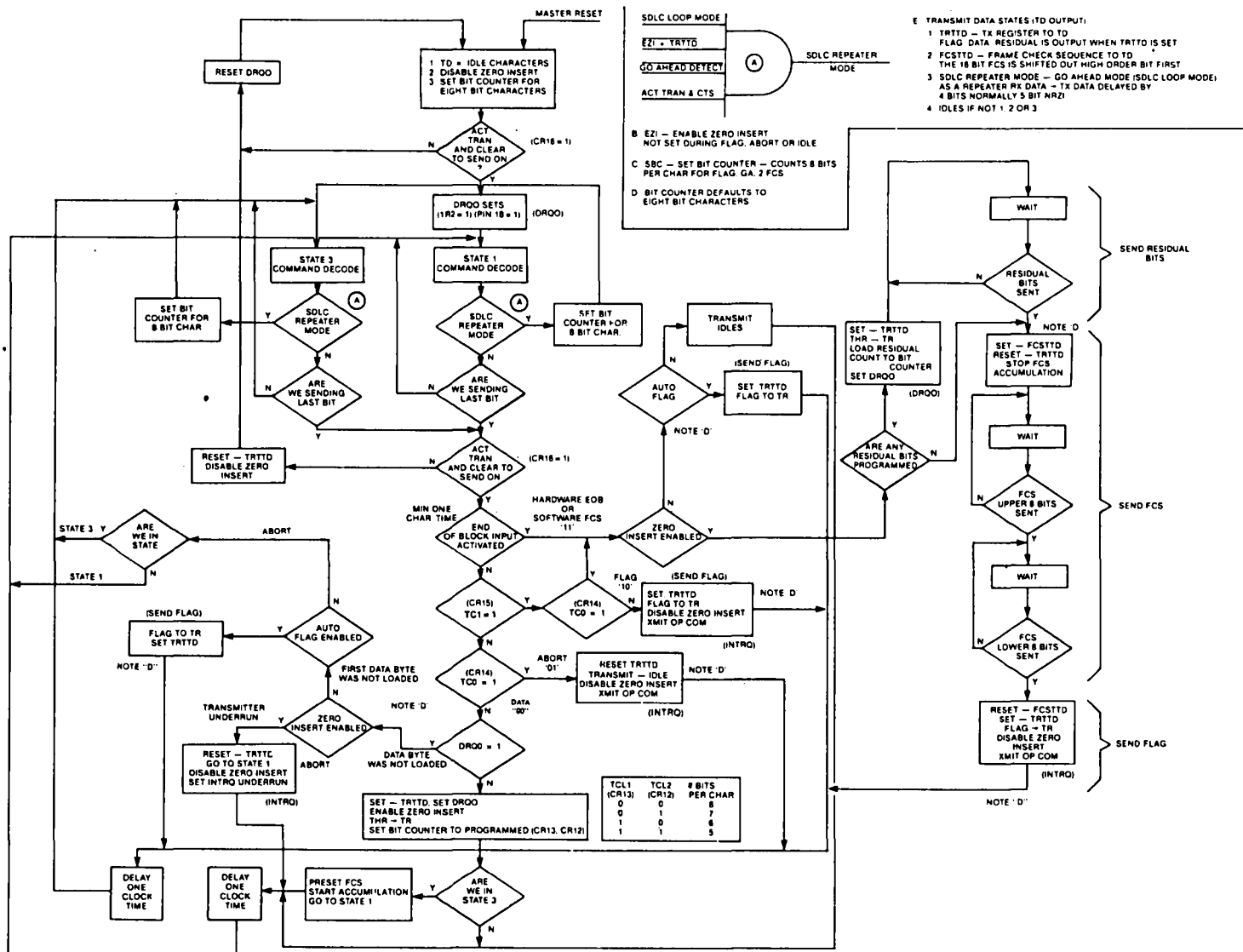
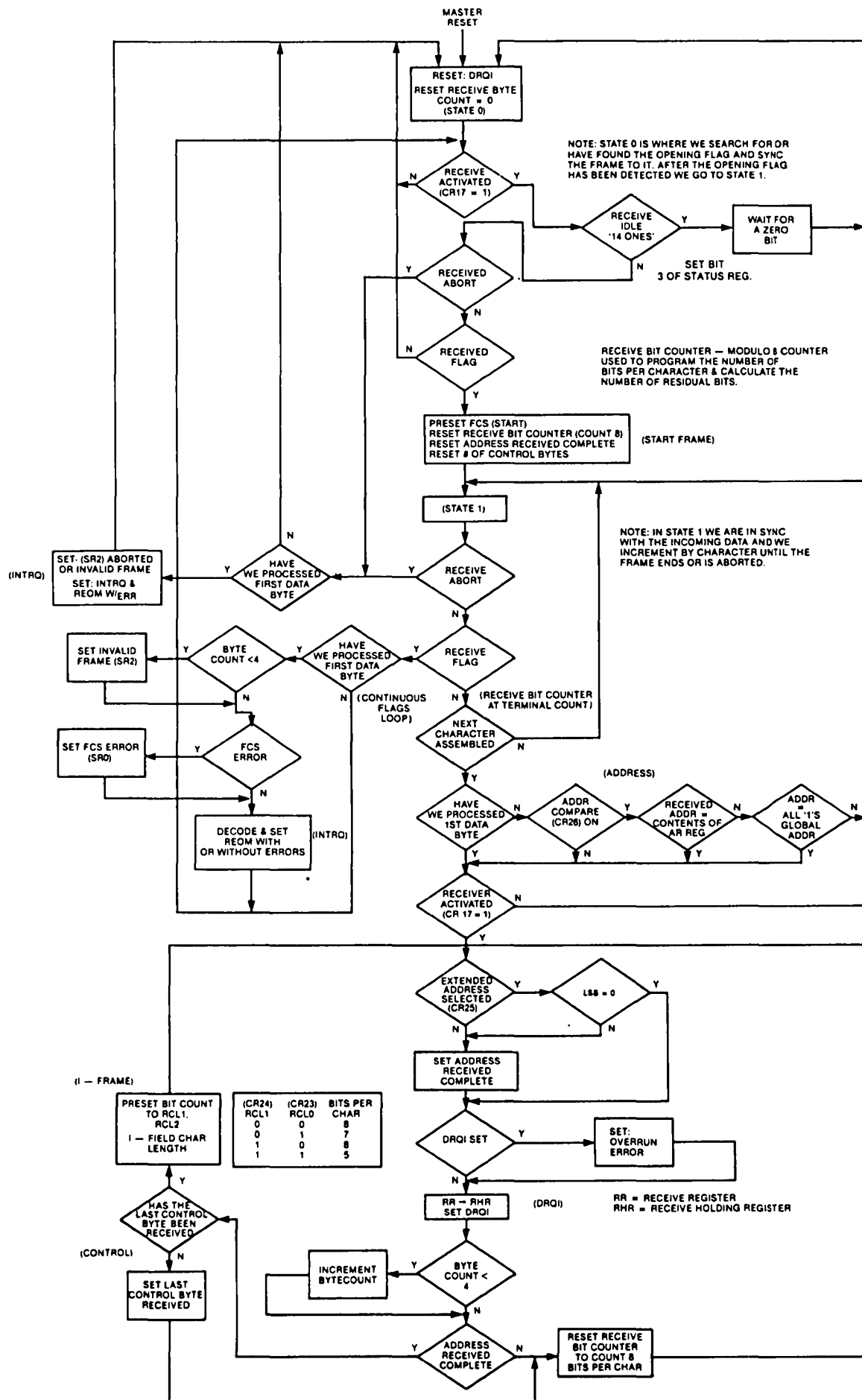


FIGURE 14. VL1935 RECEIVER FLOW CHART



16 x 16 PARALLEL MULTIPLIER-ACCUMULATOR

FEATURES

- 16 x 16 parallel multiplication and product accumulation
- High-speed multiply-accumulate time
–65 ns, typical
–90 ns, max
- CMOS silicon-gate technology
- Single 5 V supply
- Low power
–0.2 W typical
- Standard TTL-compatible I/O levels
- Performs double-precision subtraction, addition, and multiplication, including rounding control
- Pin-for-pin functional replacement for WTL1010, WTL2010, TDC1010J, LMA1010, and AMD29510
- 64-pin ceramic and plastic DIP
- 68-terminal plastic leaded chip carrier (PLCC)

DESCRIPTION

The VL2010 is a 16 x 16 parallel multiplier-accumulator (MAC) that offers ultra-low power consumption and very high performance. High performance is achieved through the use of the efficient Booth's algorithm and advanced VLSI processing technology.

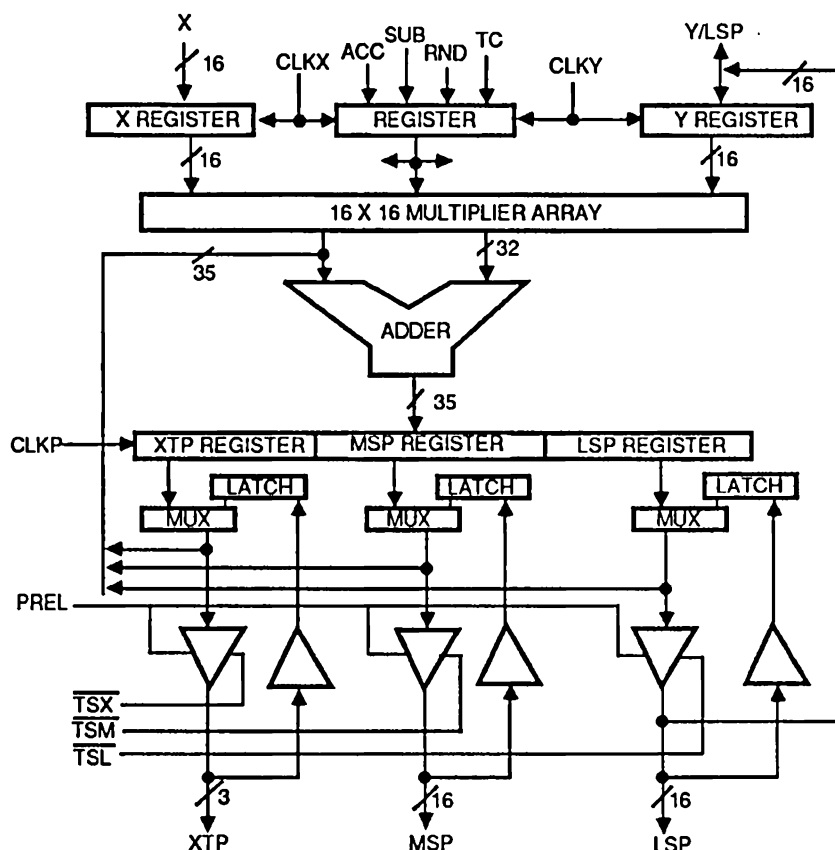
The VL2010, under control of the ACC input, performs either the multiply only, or the multiply-accumulate function. In either mode, input data X and Y can be specified as two's complement or unsigned magnitude. Input data representation is selectable via the input control line, TC. In the multiply-only mode, extended product (XTP) data is sign-extended or set to zero for two's complement and unsigned-magnitude arithmetic, respectively. An RND control is available for rounding up the most significant product (MSP) and extended product (XTP) data. In the multiply-accumulate mode, the double-precision accumulated answer is rounded back to single-precision or single-precision plus XTP bits.

The VL2010 architecture includes input and output data registers, as well as three-state output data buses with independent, non-registered control. Time-multiplexing is used for the common least significant product (LSP) and Input Data (Y) I/O lines. Input lines TSX, TSM, and TSL, respectively, control the outputs of the XTP, MSP, and LSP registers.

In the multiply-accumulate mode (ACC active), output data can be added to or subtracted from the last product. When SUB is also active, subtraction occurs. Otherwise, addition is performed.

The VL2010 can be efficiently applied in a variety of digital signal processing functions, including digital filtering (recursive, non-recursive, wave) and FFT processing (complex multiplication, butterfly computation). In addition, the VL2010 can be employed effectively in upgrading the computational capability of mini- and microcomputer systems.

BLOCK DIAGRAM

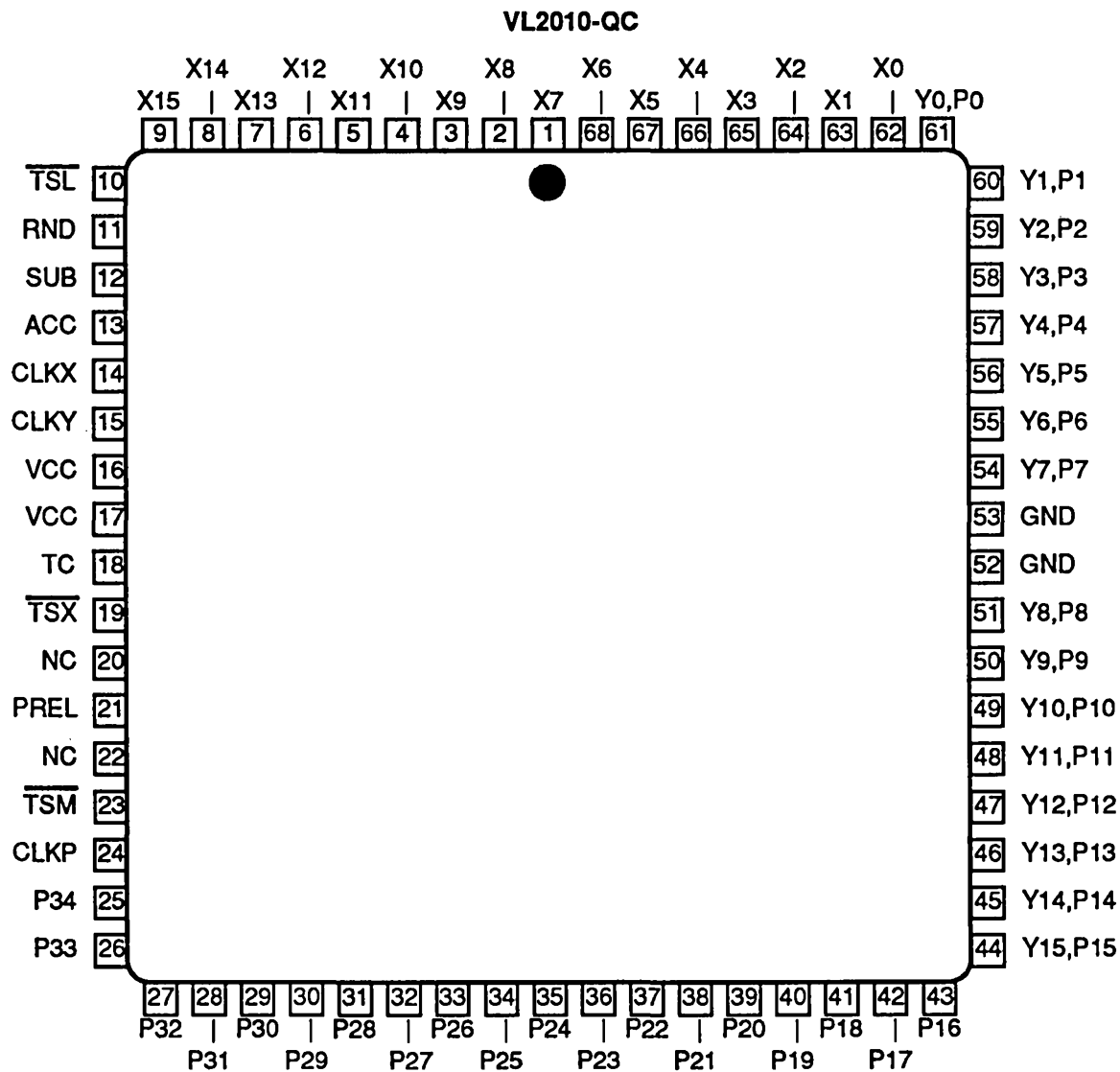


ORDER INFORMATION

Part Number	Multiply/ Accumulate Time	Package
VL2010-90CC	90 ns	Ceramic DIP
VL2010-90PC		Plastic DIP
VL2010-90QC		PLCC

Note: Operating temperature range is 0°C to +70°C.

PIN DIAGRAM



PIN DESCRIPTIONS

X

Data Input

X is a 16-bit input. Data bits are loaded on the rising edge of CLKX.

Y/LSP

Data Input/

Data Output

These pins share functions between Y (16-bit data input) and LSP (least significant product output). Input data bits are loaded on the rising edge of CLKY. Output LSP data bits are available following the rising edge of CLKP.

MSP

Data Output

The 16-bit most-significant product output. MSP data is available following

CLKX, CLKY

Input Clocks

These X and Y data input register clocks are active on their rising edges.

ACC

Accumulate

A HIGH level input permits the contents of the LSP, MSP, and XTP registers to be added to the multiplier output. A LOW level input allows multiplication only. The ACC signal is loaded on the rising edge of either CLKX or CLKY, and must be valid for the entire duration of input data.

SUB

Subtract

When ACC and SUB are both HIGH, the contents of the output register are subtracted from the last product generated, and the difference is stored back into the output registers at the rising edge of the next CLKP. When ACC is HIGH and SUB is LOW, addition instead of subtraction is performed. The SUB signal is loaded into the SUB register at the rising edge of either CLKX or CLKY.

The SUB signal must be valid over the same period that the input data is valid. When ACC is LOW, SUB is a "Don't Care" pin.

RND

Round

A HIGH-level input causes a "1" to be added to the most significant bit of the LSP to round up MSP and XTP data. RND is loaded on the rising edge of either CLKX or CLKY and must be valid for the duration of the input data.

TC

Two's Complement/ Unsigned Magnitude

A HIGH-level input defines X and Y as two's complement data, while a LOW level defines the input data as unsigned magnitude. As with ACC, SUB, and RND, TC is loaded at the rising edge of either CLKX or CLKY and must be valid for the duration of the input data.

TSX, TSM, TSL

3-state Output Controls

The LSP, MSP, or XTP output buffers are at high-impedance (output disabled) when TSL, TSM, or TSX, respectively, is HIGH. These are direct, nonregistered control signals. The output drivers are enabled when TSL, TSM, or TSX is LOW.

PIN DIAGRAM

VL2010-PC,CC

X6	1	64	X7
X5	2	63	X8
X4	3	62	X9
X3	4	61	X10
X2	5	60	X11
X1	6	59	X12
X0	7	58	X13
Y0,P0	8	57	X14
Y1,P1	9	56	X15
Y2,P2	10	55	TSL
Y3,P3	11	54	RND
Y4,P4	12	53	SUB
Y5,P5	13	52	ACC
Y6,P6	14	51	CLKX
Y7,P7	15	50	CLKY
GND	16	49	VCC
Y8,P8	17	48	TC
Y9,P9	18	47	TSX
Y10,P10	19	46	PREL
Y11,P11	20	45	TSM
Y12,P12	21	44	CLKP
Y13,P13	22	43	P34
Y14,P14	23	42	P33
Y15,P15	24	41	P32
P16	25	40	P31
P17	26	39	P30
P18	27	38	P29
P19	28	37	P28
P20	29	36	P27
P21	30	35	P26
P22	31	34	P25
P23	32	33	P24

PRELOAD TRUTH TABLE

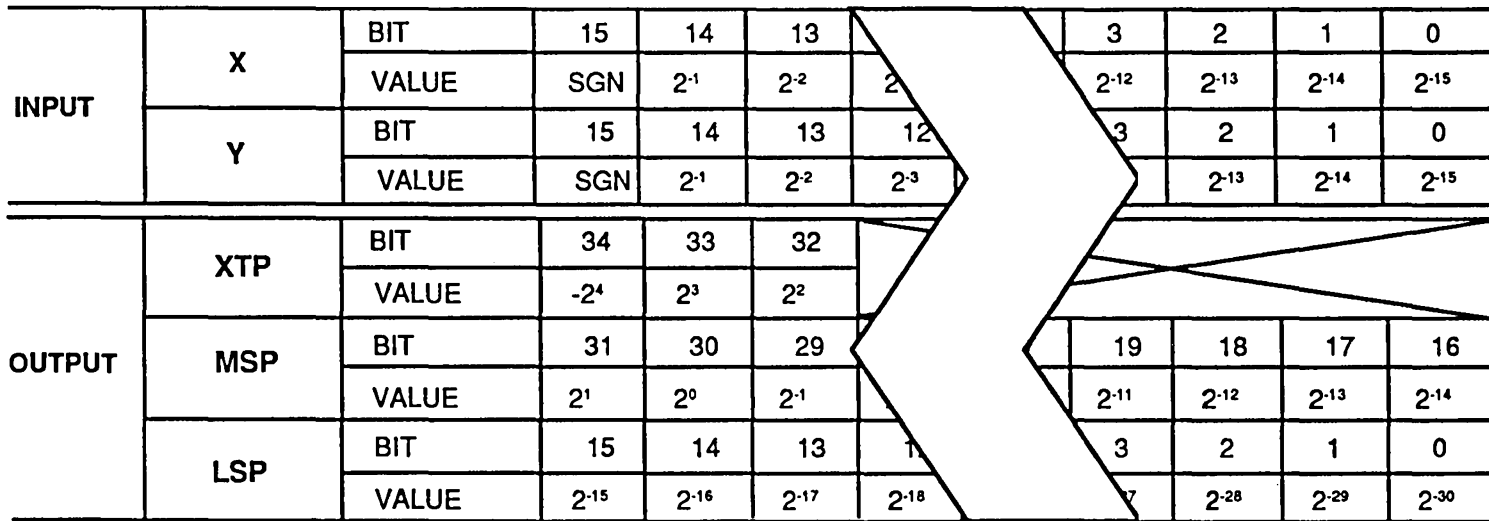
PREL	TSX	TSM	TSL	XTP	MSP	LSP
0	0	0	0	Q	Q	Q
0	0	0	1	Q	Q	Hi-Z
0	0	1	0	Q	Hi-Z	Q
0	0	1	1	Q	Hi-Z	Hi-Z
0	1	0	0	Hi-Z	Q	Q
0	1	0	1	Hi-Z	Q	Hi-Z
0	1	1	0	Hi-Z	Hi-Z	Q
0	1	1	1	Hi-Z	Hi-Z	Hi-Z
1	0	0	0	Hi-Z	Hi-Z	Hi-Z
1	0	0	1	Hi-Z	Hi-Z	PL
1	0	1	0	Hi-Z	PL	Hi-Z
1	0	1	1	Hi-Z	PL	PL
1	1	0	0	PL	Hi-Z	Hi-Z
1	1	0	1	PL	Hi-Z	PL
1	1	1	0	PL	PL	Hi-Z
1	1	1	1	PL	PL	PL

Notes:

Hi-Z = Output buffers at high impedance (Output disabled).

Q= Output buffers at low impedance. Contents of output registers will be transferred to output pins.

PL= Output buffers at high impedance, or output disabled. Preload data supplied externally will be loaded into the output register at the rising edge of CLKP.

DATA FORMATS
FRACTIONAL TWO'S COMPLEMENT

Notes:

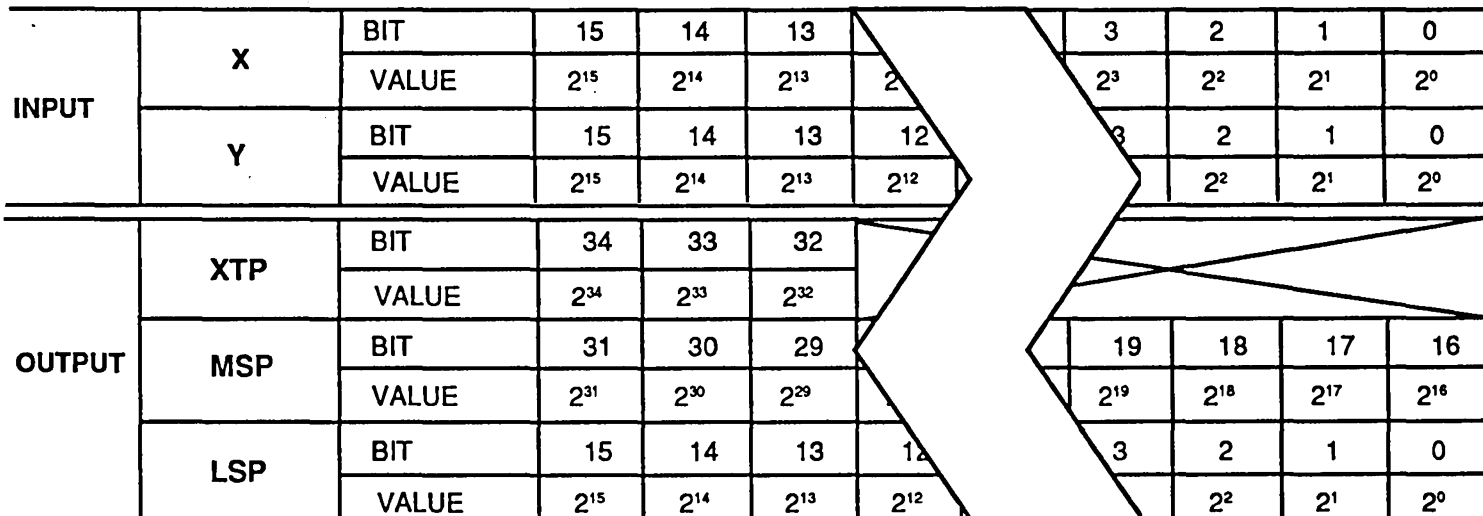
1. The value of the input sign bits is -2^0 .

2. The format shown uses a two's complement fractional notation. Note that the location of the binary point signifying the separation of the integer and fractional fields is just after the sign, between the sign (-2^0) and the next most significant bit for the multiplier inputs (-2^1). This scheme is carried over to the output format, except that an extended significance to the integer field is provided to extend the utility of the accumulator. Consistent with the input notation, the output binary point is located between the -2^0 and the -2^1 bit positions.

The location of the binary point is arbitrary, as long as one is consistent with both input and output formats. One can consider the number field entirely integer, i.e., with the binary point just to the right of the least significant bit for input, product, and accumulated sum.

3. When nonaccumulating, all first four bits (P34 to P31) will indicate the sign of the product. The P30 term will also indicate the sign, except for the one exceptional case when multiplying -1×-1 . Note that, with the additional significant bits available on this multiplier, -1×-1 is a valid operation yielding $+1$ product.

4. Whether accumulating the sum of products or doing single products, there is no change in format. However, the three additional most significant bits (the guard bits) are provided to allow valid summation beyond that available for a single multiplication product. For further clarification, no difference exists between this organization and one which would have the product accumulation off-chip in a separate 18-bit adder. Taking the sign at the most significant bit position guarantees that the largest number field will be used. In operation, the sign will be extended into the lesser significant bit positions when the accumulated sum only occupies a right-hand portion of the accumulator. As an example, when the sum only occupies the least three bit positions, then the sign will be extended through the 16 most significant positions.

INTEGER MAGNITUDE


AC CHARACTERISTICS $T_A = 0^\circ\text{C to } 70^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm .25\text{ V}$

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
t_D	Output Delay		25	35	ns	Load 1 (Figure 3)
t_{ENA}	Output Enable Delay		30	35	ns	Load 2 (Figure 4)
t_{DIS}	Output Disable Delay		25	30	ns	Load 2 (Figure 4)
t_{MA}	Multiply-Accumulate Time		65	90	ns	
t_{PW}	Clock Pulse Width	25			ns	
t_S	Input Register Setup Time	25			ns	
t_H	Input Register Hold Time	0			ns	

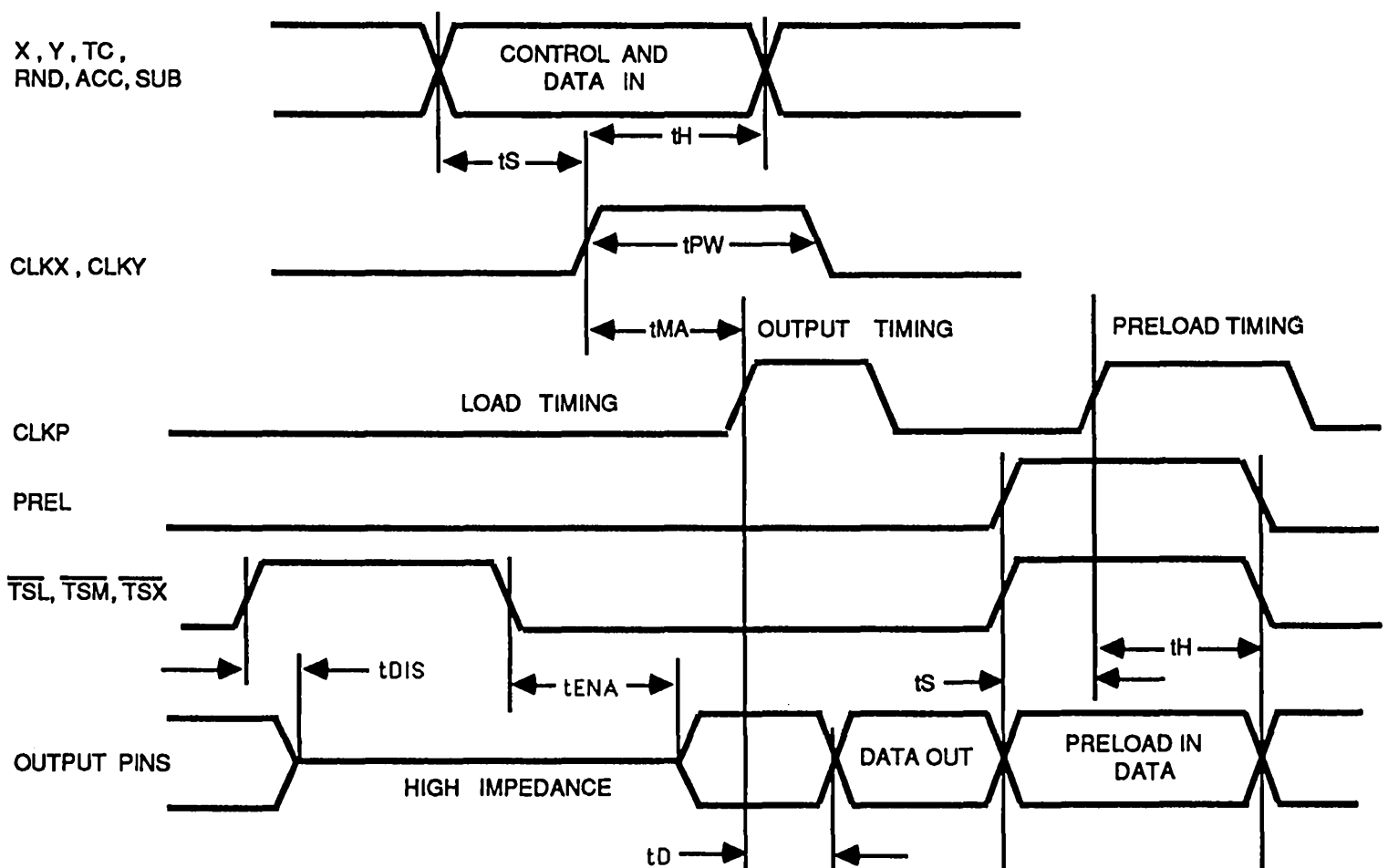
TIMING DIAGRAM


FIGURE 1. INPUT EQUIVALENT CIRCUIT

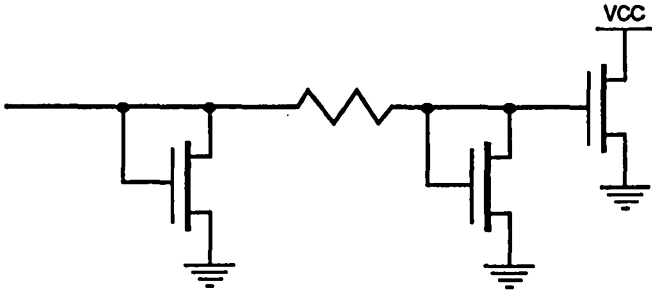


FIGURE 4. TEST LOAD FOR 3-STATE DELAY

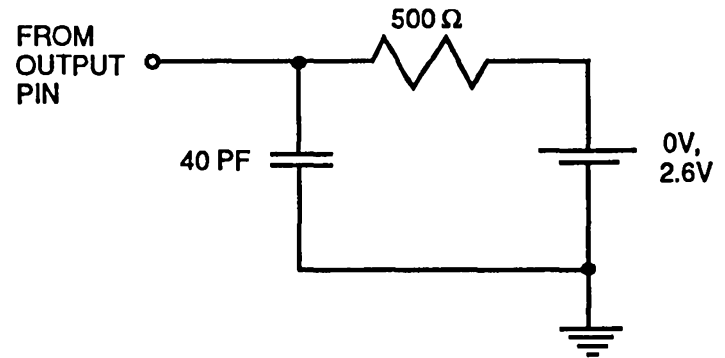


FIGURE 2. OUTPUT CIRCUIT

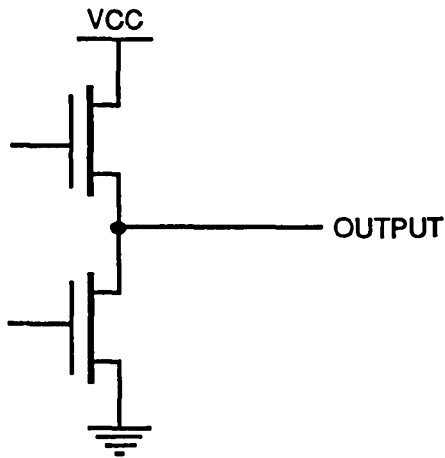
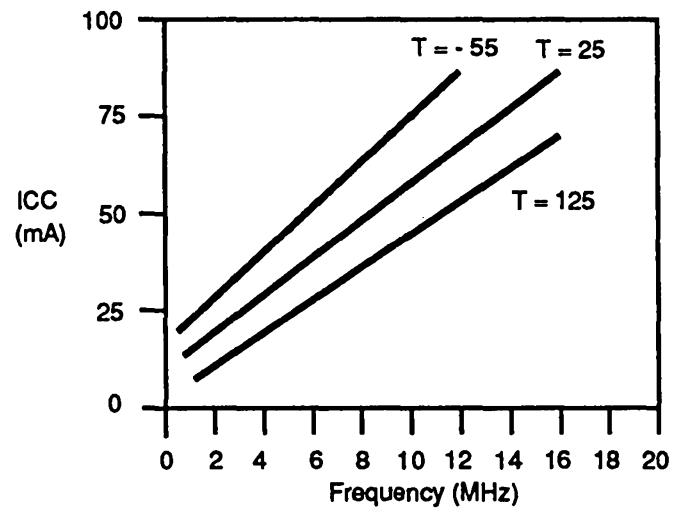


FIGURE 5. SUPPLY CURRENT VS OPERATING FREQUENCY



Note:
Temperature (T) is measured in degrees Centigrade.

FIGURE 3. TEST LOAD FOR DELAY MEASUREMENT

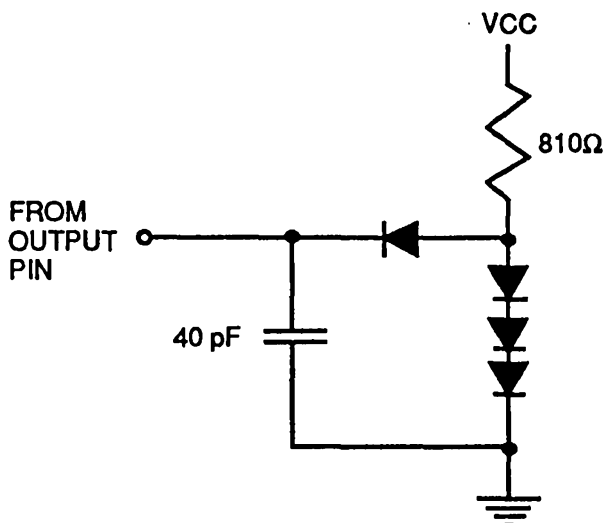
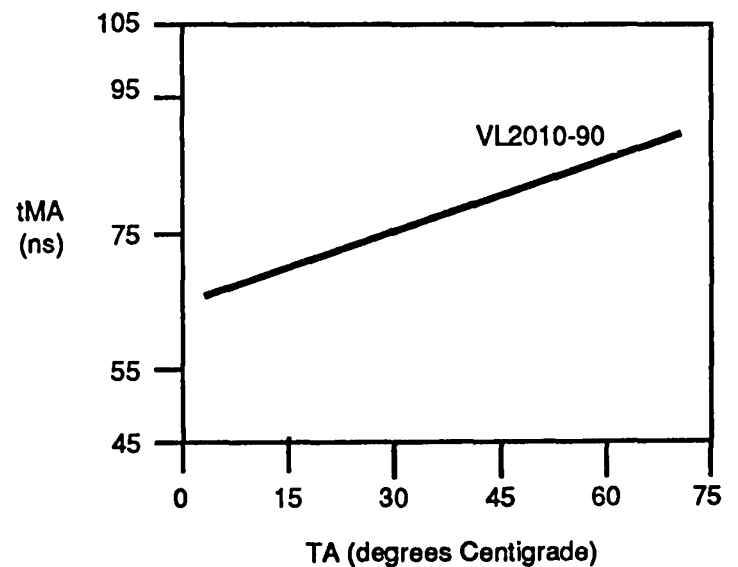


FIGURE 6. MULTIPLY-ACCUMULATE TIME VS AMBIENT TEMPERATURE



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	-0.5 to 7.0 V
Input Voltage	-0.5 to 7.0 V
Output Voltage	-0.5 to 7.0 V
Operating Temperature	0 °C to 70°C
Storage Temperature	-65 °C to 150 °C
Lead Temperature (10 Sec.)	300 °C
Maximum Junction Temp.	175 °C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above

those listed on the operational sections of this specification is not implied and exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

DC CHARACTERISTICS $T_A = 0\text{ }^{\circ}\text{C to }70\text{ }^{\circ}\text{C}$, $V_{CC} = 5\text{ V} \pm .25\text{ V}$

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V_{IH}	High-level Input Voltage	2.0			V	
V_{IL}	Low-Level Input Voltage		0.8		V	
V_{OH}	High-level Output Voltage		2.4	3.0	V	$V_{CC} = \text{Min}$; $I_{OH} = -0.4\text{ mA}$
V_{OL}	Low-Level Output Voltage		0.3	0.4	V	$V_{CC} = \text{Min}$; $I_{OL} = 4.0\text{ mA}$
I_{IH}	High-level Input Current		10	75	μA	$V_{CC} = \text{Max}$; $V_{IH} = 2.4\text{ V}$
I_{IL}	Low-Level Input Current		10	75	A	$V_{CC} = \text{Max}$; $V_{IL} = 0.4\text{ V}$
I_{OH}	High-level Output Current	-0.4			mA	
I_{OL}	Low-level Output Current	4.0	8.0		mA	
I_{CC}	Supply Current at DC		5	10	mA	$V_{CC} = \text{Max}$; DC Cond.
I_{CC}/F	Supply Current Increase/MHz		4	8	mA/MHz	$V_{CC} = \text{Max}$

CAPACITANCE $T_A = 0\text{ }^{\circ}\text{C to }70\text{ }^{\circ}\text{C}$

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
CI	Input Capacitance	Clocks, Unlatched Controls		20	pF	
		Data, Latched Controls		10		
CO	Output Capacitance		6	10	pF	

FLOPPY DISK FORMATTER/ CONTROLLER FAMILY

FEATURES

- On-chip PLL data separator
- On-chip write precompensation logic
- Single +5 V supply
- Accommodates single and double density formats
 - IBM 3740 (FM)
 - IBM 34 (MFM)
- Automatic seek with verify
- Multiple sector read/write
- TTL compatible
- Programmable control
 - Selectable track-to-track access
 - Head load timing
- Software compatible with the FD179X series
- Soft sector format compatibility

DESCRIPTION

The VL279X are N-Channel Silicon Gate MOS LSI devices which perform the functions of a Floppy Disk Formatter/Controller in a single chip implementation. The VL279X, which can be considered the end result of both the FD1771 and FD179X designs, is IBM 3740 compatible in single density mode (FM) and System 34 compatible in Double Density Mode (MFM). The VL279X contains all the features of its predecessor the FD179X plus a high performance Phase-Lock-Loop Data Separator as well as Write Precompensation Logic. In Double Density mode, Write Precompensation is automatically engaged to a value programmed via an external potentiometer. In order to maintain compatibility, the FD1771, FD179X and VL279X designs were

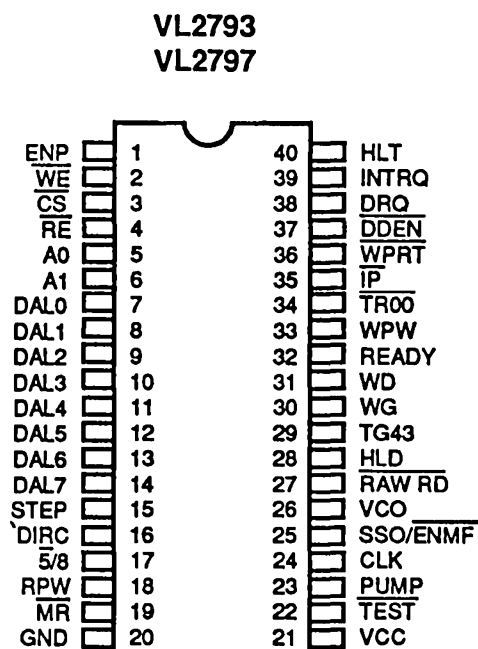
made as close as possible with the computer interface, instruction set, and I/O registers being identical. Also, head load control is identical. In each case, the actual pin assignments vary by only a few pins from any one to another.

The processor interface consists of an 8-bit bidirectional bus for data, status, and control word transfers. The VL279X is set up to operate on a multiplexed bus with other bus-oriented devices.

The VL279X is TTL compatible on all inputs and outputs. The outputs will drive one TTL load or three LS loads. The VL2793 is identical to the 2791 except the DAL lines are TRUE for systems that utilize true data busses.

The 2793/7 has a side select output for controlling double sided drives.

PIN DIAGRAM



ORDER INFORMATION

Part Number	Format	Package
VL2793-PC VL2793-CC	Single-Sided	Plastic DIP Ceramic DIP
VL2797-PC VL2797-CC	Double-Sided	Plastic DIP Ceramic DIP

Note: Operating temperature range is 0°C to +70°C.

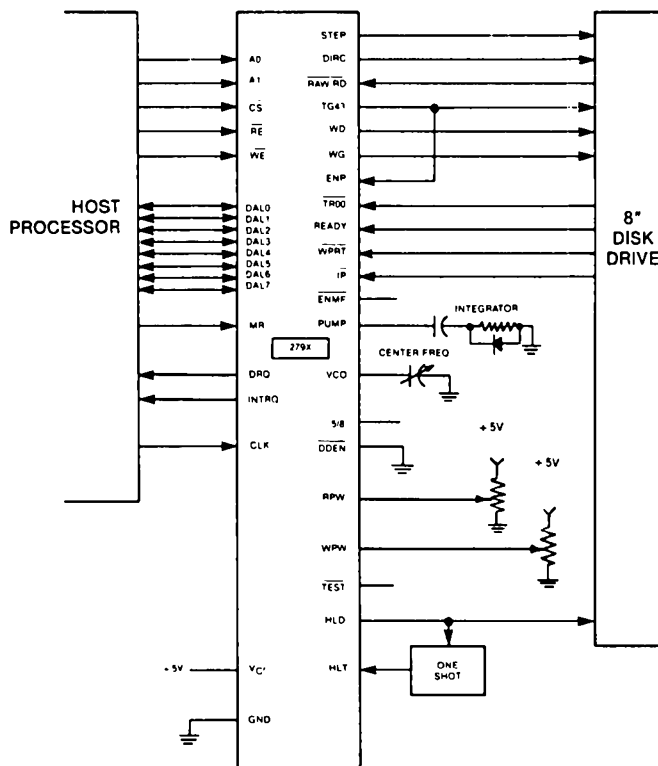
PIN DESCRIPTION

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION																									
1	ENABLE PRECOMP	ENP	A Logic high on this input enables write precompensation to be performed on double density Write Data output only.																									
19	MASTER RESET	MR	A logic low (50 microseconds min.) on this input resets the device and loads HEX 03 into the command register. The Not Ready (Status Bit 7) is reset during MR ACTIVE. When MR is brought to a logic high a RESTORE Command is executed, regardless of the state of the Ready signal from the drive. Also, HEX 01 is loaded into sector register.																									
20	POWER SUPPLIES	VSS	Ground																									
21		VCC	+5V ±5%																									
COMPUTER INTERFACE:																												
2	WRITE ENABLE	WE	A logic low on this input gates data on the DAL into the selected register when CS is low.																									
3	CHIP SELECT	CS	A logic low on this input selects the chip and enables computer communication with the device.																									
4	READ ENABLE	RE	A logic low on this input controls the placement of data from a selected register on the DAL when CS is low.																									
5, 6	REGISTER SELECT LINES	A0, A1	These inputs select the register to receive/transfer data on the DAL lines under RE and WE control: <table><tr><td>CS</td><td>A1</td><td>A0</td><td>RE</td><td>WE</td></tr><tr><td>0</td><td>0</td><td>0</td><td>Status Reg</td><td>Command Reg</td></tr><tr><td>0</td><td>0</td><td>1</td><td>Track Reg</td><td>Track Reg</td></tr><tr><td>0</td><td>1</td><td>0</td><td>Sector Reg</td><td>Sector Reg</td></tr><tr><td>0</td><td>1</td><td>1</td><td>Data Reg</td><td>Data Reg</td></tr></table>	CS	A1	A0	RE	WE	0	0	0	Status Reg	Command Reg	0	0	1	Track Reg	Track Reg	0	1	0	Sector Reg	Sector Reg	0	1	1	Data Reg	Data Reg
CS	A1	A0	RE	WE																								
0	0	0	Status Reg	Command Reg																								
0	0	1	Track Reg	Track Reg																								
0	1	0	Sector Reg	Sector Reg																								
0	1	1	Data Reg	Data Reg																								
7-14	DATA ACCESS LINES	DAL0-DAL7	Eight bit bi-directional bus used for transfer of commands, status, and data. These lines are inverted (active low) on VL279X.																									
24	CLOCK	CLK	This input requires a free-running 50% duty cycle square wave clock for internal timing reference, 2 MHz ± 1% for 8" drives, 1 MHz ± 1% for mini-floppies.																									
38	DATA REQUEST	DRQ	This output indicates that the Data Register contains assembled data in Read operations, or the DR is empty in Write operations. This signal is reset when serviced by the computer through reading or loading the DR.																									
39	INTERRUPT REQUEST	INTRQ	This output is set at the completion of any command and is reset when the Status register is read or the Command register is written to.																									
FLOPPY DISK INTERFACE:																												
15	STEP	STEP	The step output contains a pulse for each step.																									
16	DIRECTION	DIRC	Direction Output is active high when stepping in, active low when stepping out.																									
17	5¼," 8" SELECT	5/8	This input selects the internal VCO frequency for use with 5¼" drives or 8" drives.																									
18	READ PULSE WIDTH	RPW	An external potentiometer tied to this input controls the phase comparator within the data separator.																									
22	TEST	TEST	A logic low on this input allows adjustment of external resistors by enabling internal signals to appear on selected pins.																									

PIN DESCRIPTION (Continued)

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
23	PUMP	PUMP	High-Impedance output signal which is forced high or low to increase/decrease the VCO frequency.
25	ENABLE MINI-FLOPPY (2793)	$\overline{\text{ENMF}}$	A logic low on this input enables an internal $\div 2$ of the Master Clock. This allows both 5¼" and 8" drive operation with a single 2 MHz clock. For a 1 MHz clock on Pin 24, this line must be left open or tied to a Logic 1.
25	SIDE SELECT OUTPUT (2797)	SSO	The logic level of the Side Select Output is directly controlled by the 'S' flag in Type II or III commands. When $U = 1$, SSO is set to a logic 1. When $U = 0$, SSO is set to a logic 0. The SSO is compared with the side information in the Sector I.D. Field. If they do not compare Status Bit 4 (RNF) is set. The Side Select Output is only updated at the beginning of a Type II or III command. It is forced to a logic 0 upon a MASTER RESET condition.
26	VOLTAGE-CONTROLLED OSCILLATOR	VCO	An external capacitor tied to this pin adjusts the VCO center frequency.
27	$\overline{\text{RAW READ}}$	$\overline{\text{RAW READ}}$	The data input signal directly from the drive. This input shall be a negative pulse for each recorded flux transition.
28	HEAD LOAD	HLD	The HLD output controls the loading of the Read-Write head against the media.
29	TRACK GREATER THAN 43	TG43	This output informs the drive that the Read/Write head is positioned between tracks 44-76. This output is valid only during Read and Write Commands.
30	WRITE GATE	WG	This output is made valid before writing is to be performed on the diskette.
31	WRITE DATA	WD	MFM or FM output pulse per flux transition. WD contains the unique Address marks as well as data and clock in both FM and MFM formats.
32	READY	READY	This input indicates disk readiness and is sampled for a logic high before Read or Write commands are performed. If Ready is low the Read or Write operation is not performed and an interrupt is generated. Type I operations are performed regardless of the state of Ready. The Ready input appears in inverted format as Status Register bit 7.
33	WRITE PRECOMP WIDTH	WPW	An external potentiometer tied to this input controls the amount of delay in Write precompensation mode.
34	$\overline{\text{TRACK 00}}$	$\overline{\text{TR00}}$	This input informs the VL279X that the Read/Write head is positioned over Track 00.
35	$\overline{\text{INDEX PULSE}}$	$\overline{\text{IP}}$	This input informs the VL279X when the index hole is encountered on the diskette.
36	$\overline{\text{WRITE PROTECT}}$	$\overline{\text{WPRT}}$	This input is sampled whenever a Write Command is received. A logic low terminates the command and sets the Write Protect Status bit.
37	$\overline{\text{DOUBLE DENSITY}}$	$\overline{\text{DDEN}}$	This input pin selects either single or double density operation. When $\overline{\text{DDEN}} = 0$, double density is selected. When $\overline{\text{DDEN}} = 1$, single density is selected.
40	HEAD LOAD TIMING	HLT	When a logic high is found on the HLT input the head is assumed to be engaged. It is typically derived from a 1 shot triggered by HLD.

Figure 1.



APPLICATIONS

**8" FLOPPY AND 5¼" MINI FLOPPY CONTROLLER
SINGLE OR DOUBLE DENSITY
CONTROLLER/FORMATTER**

The VL279X Family are MOS/LSI devices which perform the functions of a Floppy Disk Controller/Formatter. Software compatible with its predecessor, the FD179X, the device also contains a high performance Phase-Lock-Loop Data Separator as well as Write Precompensation Logic.

When operating in Double Density mode, Write Precompensation may be enabled, its value predetermined by an external potentiometer. An on-chip VCO and phase comparator allows adjustable frequency range for 5¼" or 8" Floppy Disk interfacing.

The VL279X is fabricated in NMOS silicon gate technology and available in a 40 pin dual-in-line package.

FEATURES	2793	2797
Single Density (FM)	X	X
Double Density (MFM)	X	X
True Data Bus	X	X
Inverted Data Bus		
Side Select Out		X
Internal CLK Divide	X	

ORGANIZATION

The Floppy Disk Formatter block diagram is illustrated on page 5. The primary sections include the parallel processor interface and the Floppy Disk interface.

Data Shift Register — This 8-bit register assembles serial data from the Read Data input (RAW READ) during Read operations and transfers serial data to the Write Data output during Write operations.

Data Register — This 8-bit register is used as a holding register during Disk Read and Write operations in Disk Read operations the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In Disk Write operations information is transferred in parallel from the Data Register to the Data Shift Register.

When executing the Seek command the Data Register holds the address of the desired Track position. This register is loaded from the DAL and gated onto the DAL under processor control.

Track Register — This 8-bit register holds the track number of the current Read/Write head position. It is incremented by one every time the head is stepped in (towards track 76) and decremented by one when the head is stepped out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during disk Read, Write and Verify operations. The Track Register can be loaded from or transferred to the DAL. This Register should not be loaded when the device is busy.

Sector Register (SR) — This 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk Read or Write operations. The Sector Register contents can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

Command Register (CR) — This 8-bit register holds the command presently being executed. This register should not be loaded when the device is busy unless the new command is a force interrupt. The command register can be loaded from the DAL, but not read onto the DAL.

Status Register (STR) — This 8-bit register holds device Status information. The meaning of the Status bits is a function of the type of command previously executed. This register can be read onto the DAL, but not loaded from the DAL.

CRC Logic — This logic is used to check or to generate the 16-bit Cyclic Redundancy Check (CRC). The polynomial is: $G(x) = x^{16} + x^{12} + x^5 + 1$.

The CRC includes all information starting with the address mark and up to the CRC characters. The CRC register is preset to ones prior to data being shifted through the circuit.

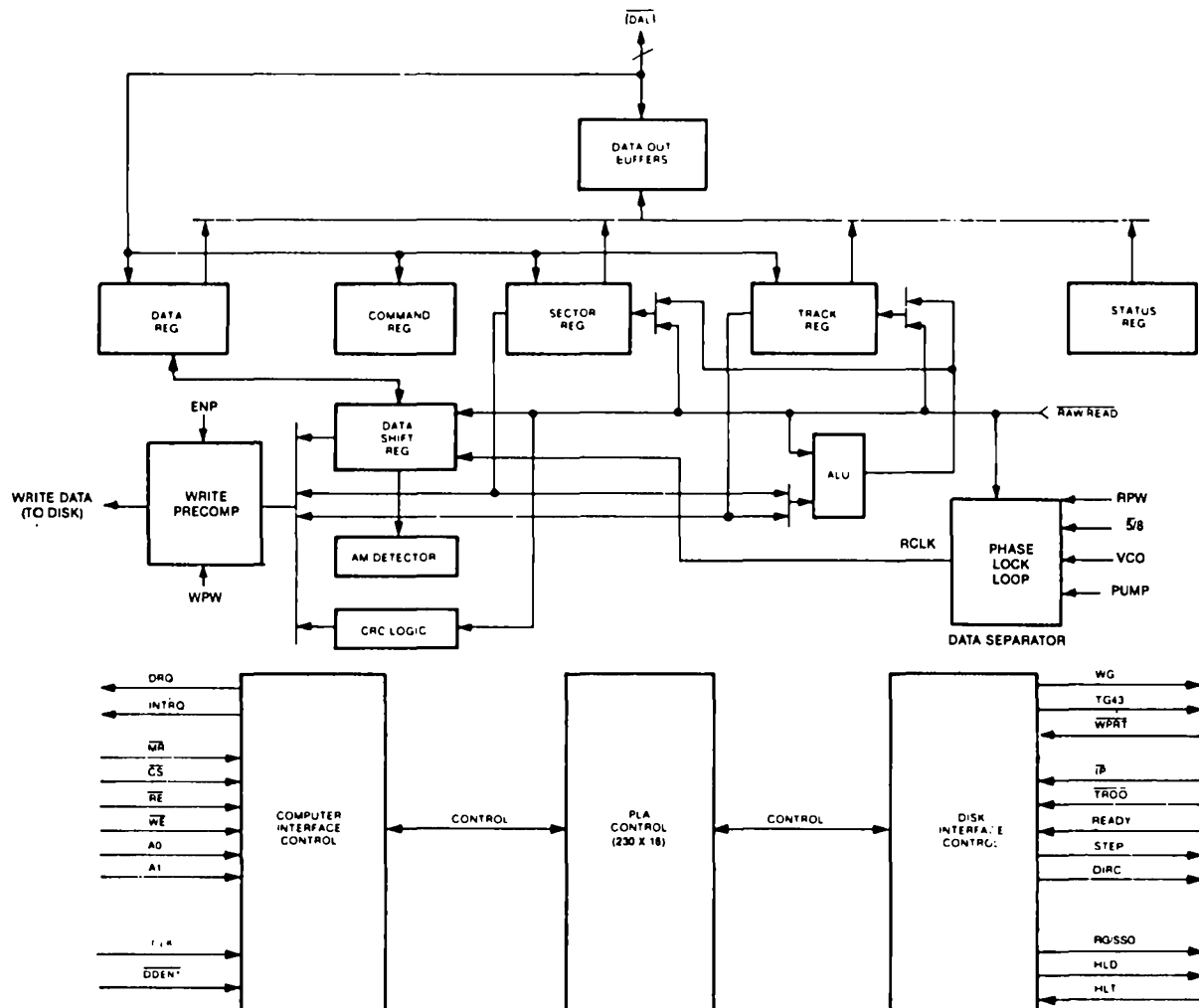
Arithmetic/Logic Unit (ALU) — The ALU is a serial comparator, incrementer, and decrements and is used for register modification and comparisons with the disk recorded ID field.

Timing and Control — All computer and Floppy Disk interface controls are generated through this logic. The internal device timing is generated from an external crystal clock.

AM Detector — The address mark detector detects ID, data and index address marks during read and write operations.

Write Precompensation — enables write precompensation to be performed on the Write Data output.

VL279X BLOCK DIAGRAM



Data Separator — a high performance Phase-Lock-Loop Data Separator with on-chip VCO and phase comparator allows adjustable frequency range for 5¼" or 8" Floppy Disk interfacing.

PROCESSOR INTERFACE

The interface to the processor is accomplished through the eight Data Access Lines (DAL) and associated control signals. The DAL are used to transfer Data, Status, and Control words out of, or into the VL279X. The DAL are three state buffers that are enabled as output drivers when Chip Select (\overline{CS}) and Read Enable (\overline{RE}) are active (low logic state) or act as input receivers when \overline{CS} and Write Enable (\overline{WE}) are active.

When transfer of data with the Floppy Disk Controller is required by the host processor, the device address is decoded and $\overline{\text{CS}}$ is made low. The address bits A1 and A0, combined with the signals $\overline{\text{RE}}$ during a Read operation or $\overline{\text{WE}}$ during a Write operation are interpreted as selecting the following registers:

A1	A0	READ (RE)	WRITE (WE)
0	0	Status Register	Command Register
0	1	Track Register	Track Register
1	0	Sector Register	Sector Register
1	1	Data Register	Data Register

During Direct Memory Access (DMA) types of data transfers between the Data Register of the VL279X and the processor, the Data Request (DRQ) output is used in Data Transfer control. This signal also appears as status bit 1 during Read and Write operations.

On Disk Read operations the Data Request is activated (set high) when an assembled serial input byte is transferred in parallel to the Data Register. This bit is cleared when the Data Register is read by the processor. If the Data Register is read after one or more characters are lost, by having new data transferred into the register prior to processor readout, the Lost Data bit is set in the Status Register. The Read operation continues until the end of sector is reached.

On Disk Write operations the data Request is activated when the Data Register transfers its contents to the Data Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor. If new data is not loaded at the time the next serial byte is required by the Floppy Disk, a byte of zeroes is written on the diskette and the Lost Data bit is set in the Status Register.

At the completion of every command an INTRQ is generated. INTRQ is reset by either reading the status register or by loading the command register with a new command. In addition, INTRQ is generated if a Force Interrupt command condition is met.

The 279X has two modes of operation according to the state of $\overline{\text{DDEN}}$ (Pin 37). When $\overline{\text{DDEN}} = 1$, Single Density (FM) is selected. When $\overline{\text{DDEN}} = 0$, Double Density (MFM) is selected. In either case, the CLK input (Pin 24) is set at 2 MHz for 8" drives or 1 MHz for 5¼" drives.

On the 2791/2793, the $\overline{\text{ENMF}}$ input (Pin 25) can be used for controlling both 5¼" and 8" drives with a single 2 MHz clock. When $\overline{\text{ENMF}} = 0$, an internal $\div 2$ of the CLK is performed. When $\overline{\text{ENMF}} = 1$, no divide takes place. This allows the use of a 2 MHz clock for both 5¼" and 8" configurations.

The internal VCO frequency must also be set to the proper value. The $\overline{5/8}$ input (Pin 17) is used to select data separator operation by internally dividing the Read Clock. When $\overline{5/8} = 0$, 5¼" data separation is selected; when $\overline{5/8} = 1$, 8" drive data separation is selected.

CLOCK (24)	$\overline{\text{ENMF}}$ (25)	$\overline{5/8}$ (17)	DRIVE
2 MHz	1	1	8"
2 MHz	0	0	5¼"
1 MHz	1	0	5¼"

FUNCTIONAL DESCRIPTION

The VL279X is software compatible with the FD179X series of Floppy Disk Controllers. Commands, status, and data transfers are performed in the same way. Software generated for the 179X can be transferred to a 279X system without modification.

In addition to the 179X, the 279X contains an internal Data Separator and Write precompensation circuit. The $\overline{\text{TEST}}$ (Pin 22) line is used to adjust both data separator and precompensation. When $\overline{\text{TEST}} = 0$, the WD (Pin 31) line is internally connected to the output of the write precomp one-shot. Adjustment of the WPW (Pin 33) line can then be accomplished. A second one-shot tracks the precomp setting at approximately 3:1 to insure adequate Write Data pulse widths to meet drive specifications.

Similarly, Data separation is also adjusted with $\overline{\text{TEST}} = 0$. The TG43 (Pin 29) line is internally connected to the output of the read data one-shot, which is adjusted via the RPW (Pin 18) line. The DIRC (Pin 16) line contains the Read Clock output (.5 MHz for 8" drives). The VCO Trimming capacitor (Pin 26) is adjusted for center frequency.

Internal timing signals are used to generate pulses during the adjustment mode so that these adjustments can be made while the device is in-circuit. The $\overline{\text{TEST}}$ line also contains a pull-up resistor, so adjustments can be performed simply by grounding the $\overline{\text{TEST}}$ pin, overriding the pull-up. The $\overline{\text{TEST}}$ pin cannot be used to disable stepping rates during operation as its function is quite different from the 179X.

Other pins on the device also include pull-up resistors and may be left open to satisfy a Logic 1 condition. These are: ENP, $\overline{5/8}$, $\overline{\text{ENMF}}$, $\overline{\text{WPRT}}$, $\overline{\text{DDEN}}$, HLT, TEST, and $\overline{\text{MR}}$.

GENERAL DISK READ OPERATIONS

Sector lengths of 128, 256, 512 or 1024 are obtainable in either FM or MFM formats. For FM, $\overline{\text{DDEN}}$ should be placed to logical "1." For MFM formats, $\overline{\text{DDEN}}$ should be

Sector Length Table*

Sector Length Field (hex)	Number of Bytes in Sector (decimal)
00	128
01	256
02	512
03	1024

*2793/97 may vary — see command summary.

placed to a logical "0." Sector lengths are determined at format time by the fourth byte in the "ID" field.

The VL279X recognizes tracks and sectors numbered 00-FFX. However, due to programming restrictions, only tracks and sectors 00 thru F4 can be formatted.

GENERAL DISK WRITE OPERATION

When writing is to take place on the diskette the Write Gate (WG) output is activated, allowing current to flow into the Read/Write head. As a precaution to erroneous writing the first data byte must be loaded into the Data Register in response to a Data Request from the 279X before the Write Gate signal can be activated.

Writing is inhibited when the Write Protect input is a logic low, in which case any Write command is immediately terminated, an interrupt is generated and the Write Protect status bit is set.

For write operations, the 279X provides Write Gate (Pin 30) and Write Data (Pin 31) outputs. Write data consists of a series of pulses set to a width approximately three times greater than the precomp adjustment. Write Data provides the unique address marks in both formats.

READY

Whenever a Read or Write command (Type II or III) is received the 279X samples the Ready input. If this input is logic low the command is not executed and an interrupt is generated. All Type I commands are performed regardless of the state of the Ready input. Also, whenever a Type II or III command is received, the TG43 signal output is updated. TG43 may be tied to ENP to enable write precompensation on tracks 44-76.

COMMAND DESCRIPTION

The VL279X will accept eleven commands. Command words should only be loaded in the Command Register when the Busy status bit is off (Status bit 0). The one exception is the Force interrupt command. Whenever a command is being executed, the Busy status bit is set. When a command is completed, an interrupt is generated and the Busy status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault free. For ease of discussion, commands are divided into four types. Commands and types are summarized in Table 1.



TABLE 1. COMMAND SUMMARY

A. Commands for Model 2793

B. Commands for Model 2797

Type	Command	Bits								Bits							
		7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r1	r0	0	0	0	0	h	V	r1	r0
I	Seek	0	0	0	1	h	V	r1	r0	0	0	0	1	h	V	r1	r0
I	Step	0	0	1	T	h	V	r1	r0	0	0	1	T	h	V	r1	r0
I	Step-in	0	1	0	T	h	V	r1	r0	0	1	0	T	h	V	r1	r0
I	Step-out	0	1	1	T	h	V	r1	r0	0	1	1	T	h	V	r1	r0
II	Read Sector	1	0	0	m	S	E	C	0	1	0	0	m	L	E	U	0
II	Write Sector	1	0	1	m	S	E	C	a0	1	0	1	m	L	E	U	a0
III	Read Address	1	1	0	0	0	E	0	0	1	1	0	0	0	E	U	0
III	Read Track	1	1	1	0	0	E	0	0	1	1	1	0	0	E	U	0
III	Write Track	1	1	1	1	0	E	0	0	1	1	1	1	0	E	U	0
IV	Force Interrupt	1	1	0	1	l3	l2	l1	l0	1	1	0	1	l3	l2	l1	l0

TABLE 2. FLAG SUMMARY

Command Type	Bit No(s)		Description																				
I	0, 1	r1 r0 = Stepping Motor Rate See Table 3 for Rate Summary																					
I	2	V = Track Number Verify Flag	V = 0, No verify V = 1, Verify on destination track																				
I	3	h = Head Load Flag	h = 0, Unload head at beginning h = 1, Load head at beginning																				
I	4	T = Track Update Flag	T = 0, No update T = 1, Update track register																				
II & III	0	a0 = Data Address Mark	a0 = 0, FB (DAM) a0 = 1, F8 (deleted DAM)																				
II	1	C = Side Compare Flag	C = 0, Disable side compare C = 1, Enable side compare																				
II & III	1	U = Update SSO	U = 0, Update SSO to 0 U = 1, Update SSO to 1																				
II & III	2	E = 15 MS Delay	E = 0, No. 15 MS delay E = 1, 15 MS delay (30 MS for 1 MHz)																				
II	3	S = Side Compare Flag	S = 0, Compare for side 0 S = 1, Compare for side 1																				
II	3	L = Sector Length Flag	<table><tr><td></td><td colspan="4">LSB's Sector Length in ID Field</td></tr><tr><td></td><td>00</td><td>01</td><td>10</td><td>11</td></tr><tr><td>L = 0</td><td>256</td><td>512</td><td>1024</td><td>128</td></tr><tr><td>L = 1</td><td>128</td><td>256</td><td>512</td><td>1024</td></tr></table>		LSB's Sector Length in ID Field					00	01	10	11	L = 0	256	512	1024	128	L = 1	128	256	512	1024
	LSB's Sector Length in ID Field																						
	00	01	10	11																			
L = 0	256	512	1024	128																			
L = 1	128	256	512	1024																			
II	4	m = Multiple Record Flag	m = 0, Single record m = 1, Multiple records																				
IV	0-3	l _x = Interrupt Condition Flags l ₀ = 1 Not Ready To Ready Transition l ₁ = 1 Ready To Not Ready Transition l ₂ = 1 Index Pulse l ₃ = 1 Immediate Interrupt, Requires A Reset* l _{3-l₀} = 0 Terminate With No Interrupt (INTRQ)																					

*NOTE: See Type IV Command Description for further information.

Write Precompensation

When operating in Double Density mode ($\overline{\text{DDEN}} = 0$), the 279X has the capability of providing a user-defined precompensation value for Write Data. An external potentiometer (10K) tied to the WPW signal (Pin 33) allows a setting of 100 to 300 ns from nominal.

Setting the Write precomp value is accomplished by forcing the $\overline{\text{TEST}}$ line (Pin 22) to a Logic 0. A stream of pulses can then be seen on the Write Data (Pin 31) line. Adjust the WPW Potentiometer for the desired pulse width. This adjustment may be performed in-circuit since Write Gate (Pin 30) is inactive while $\overline{\text{TEST}} = 0$.

Data Separation

The 279X can operate with either an external data separator or its own internal recovery circuits. The condition of the $\overline{\text{TEST}}$ line (Pin 22) in conjunction with $\overline{\text{MR}}$ (Pin 19) will select internal or external mode.

To program the 279X for external VCO, a $\overline{\text{MR}}$ pulse must be applied while $\overline{\text{TEST}} = 0$. A clock equivalent to eight times the data rate (e.g., 4.0 MHz for 8" Double Density) is applied to the VCO input (Pin 26). The feedback reference voltage is available on the Pump output (Pin 23) for external integration to control the VCO. $\overline{\text{TEST}}$ is returned to a Logic 1 for normal operation. Note: To maintain this mode, $\overline{\text{TEST}}$ must be held low whenever $\overline{\text{MR}}$ is applied.

For internal VCO operation, the $\overline{\text{TEST}}$ line must be high during the $\overline{\text{MR}}$ pulse, then set to a Logic 0 for the adjustment procedure.

A 50K Potentiometer tied to the RPW input (Pin 18) is used to set the internal Read Data pulse for proper phasing. With a scope on Pin 29 (TG43), adjust the RPW pulse for 1/8 of the data rate (250 ns for 8" Double Density). An external variable capacitor of 5-60 pf is tied to the VCO input (Pin 26) for adjusting center frequency. With a frequency counter on Pin 16 (DIRC) adjust the trimmer cap to yield the appropriate Data Rate (500 KHz for 8" Double Density). The $\overline{\text{DDEN}}$ line must be low while the 5/8 line is held high or the adjustment times above will be doubled.

After adjustments have been made, the $\overline{\text{TEST}}$ pin is returned to a Logic 1 and the device is ready for operation. Adjustments may be made in-circuit since the DIRC and TG43 lines may toggle without affecting the drive.

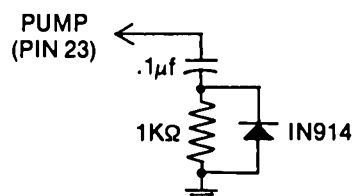
The PUMP output (Pin 23) consists of positive and negative pulses, which their duration is equivalent to the phase difference of incoming Data vs. VCO frequency. This signal is internally connected to the VCO input, but a Filter is needed to connect these pulses to a slow moving DC voltage.

The internal phase-detector is unsymmetrical for a random distribution of data pulses by a factor of two, in favor of a PUMP UP condition. Therefore, it is desirable to have a PUMP DOWN twice as responsive to prevent run-away during a lock attempt.

A first order lag-lead filter can be used at the PUMP output (Pin 23). This filter controls the instantaneous response of the VCO to bit-shifted data (jitter) as well as the response to normal frequency shift, i.e., the lock-up time. A balance

must be accomplished between the two conditions to inhibit over-responsiveness to jitter and to prevent an extremely wide lock-up response, leading to PUMP run-away. The filter affects these two reactions in mutually opposite directions.

The following Filter Circuit is recommended for 8" FM/MFM:



Since 5 1/4" Drives operate at exactly one-half the data rate (250 Kb/sec) the above capacitor should be doubled to .2 or .22µf.

TYPE I COMMANDS

The Type I Commands include the Restore, Seek, Step, Step-in, and Step-Out commands. Each of the Type I Commands contains a rate field (r0 r1), which determines the stepping motor rate as defined in Table 3.

A 2µs (MFM) or 4 µs (FM) pulse is provided as an output to the drive. For every step pulse issued, the drive moves one track location in a direction determined by the direction output. The chip will step the drive in the same direction it last stepped unless the command changes the direction.

The Direction signal is active high when stepping in and low when stepping out. The Direction signal is valid before the first stepping pulse is generated.

The rates (shown in Table 3) can be applied to a Step-Direction Motor through the device interface.

TABLE 3. STEPPING RATES

CLK		2 MHz	1 MHz
R1	R0	$\overline{\text{TEST}} = 1$	$\overline{\text{TEST}} = 1$
0	0	3 ms	6 ms
0	1	6 ms	12 ms
1	0	10 ms	20 ms
1	1	15 ms	30 ms

After the last directional step an additional 15 milliseconds of head settling time takes place if the Verify flag is set in Type I commands. Note that this time doubles to 30 ms for a 1 MHz clock. There is also a 15 ms head settling time if the E flag is set in any Type II or III command.

When a Seek, Step or Restore command is executed an optional verification of Read-Write head position can be performed by setting bit 2 (V = 1) in the command word to a logic 1. The verification operation begins at the end of the 15 millisecond settling time after the head is loaded against the media. The track number from the first encountered ID

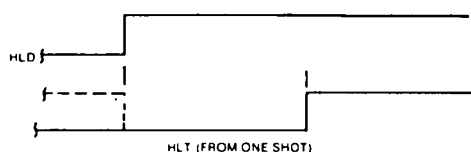
Field is compared against the contents of the Track Register. If the track numbers compare and the ID Field Cyclic Redundancy Check (CRC) is correct, the verify operation is complete and an INTRQ is generated with no errors. If there is a match but not a valid CRC, the CRC error status bit is set (Status bit 3), and the next encountered ID field is read from the disk for the verification operation.

The VL279X must find an ID field with correct track number and correct CRC within 5 revolutions of the media; otherwise the seek error is set and an INTRQ is generated. If $V = 0$, no verification is performed.

The Head Load (HLD) output controls the movement of the read/write head against the media. HLD is activated at the beginning of a Type I command if the h flag is set ($h = 1$), at the end of the Type I command if the verify flag ($V = 1$), or upon receipt of any Type II or III command. Once HLD is active it remains active until either a Type I command is received with ($h = 0$ and $V = 0$); or if the 279X is in an idle state (non-busy) and 15 index pulses have occurred.

Head Load timing (HLT) is an input to the 279X which is used for the head engage time. When $HLT = 1$, the 279X assumes the head is completely engaged. The head engage time is typically 30 to 100 ms depending on drive. The low to high transition on HLD is typically used to fire a one shot. The output of the one shot is then used for HLT and supplied as an input to the 279X.

HEAD LOAD TIMING



When both HLD and HLT are true, the 279X will then read from or write to the media. The "and" of HLD and HLT appears as status Bit 5 in Type I status.

In summary for the Type I commands: if $h = 0$ and $V = 0$, HLD is reset. If $h = 1$ and $V = 0$, HLD is set at the beginning of the command and HLT is not sampled nor is there an internal 15 ms delay. If $h = 0$ and $V = 1$, HLD is set near the end of the command, an internal 15 ms occurs, and the 279X waits for HLT to be true. If $h = 1$ and $V = 1$, HLD is set at the beginning of the command. Near the end of the command, after all the steps have been issued, an internal 15 ms delay occurs and the 279X then waits for HLT to occur.

For Type II and III commands with E flag off, HLD is made active and HLT is sampled until true. With E flag on, HLD is made active; an internal 15 ms delay occurs and then HLT is sampled until true.

RESTORE (SEEK TRACK 0)

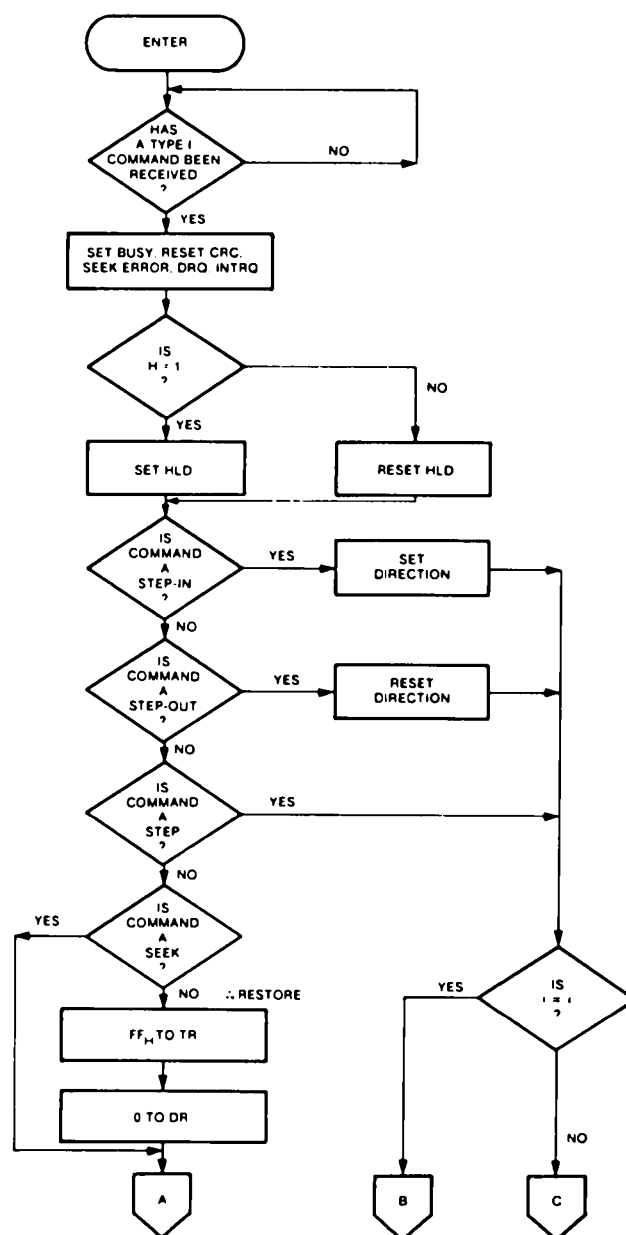
Upon receipt of this command the Track 00 ($\overline{TR00}$) input is sampled. If $\overline{TR00}$ is active low indicating the Read-Write head is positioned over track 0, the Track Register is loaded with zeroes and an interrupt is generated. If $\overline{TR00}$ is not

active low, stepping pulses at a rate specified by the $r1r0$ field are issued until the $\overline{TR00}$ input is activated. At this time the Track Register is loaded with zeroes and an interrupt is generated. If the $\overline{TR00}$ input does not go active low after 255 stepping pulses, the 279X terminates operation, interrupts, and sets the Seek error status bit. A verification operation takes place if the V flag is set. The h bit allows the head to be loaded at the start of command. Note that the Restore command is executed when \overline{MR} goes from an active to an inactive state.

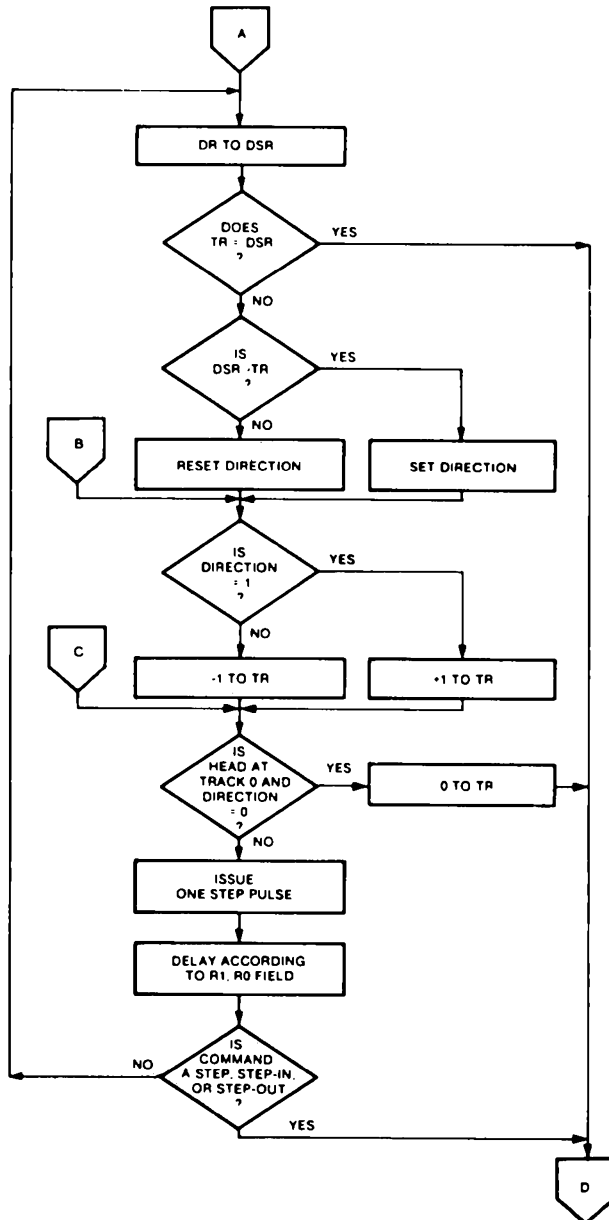
SEEK

This command assumes that the Track Register contains the track number of the current position of the Read-Write head and the Data Register contains the desired track number. The VL279X will update the Track register and issue stepping pulses in the appropriate direction until the

TYPE I COMMAND FLOW



TYPE I COMMAND FLOW



contents of the Track register are equal to the contents of the Data Register (the desired track location). A verification operation takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command. Note: When using multiple drives, the track register must be updated for the drive selected before seeks are issued.

STEP

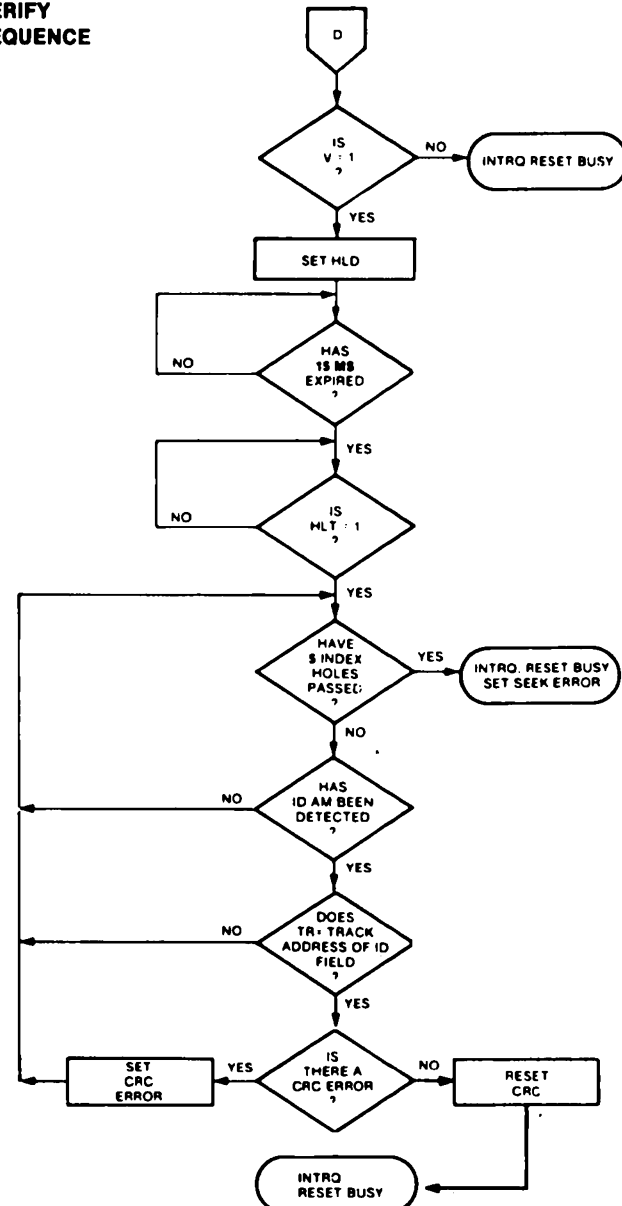
Upon receipt of this command, the 279X issues one stepping pulse to the disk drive. The stepping motor direction is the same as in the previous step command. After a delay determined by the r1r0 field, a verification takes place if the V flag is on. If the T flag is on, the Track Register is updated. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP-IN

Upon receipt of this command, the 279X issues one stepping pulse in the direction towards track 76. If the T flag is on, the Track Register is incremented by one. After a

TYPE I COMMAND FLOW

VERIFY SEQUENCE



NOTE: 1 MHz THERE IS A 10MS DELAY

delay determined by the r1r0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP-OUT

Upon receipt of this command, the 279X issues one stepping pulse in the direction towards track 0. If the T flag is on, the Track Register is decremented by one. After a delay determined by the r1r0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

EXCEPTIONS

On the 2797 device, the SSO output is not affected during Type I commands, and an internal side compare does not take place when the (V) Verify Flag is on.

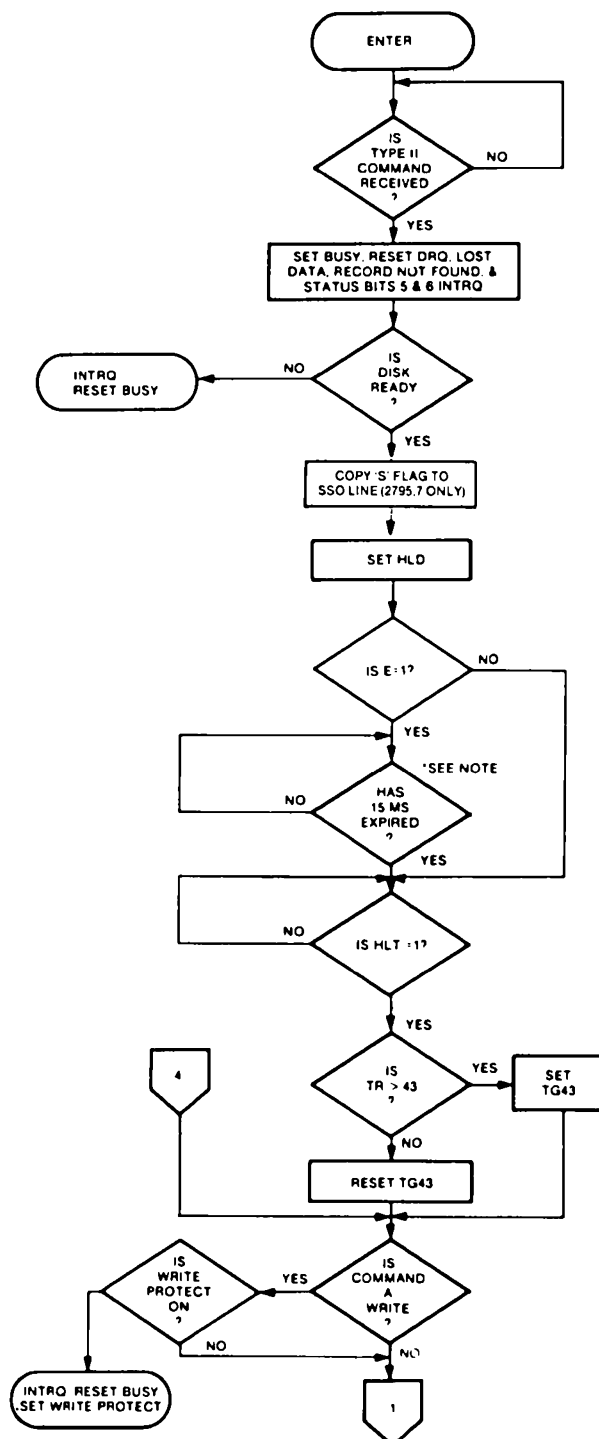
TYPE II COMMANDS

The Type II Commands are the Read Sector and Write Sector commands. Prior to loading the Type II Command into the Command Register, the computer must load the

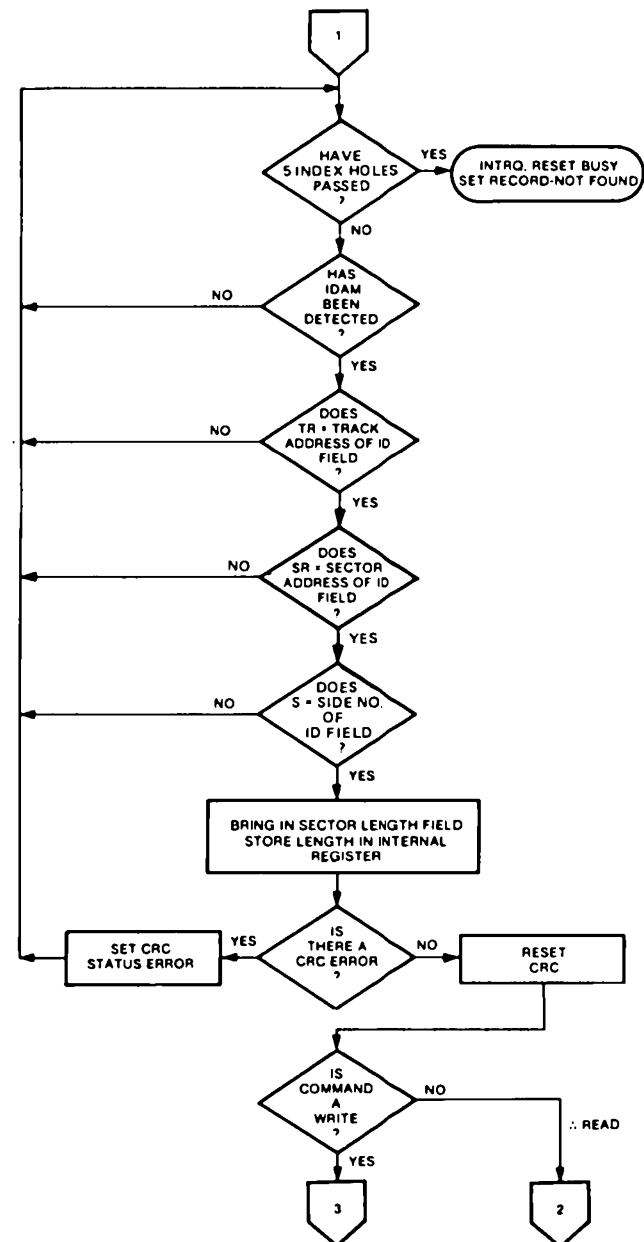
Sector Register with the desired sector number. Upon receipt of the Type II command, the busy status Bit is set. If the E flag = 1 (this is the normal case) HLD is made active and HLT is sampled after a 15 msec delay. If the E flag is 0, the head is loaded and HLT sampled with no 15 msec delay.

When an ID field is located on the disk, the 279X compares the Track Number on the ID field with the Track Register. If there is not a match, the next encountered ID field is read and a comparison is again made. If there was a match, the Sector Number of the ID field is compared with the Sector Register. If there is not a Sector match, the next encountered ID field is read off the disk and comparisons again made. If the ID field CRC is correct, the data field is then located and will be either written into, or read from

TYPE II COMMAND



TYPE II COMMAND

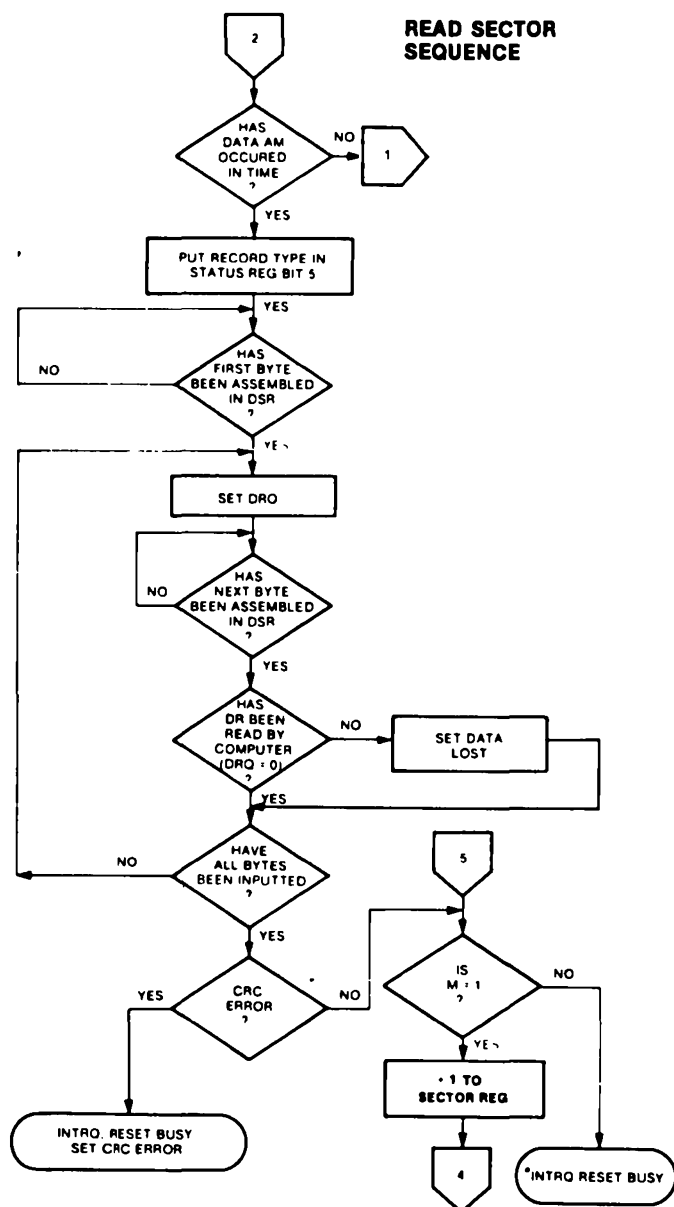


depending upon the command. The 279X must find an ID field with a Track number, Sector number, side number, and CRC within 5 revolutions of the disk; otherwise, the Record not found status bit is set (Status bit 4) and the command is terminated with an interrupt.

Each of the Type II Commands contains an (m) flag which determines if multiple records (sectors) are to be read or written, depending upon the command. If $m = 0$, a single sector is read or written and an interrupt is generated at the completion of the command. If $m = 1$, multiple records are read or written with the sector register internally updated so that an address verification can occur on the next record. The 279X will continue to read or write multiple records and update the sector register in numerical ascending sequence until the sector register exceeds the number of sectors on the track or until the Force Interrupt command is loaded into the Command Register, which terminates the command and generates an interrupt.

For example: If the 279X is instructed to read sector 27 and there are only 26 on the track, the sector register exceeds

TYPE II COMMAND



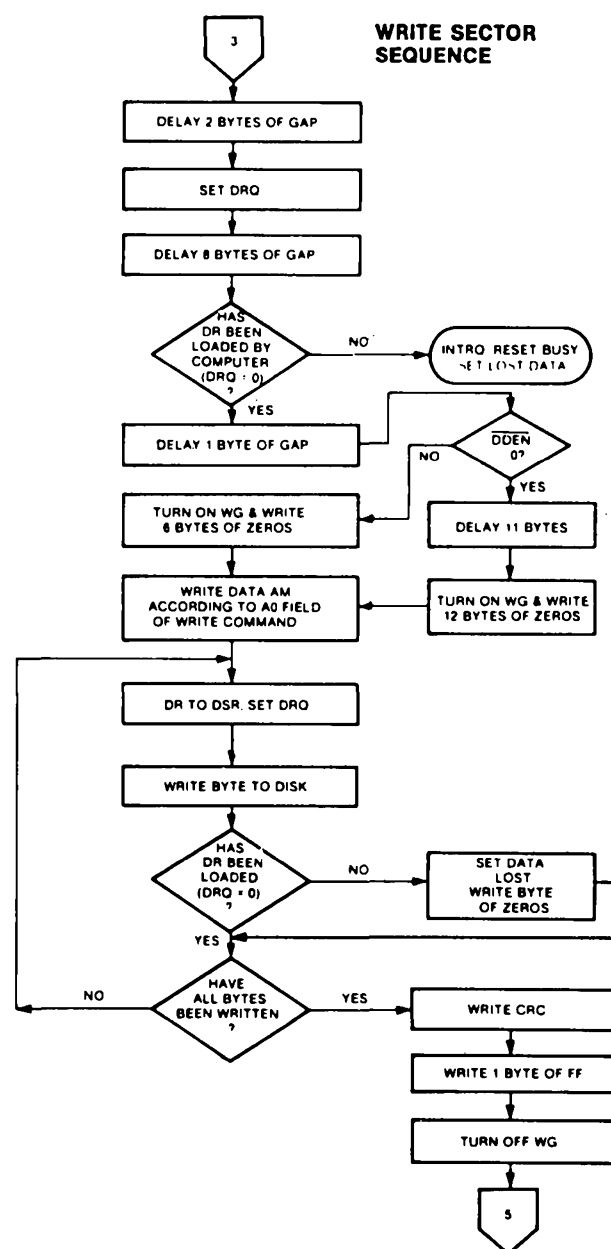
the number available. The 279X will search for 5 disk revolutions, interrupt out, reset busy, and set the record not found status bit.

The Type II commands for the 2793 also contain side select compare flags. When C = 0 (Bit 1) no side comparison is made. When C = 1, the LSB of the side number is read off the ID Field of the disk and compared with the contents of the (S) flag (Bit 3). If the S flag compares with the side number recorded in the ID field, the 279X continues with the ID search. If a comparison is not made within 5 index pulses, the interrupt line is made active and the Record-Not-Found status bit is set.

The Type II and III commands for the 2797 contain a side select flag (Bit 1). When U = 0, SSO is updated to 0. Similarly, U = 1 updates SSO to 1. The chip compares the SSO to the ID field. If they do not compare within 5 revolutions the interrupt line is made active and the RNF status bit is set.

The 2797 READ SECTOR and WRITE SECTOR com-

TYPE II COMMAND



mands include a 'L' flag. The 'L' flag, in conjunction with the sector length byte of the ID Field, allows different byte lengths to be implemented in each sector. For IBM compatibility, the 'L' flag should be set to a one.

READ SECTOR

Upon receipt of the Read Sector command, the head is loaded, the Busy status bit set, and when an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, the data field is presented to the computer. The Data Address Mark of the data field must be found within 30 bytes in single density and 43 bytes in double density of the last ID field CRC byte; if not, the ID field search is repeated.

When the first character or byte of the data field has been shifted through the DSR, it is transferred to the DR, and DRQ is generated. When the next byte is accumulated in the DSR, it is transferred to the DR and another DRQ is generated. If the Computer has not read the previous contents of the DR before a new character is transferred

that character is lost and the Lost Data Status bit is set. This sequence continues until the complete data field has been inputted to the computer. If there is a CRC error at the end of the data field, the CRC error status bit is set, and the command is terminated (even if it is a multiple sector command).

At the end of the Read operation, the type of Data Address Mark encountered in the data field is recorded in the Status Register (Bit 5) as shown:

**STATUS
BIT 5**

1	Deleted Data Mark
0	Data Mark

WRITE SECTOR

Upon receipt of the Write Sector command, the head is loaded (HLD active) and the Busy status bit is set. When an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, a DRQ is generated. The 279X counts off 11 bytes in single density and 22 bytes in double density from the CRC field and the Write Gate (WG) output is made active if the DRQ is serviced (i.e., the DR has been loaded by the computer). If DRQ has not been serviced, the command is terminated and the Lost Data status bit is set. If the DRQ has been serviced, the WG is made active and six bytes of zeroes in single density and 12 bytes in double density are then written on the disk. At this time the Data Address Mark is then written on the disk as determined by the $\alpha 0$ field of the command as shown below:

$\alpha 0$ Data Address Mark (Bit 0)

1	Deleted Data Mark
0	Data Mark

The 279X then writes the data field and generates DRQ's to the computer. If the DRQ is not serviced in time for continuous writing the Lost Data Status Bit is set and a byte of zeroes is written on the disk. The command is not terminated. After the last data byte has been written on the disk, the two-byte CRC is computed internally and written on the disk followed by one byte of FE in FM or in MFM. The WG output is then deactivated. For a 2 MHz clock the INTRQ will set 8 to 12 μ sec after the last CRC byte is written. For partial sector writing, the proper method is to write the data and fill the balance with zeroes. By letting the chip fill the zeroes, errors may be masked by the lost data status and improper CRC Bytes.

TYPES III COMMANDS

READ ADDRESS

Upon receipt of the Read Address command, the head is loaded and the Busy Status Bit is set. The next encountered ID field is then read in from the disk, and the six data bytes of the ID field are assembled and transferred to the DR, and a DRQ is generated for each byte. The six bytes of the ID field are shown below:

TRACK ADDR	SIDE NUMBER	SECTOR ADDRESS	SECTOR LENGTH	CRC 1	CRC 2
1	2	3	4	5	6

Although the CRC characters are transferred to the computer, the 279X checks for validity and the CRC error status bit is set if there is a CRC error. The Track Address of the ID field is written into the sector register so that a comparison can be made by the host. At the end of the operation an interrupt is generated and the Busy Status is reset.

READ TRACK

Upon receipt of the READ track command, the head is loaded, and the Busy Status bit is set. Reading starts with the leading edge of the first encountered index pulse and continues until the next index pulse. All Gap, Header, and data bytes are assembled and transferred to the data register and DRQ's are generated for each byte. The accumulation of bytes is synchronized to each address mark encountered. An interrupt is generated at the completion of the command.

This command has several characteristics which make it suitable for diagnostic purposes. They are: no CRC checking is performed; gap information is included in the data stream; the internal side compare is not performed; and the address mark detector is on for the duration of the command. Because the A.M. detector is always on, write splices or noise may cause the chip to look for an A.M. If an address mark does not appear on schedule with the Lost Data status flag being set.

The ID A.M., ID field, ID CRC bytes, DAM, Data and Data CRC Bytes for each sector will be correct. The Gap Bytes may be read incorrectly during write-splice time because of synchronization.

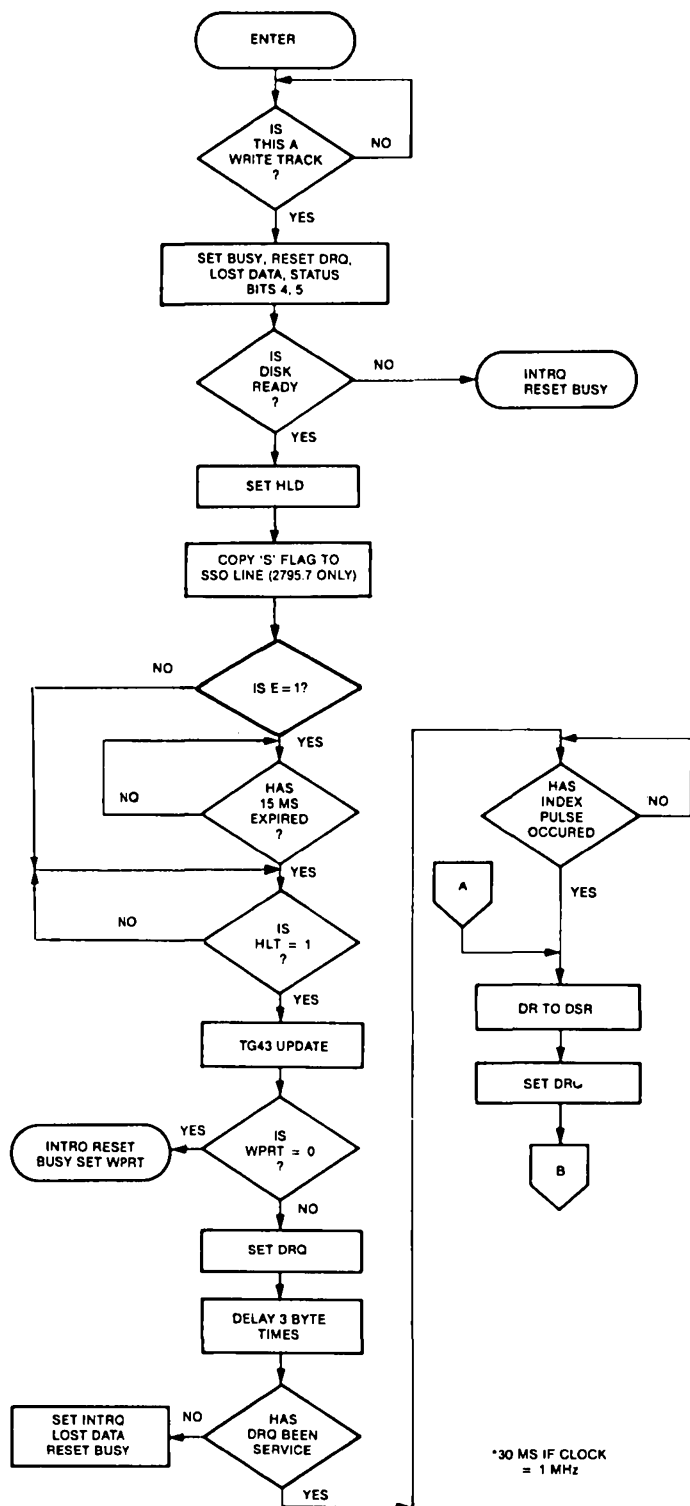
WRITE TRACK FORMATTING THE DISK

(Refer to section on Type III commands for flow diagrams.)

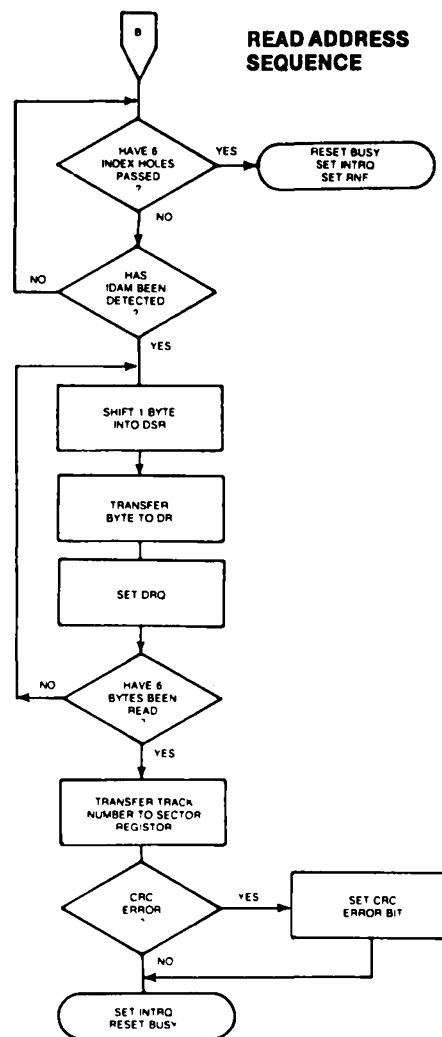
Formatting the disk is a relatively simple task when operating programmed I/O or when operating under DMA with a large amount of memory. Data and gap information must be provided at the computer interface. Formatting the disk is accomplished by positioning the RW head over the desired track number and issuing the Write Track command.

Upon receipt of the Write Track command, the head is loaded and the Busy Status bit is set. Writing starts with the leading edge of the first encountered index pulse and continues until the next index pulse, at which time the interrupt is activated. The Data Request is activated immediately upon receiving the command, but writing will not start until after the first byte has been loaded into the Data Register. If the DR has not been loaded by the time the index pulse is encountered the operation is terminated making the device Not Busy, the Lost Data Status Bit is set, and the interrupt is activated. If a byte is not present in the DR when needed, a byte of zeroes is substituted.

TYPE III COMMAND WRITE TRACK



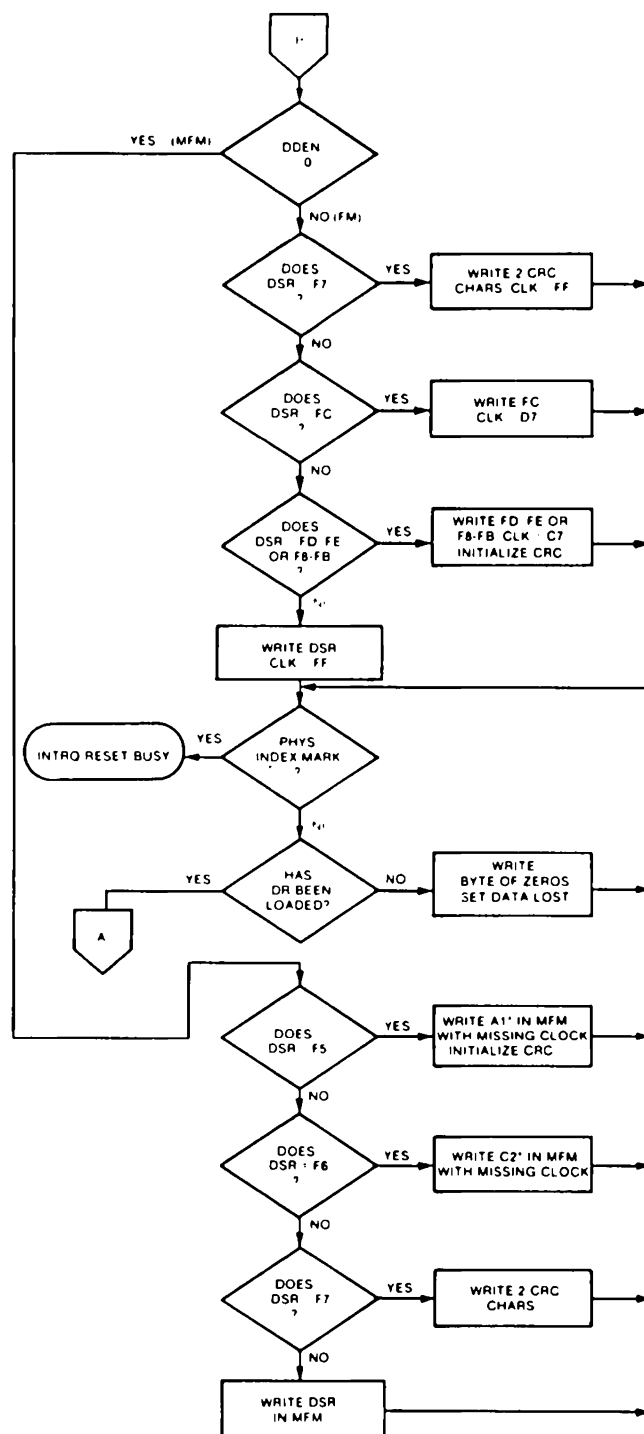
TYPE III COMMAND Read Track/Address



This sequence continues from one index mark to the next index mark. Normally, whatever data pattern appears in the data register is written on the disk with a normal clock pattern. However, if the 279X detects a data pattern of F5 thru FE in the data register, this is interpreted as data address marks with missing clocks or CRC generation.

The CRC generator is initialized when any data byte from F8 to FE is about to be transferred from the DR to the DSR

TYPE III COMMAND WRITE TRACK



CONTROL BYTES FOR INITIALIZATION

DATA PATTERN IN DR (HEX)	VL279X INTERPRETATION IN FM (DDEN = 1)	VL279X INTERPRETATION IN MFM (DDEN = 0)
00 thru F4	Write 00 thru F4 with CLK = FF	Write 00 thru F4, in MFM
F5	Not Allowed	Write A1* in MFM, Preset CRC
F6	Not Allowed	Write C2** in MFM
F7	Generate 2 CRC bytes	Generate 2 CRC bytes
F8 thru FB	Write F8 thru FB, Clk = C7, Preset CRC	Write F8 thru FB, in MFM
FC	Write FC with Clk = D7	Write FC in MFM
FD	Write FD with Clk = FF	Write FD in MFM
FE	Write FE, Clk = C7, Preset CRC	Write FE in MFM
FF	Write FF with Clk = FF	Write FF in MFM

* Missing clock transition between bits 4 and 5

** Missing clock transition between bits 3 and 4

or by receipt of F5 in MFM. An F7 pattern will generate two CRC characters in FM or MFM. As a consequence, the patterns F5 thru FE must not appear in the gaps, data fields, or ID fields. Also, CRC's must be generated by an F7 pattern.

Disks may be formatted in IBM 3740 or System 34 formats with sector lengths of 128, 256, 512, or 1024 bytes.

TYPE IV COMMANDS

The Forced Interrupt command is generally used to terminate a multiple sector read or write command or to insure Type I status in the status register. This command can be loaded into the command register at any time. If there is a current command under execution (busy status bit set)

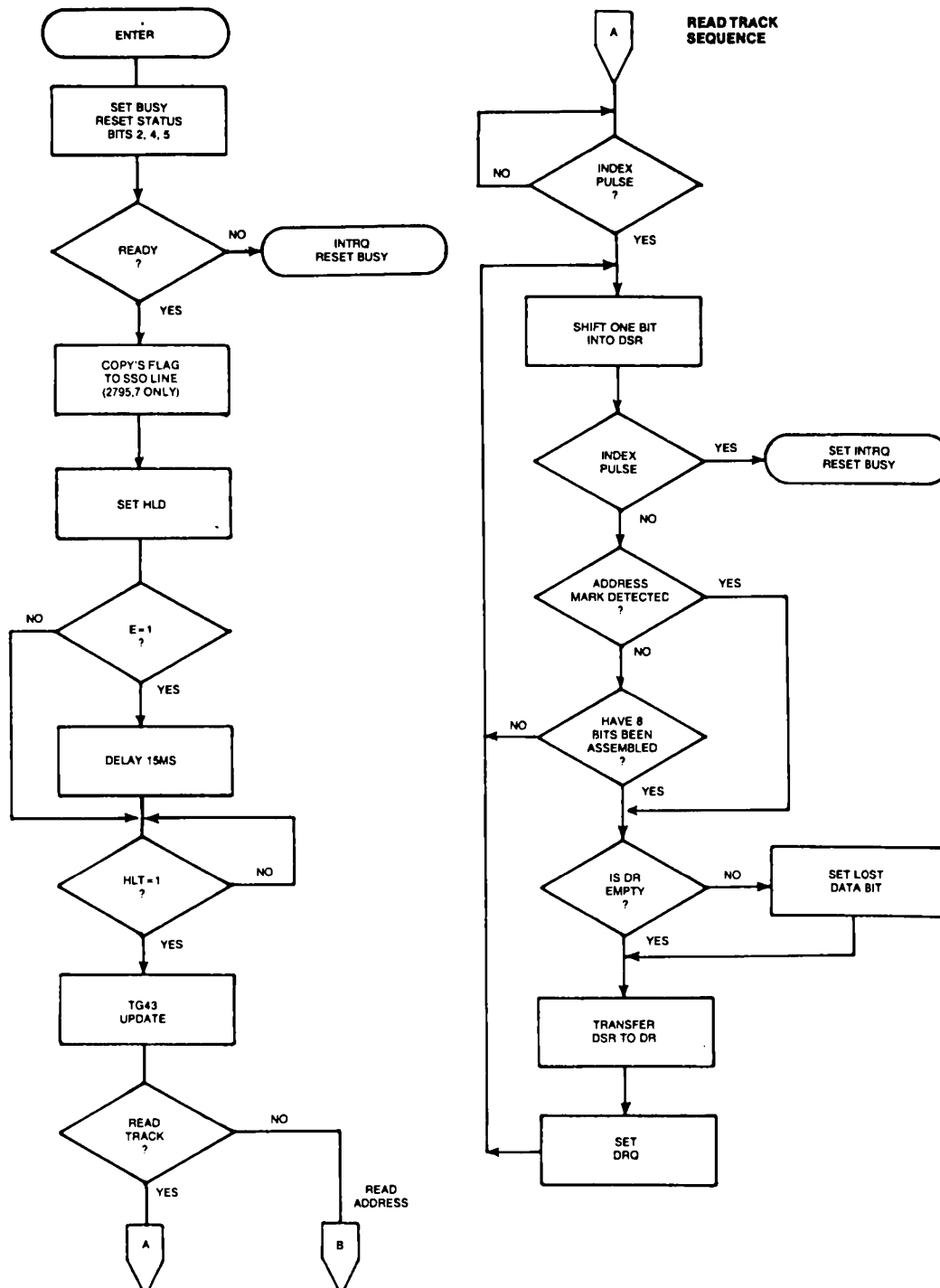
the command will be terminated and the busy status bit reset.

The lower four bits of the command determine the conditional interrupt as follows:

- I₀ = Not-Ready to Ready Transition
- I₁ = Ready to Not-Ready Transition
- I₂ = Every Index Pulse
- I₃ = Immediate Interrupt

The conditional interrupt is enabled when the corresponding bit positions of the command (I₃ - I₀) are set to a 1. Then, when the condition for interrupt is met, the INTRQ line will go high signifying that the condition specified has occurred. If I₃ - I₀ are all set to zero (HEX D0), no interrupt will occur but any command presently under execution will be immediately terminated. When using the Immediate

TYPE III COMMAND Read Track/Address



interrupt condition $I_3 = 1$), an interrupt will be immediately generated and the current command terminated. Reading the status or writing to the command register will not automatically clear the interrupt. The HEX D0 is the only command that will enable the immediate interrupt (HEX D8) to clear on a subsequent load command register or read status register operation. Follow a HEX D8 with D0 command.

Wait 8 micro sec (double density) or 16 micro sec (single density) before issuing a new command after issuing a forced interrupt (times double when clock = 1 MHz). Loading a new command sooner than this will nullify the forced interrupt.

Forced interrupt stops any command at the end of an internal micro-instruction and generates INTRQ when the specified condition is met. Forced interrupt will wait until ALU operations in progress are complete (CRC calculations, compares, etc.)

More than one condition may be set at a time. If for example, the READY TO NOT-READY condition ($I_1 = 1$) and the Every Index Pulse ($I_2 = 1$) are both set, the resultant command would be HEX "DA." The "OR" function is performed so that either a READY TO NOT-READY or the next Index Pulse will cause an interrupt condition.

STATUS REGISTER

Upon receipt of any command, except the Force Interrupt command, the Busy Status bit is set and the rest of the status bits are updated or cleared for the new command. If the Force Interrupt Command is received when there is a current command under execution, the Busy status bit is reset, and the rest of the status bits are unchanged. If the Force Interrupt command is received when there is not a current command under execution, the Busy Status bit is reset and the rest of the status bits are updated or cleared. In this case, Status reflects the Type I commands.

The user has the option of reading the status register through program control or using the DRQ line with DMA or interrupt methods. When the Data register is read the DRQ bit in the status register and the DRQ line are automatically reset. A write to the Data register also causes both DRQ's to reset.

The busy bit in the status may be monitored with a user program to determine when a command is complete, in lieu of using the INTRQ line. When using the INTRQ, a busy status check is not recommended because a read of the status register to determine the condition of busy will reset the INTRQ line.

The format of the Status Register is shown below:

(BITS)							
7	6	5	4	3	2	1	0
S7	S6	S5	S4	S3	S2	S1	S0

Status varies according to the type of command executed as shown in Table 4.

Because of internal sync cycles, certain time delays must be observed when operating under programmed I/O. They are: (times double when clock = 1 MHz)

Operation	Next Operation	Delay Req'd.	
		FM	MFM
Write to Command Reg.	Read Busy Bit (Status Bit 0)	12 μ s	6 μ s
Write to Command Reg.	Read Status Bits 1-7	28 μ s	14 μ s
Write Any Register	Read From Diff. Register	0	0

IBM 3740 FORMAT — 128 BYTES/SECTOR

Shown below is the IBM single-density format with 128 bytes/sector. In order to format a diskette, the user must issue the Write Track command, and load the data register with the following values. For every byte to be written, there is one Data Request.

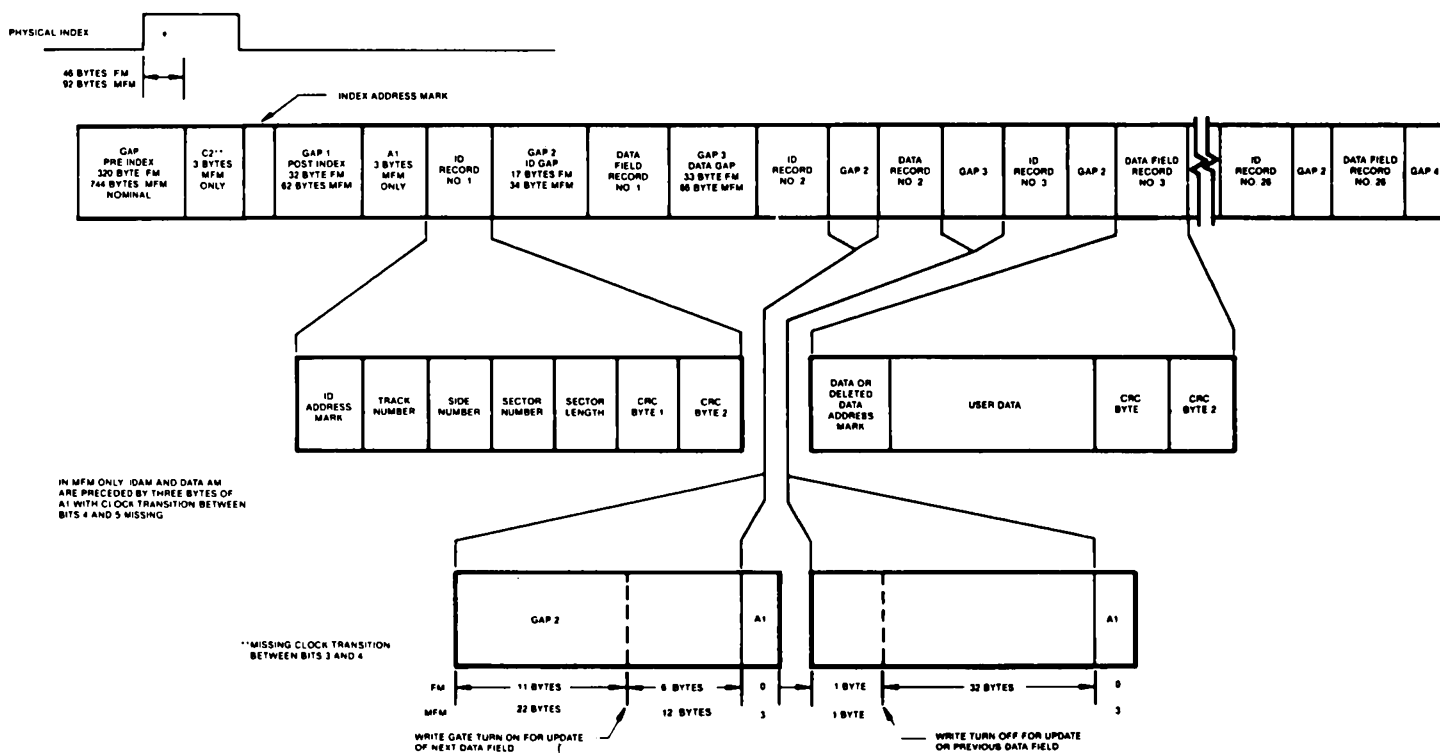
NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
40	FF (or 00) ³
6	00
1	FC (Index Mark)
1 26	FF (or 00)
6	00
1	FE (ID Address Mark)
1	Track Number
1	Side Number (00 or 01)
1	Sector Number (1 thru 1A)
1	00 (Sector Length)
1	F7 (2 CRC's written)
11	FF (or 00)
6	00
1	FB (Data Address Mark)
128	Data (IBM uses E5)
1	F7 (2 CRC's written)
27	FF (or 00)
2472	FF (or 00)

1. Write bracketed field 26 times
2. Continue writing until 279X interrupts out.
Approx. 247 bytes.
3. A '00' option is allowed.

IBM SYSTEM 34 FORMAT- 256 BYTES/SECTOR

Shown below is the IBM dual-density format with 256 bytes/sector. In order for format a diskette the user must issue the Write Track command and load the data register with the following values. For every byte to be written, there is one data request.

IBM TRACK FORMAT



NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
80	4E
12	00
3	F6 (Writes C2)
1	FC (Index Mark)
* 50	4E
12	00
3	F5 (Writes A1)
1	FE (ID Address Mark)
1	Track Number (0 thru 4C)
1	Side Number (0 or 1)
1	Sector Number (1 thru 1A)
1	01 (Sector Length)
1	F7 (2 CRCs written)
22	4E
12	00
3	F5 (Writes A1)
1	FB (Data Address Mark)
256	DATA
1	F7 (2 CRCs written)
54	4E
598**	4E

- * Write bracketed field 26 times
- ** Continue writing until 279X interrupts out.
Approx. 598 bytes.

1. NON-IBM FORMATS

Variations in the IBM formats are possible to a limited extent if the following requirements are met:

- 1) Sector size must be 128, 256, 512 of 1024 bytes.
- 2) Gap 2 cannot be varied from the IBM format.
- 3) 3 bytes of A1 must be used in MFM.

In addition, the Index Address Mark is not required for operation by the 279X. Gap 1, 3, and 4 lengths can be as short as 2 bytes for 279X operation, however PLL lock up time, motor speed variation, write splice area, etc. will add more bytes to each gap to achieve proper operation. It is recommended that the IBM format be used for highest system reliability.

GAP	FM	MFM
Gap I	16 bytes FF	32 bytes 4E
Gap II	11 bytes FF	22 bytes 4E
•	6 bytes 00	12 bytes 00
•		3 bytes A1
Gap III**	10 bytes FF	24 bytes 4E
	4 bytes 00	8 bytes 00
		3 bytes A1
Gap IV	16 bytes FF	16 bytes 4E

* Byte counts must be exact.

** Byte counts are minimum, except exactly 3 bytes of A1 must be written.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Voltage to any input with

respect to $V_{SS} = +7$ to $-0.5V$

Operating temperature = $0^{\circ}C$ to $70^{\circ}C$

Storage temperature = $-55^{\circ}C$ to $+125^{\circ}C$

NOTE: Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Electrical characteristics.

OPERATING CHARACTERISTICS (DC) $T_A = 0^{\circ}C$ to $70^{\circ}C$, $V_{SS} = 0V$, $V_{CC} = +5V \pm .25V$

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
I_{IL}	Input Leakage			10	μA	$V_{IN} = V_{CC}$
I_{OL}	Output Leakage			10	μA	$V_{OUT} = V_{CC}$
V_{IH}	Input High Voltage	2.0			V	
V_{IL}	Input Low Voltage			0.8	V	
V_{OH}	Output High Voltage	2.4			V	$I_O = -100\mu A$
V_{OL}	Output Low Voltage			0.45	V	$I_O = 1.6 mA$
V_{OHP}	Output High PUMP	2.2			V	$I_{OP} = -1.0 mA$
V_{OLP}	Output Low PUMP			0.2	V	$I_{OP} = +1.0 mA$
P_D	Power Dissipation			.75	W	All Outputs Open
R_{PU}	Internal Pull-up*	100		1700	μA	$V_{IN} = 0V$
I_{CC}	Supply Current		70	150	mA	All Outputs Open

* Internal Pull-up resistors on PINS 1, 17, 19, 22, 36, 37 and 40. Also pin 25 on 2793.

TIMING CHARACTERISTICS $T_A = 0^\circ\text{C to } 70^\circ\text{C}$, $V_{SS} = 0\text{V}$, $V_{CC} = +5\text{V} \pm .25\text{V}$

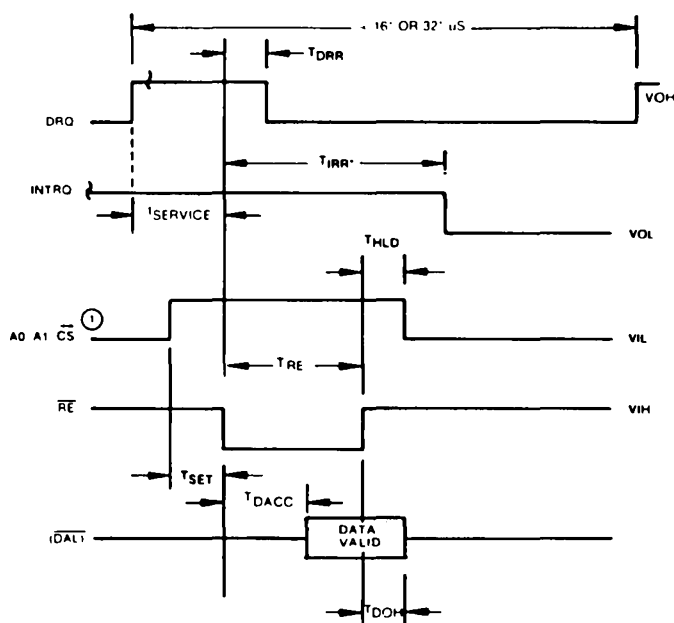
READ ENABLE TIMING

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
TSET	Setup ADDR & CS to \overline{RE}	50			nsec	$C_L = 50\text{ pf}$
THLD	Hold ADDR & CS from \overline{RE}	10			nsec	
TRE	\overline{RE} Pulse Width	200			nsec	
TDRR	DRQ Reset from \overline{RE}		100	200	nsec	See Note $C_L = 50\text{ pf}$ $C_L = 50\text{ pf}$
TIRR	INTRQ Reset from \overline{RE}		500	3000	nsec	
TDACC	Data Valid from \overline{RE}		100	200	nsec	
TDOH	Data Hold From \overline{RE}	20		150	nsec	

WRITE ENABLE TIMING

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
TSET	Setup ADDR & CS to \overline{WE}	50			nsec	See Note
THLD	Hold ADDR & CS from \overline{WE}	10			nsec	
TWE	\overline{WE} Pulse Width	200			nsec	
TDRR	DRQ Reset from \overline{WE}		100	200	nsec	
TIRR	INTRQ Reset from \overline{WE}		500	3000	nsec	
TDS	Data Setup to \overline{WE}	150			nsec	
TDH	Data Hold from \overline{WE}	50			nsec	

READ ENABLE TIMING

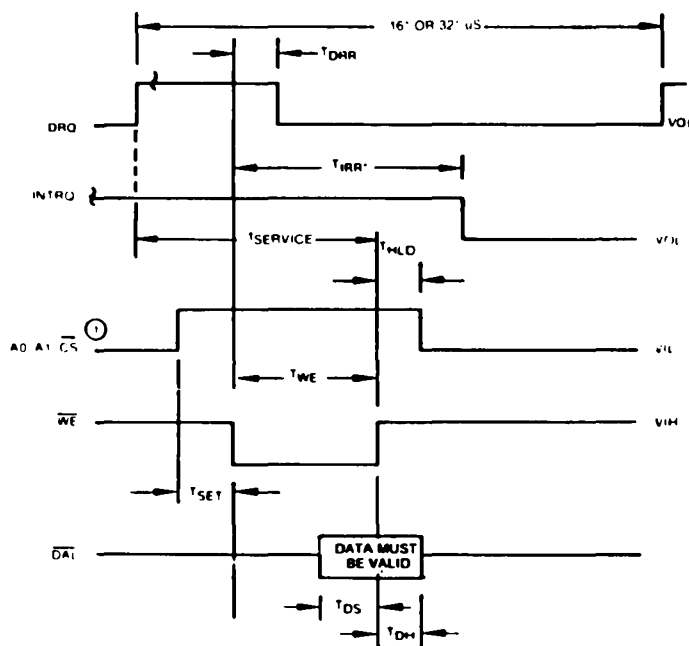


NOTE 1 \overline{CS} MAY BE PERMANENTLY TIED LOW IF DESIRED
*TIME DOUBLES WHEN CLOCK = 1MHz

1 SERVICE (WORST CASE)
FM 27.5 uS
MFM 13.5 uS

DRQ RISING EDGE: INDICATES THAT THE DATA REGISTER HAS ASSEMBLED DATA
DRQ FALLING EDGE: INDICATES THAT THE DATA REGISTER WAS READ
INTRQ RISING EDGE: OCCURS AT END OF COMMAND
INTRQ FALLING EDGE: INDICATES THAT THE STATUS REGISTER WAS READ

WRITE ENABLE TIMING



NOTE 1 \overline{CS} MAY BE PERMANENTLY TIED LOW IF DESIRED
2 WHEN WRITING DATA INTO SECTOR TRACK OR DATA REGISTER USER CANNOT READ THIS REGISTER UNTIL AT LEAST 4 uS IN MFM AFTER THE RISING EDGE OF WE WHEN WRITING INTO THE COMMAND REGISTER STATUS IS NOT VALID UNTIL SOME 28 uS IN FM, 14 uS IN MFM LATER THESE TIMES ARE DOUBLED WHEN CLK = 1MHz
*TIME DOUBLES WHEN CLOCK = 1MHz

1 SERVICE (WORST CASE)
FM 23.5 uS
MFM 11.5 uS

DRQ RISING EDGE: INDICATES THAT THE DATA REGISTER IS EMPTY
DRQ FALLING EDGE: INDICATES THAT THE DATA REGISTER IS LOADED
INTRQ RISING EDGE: INDICATE THE END OF A COMMAND
INTRQ FALLING EDGE: INDICATES THAT THE COMMAND REGISTER IS WRITTEN TO

INPUT DATA TIMING

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
TPW	Raw Read Pulse Width	100	200		nsec	
TBC	Raw Read Cycle Time	1500	2000		nsec	

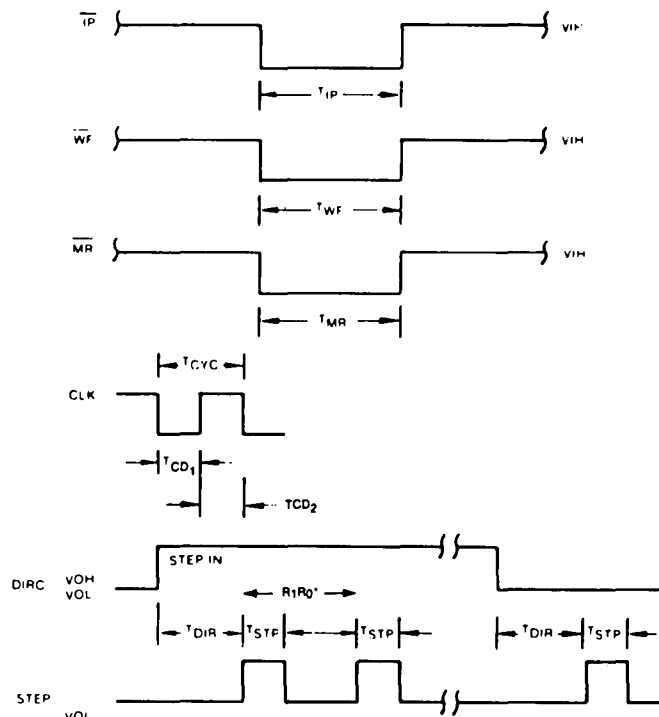
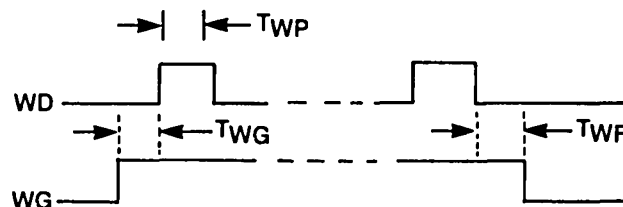
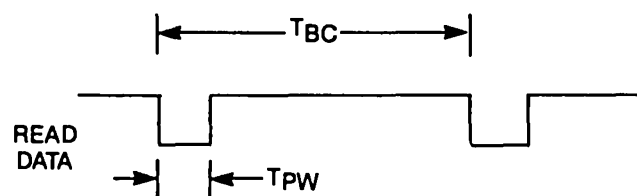
WRITE DATA TIMING: (ALL TIMES DOUBLE WHEN CLK = 1 MHz) (NO WRITE PRECOMPENSATION)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
TWP	Write Data Pulse Width	400	500	600	nsec	FM
		200	250	300	nsec	MFM
TWG	Write Gate to Write Data		2		μsec	FM
			1		μsec	MFM
TWF	Write Gate off from WD		2		μsec	FM
			1		μsec	MFM

MISCELLANEOUS TIMING:

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
tCD ₁	Clock Duty (low)	230	250	20000	nsec	See Note ± CLK ERROR
tCD ₂	Clock Duty (high)	230	250	20000	nsec	
tSTP	Step Pulse Output	2 or 4			μsec	
tDIR	Dir Setup to Step		12		μsec	
tMR	Master Reset Pulse Width	50			μsec	See Note Input 0-5V
tIP	Index Pulse Width	10			μsec	
RWP	Read Window Pulse Width					
		120		700	nsec	
		240		1400	nsec	FM ± 15%
	Precomp Adjust.	100		300	nsec	MFM
WPW	Write Data Pulse Width					Precomp = 100 nsec
		200	300	400	nsec	MFM
WPW	Write Data Pulse Width					Precomp = 300 nsec
		600	900	1200	nsec	FM
VCO	Free Run Voltage Controlled Oscillator. Adjustable by ext. capacitor on Pin 26	6.0	4.0		MHz	Cext = 0
	Pump Up + 25%	5.0			MHz	Cext = 35 pf
VCO	Pump Down - 25%			3.0	MHz	PU = 2.2V
						Cext = 35 pf
VCO	5% Change V _{CC}	3.8		4.2	MHz	P _D = 0.2V
	T _A = 75°C	3.5			MHz	Cext = 35 pf
Cext	Adjustable external capacitor	20	45	100	pf	Cext = 35 pf
RCLK	Derived read clock = VCO ÷ 8, 16, 32					VCO = 4.0MHz nom
			500		KHz	VCO = 4.0MHz
			250		KHz	DDEN = 0
			250		KHz	5/8 = 1
			125		KHz	DDEN = 0
					KHz	5/8 = 0
					KHz	DDEN = 1
					KHz	5/8 = 1
					KHz	DDEN = 1
					KHz	5/8 = 0
PU/DON	PU/P _D time on (pulse width)			250	ns	MFM
				500	ns	FM
f _{LOCK} *	Data Separator Capture Range	237.5	250	262.5	kbits/sec	5/8 = 0

*The f_{LOCK} specification is guaranteed from 10°C to 40°C.

MISCELLANEOUS TIMING

WRITE DATA TIMING

READ DATA TIMING

NOTES:

1. Times double when clock = 1 MHz.
2. Output timing readings are at $V_{OL} = 0.8v$ and $V_{OH} = 2.0v$.

* FROM STEP RATE TABLE

TABLE 4. STATUS REGISTER SUMMARY

BIT	ALL TYPE I COMMANDS	READ ADDRESS	READ SECTOR	READ TRACK	WRITE SECTOR	WRITE TRACK
S7	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY
S6	WRITE PROTECT	0	0	0	WRITE PROTECT	WRITE PROTECT
S5	HEAD LOADED	0	RECORD TYPE	0	0	0
S4	SEEK ERROR	RNF	RNF	0	RNF	0
S3	CRC ERROR	CRC ERROR	CRC ERROR	0	CRC ERROR	0
S2	TRACK 0	LOST DATA	LOST DATA	LOST DATA	LOST DATA	LOST DATA
S1	INDEX PULSE	DRQ	DRQ	DRQ	DRQ	DRQ
S0	BUSY	BUSY	BUSY	BUSY	BUSY	BUSY

STATUS FOR TYPE I COMMANDS

BIT NAME	MEANING
S7 NOT READY	This bit when set indicates the drive is not ready. When reset it indicates that the drive is ready. This bit is an inverted copy of the Ready input and logically 'ored' with MR.
S6 PROTECTED	When set, indicates Write Protect is activated. This bit is an inverted copy of \overline{WRPT} input.
S5 HEAD LOADED	When set, it indicates the head is loaded and engaged. This bit is a logical "and" of HLD and HLT signals.
S4 SEEK ERROR	When set, the desired track was not verified. This bit is reset to 0 when updated.
S3 CRC ERROR	CRC encountered in ID field.
S2 TRACK 00	When set, indicates Read/Write head is positioned to Track 0. This bit is an inverted copy of the \overline{TROO} input.
S1 INDEX	When set, indicates index mark detected from drive. This bit is an inverted copy of the \overline{IP} input.
S0 BUSY	When set command is in progress. When reset no command is in progress.

STATUS FOR TYPE II AND III COMMANDS

BIT NAME	MEANING
S7 NOT READY	This bit when set indicates the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the Ready input and 'ored' with MR. The Type II and III Commands will not execute unless the drive is ready.
S6 WRITE PROTECT	On Read Record: Not Used. On Read Track: Not Used. On any Write: It indicates a Write Protect. This bit is reset when updated.
S5 RECORD TYPE	On Read Record: It indicates the record-type code from data field address mark. 1 = Deleted Data Mark. 0 = Data Mark. On any Write: Forced to a Zero.
S4 RECORD NOT FOUND (RNF)	When set, it indicates that the desired track, sector, or side were not found. This bit is reset when updated.
S3 CRC ERROR	If S4 is set, an error is found in one or more ID fields; otherwise it indicates error in data field. This bit is reset when updated.
S2 LOST DATA	When set, it indicates the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated.
S1 DATA REQUEST	This bit is a copy of the DRQ output. When set, it indicates the DR is full on a Read Operation or the DR is empty on a Write operation. This bit is reset to zero when updated.
S0 BUSY	When set, command is under execution. When reset, no command is under execution.

SUMMARY OF ADJUSTMENT PROCEDURE
WRITE PRECOMPENSATION

- 1) Set $\overline{\text{TEST}}$ (Pin 22) to a logic high.
- 2) Strobe $\overline{\text{MR}}$ (Pin 19).
- 3) Set $\overline{\text{TEST}}$ (Pin 22) to a logic low.
- 4) Observe pulse width on WD (Pin 31).
- 5) Adjust WPW (Pin 33) for desired pulse width (Precomp Value).
- 6) Set $\overline{\text{TEST}}$ (Pin 22) to a logic high.

DATA SEPARATOR

- 1) Set $\overline{\text{TEST}}$ (Pin 22) to a logic high.
- 2) Strobe $\overline{\text{MR}}$ (Pin 19). Insure that $\overline{5/8}$, and $\overline{\text{DDEN}}$ are set properly.
- 3) Set $\overline{\text{TEST}}$ (Pin 22) to a logic low.
- 4) Observe Pulse Width on TG43 (Pin 29).
- 5) Adjust RPW (Pin 18) for 1/8 of the read clock (250ns for 8" DD, 500ns for 5 1/4" DD, etc.).
- 6) Observe Frequency on DIRC (Pin 16).
- 7) Adjust variable capacitor on VCO pin for Data Rate (500 KHz for 8" DD, 250 KHz for 5 1/4" DD, etc.).
- 8) Set $\overline{\text{TEST}}$ (Pin 22) to a logic high.

NOTE: To maintain internal VCO operation, insure that $\overline{\text{TEST}} = 1$ whenever a master reset pulse is applied.



DYNAMIC RAM CONTROLLER

FEATURES

- Controls operation of 8K/16K/32K/64K dynamic RAMs
- Creates static RAM appearance
- One package contains address multiplexer, refresh control and timing control
- Directly addresses and drives up to 256K bytes of memory without external drivers
- Operates from microprocessor clock
- Refresh may be internally or externally initiated
- Strap-selected wait state generation for microprocessor/memory speed matching

- Three-state outputs allow multiport memory configuration
- Performance ranges of 150 ns/200 ns/250 ns
- Compatible with TI TMS 4500A

DESCRIPTION

The VL4500A is a monolithic DRAM system controller designed to provide address multiplexing, timing, control, and refresh/access arbitration functions to simplify the interface of dynamic RAMs to microprocessor systems.

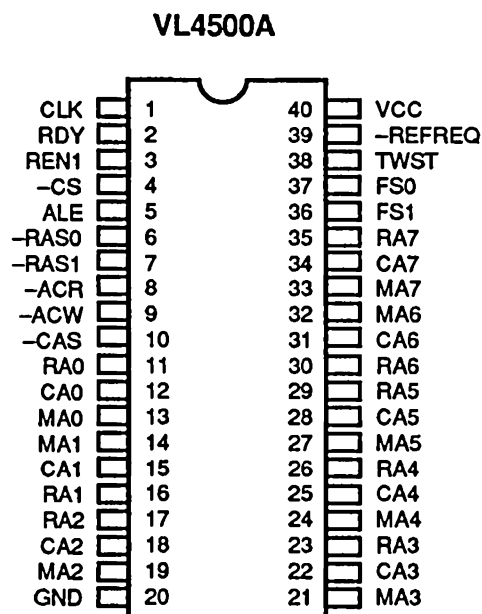
The controller contains a 16-bit multiplexer that generates the address

lines for the memory device from the 16 system address bits and provides the strobe signals required by the memory to decode the address. An 8-bit refresh counter generates the 256-row addresses required to refresh.

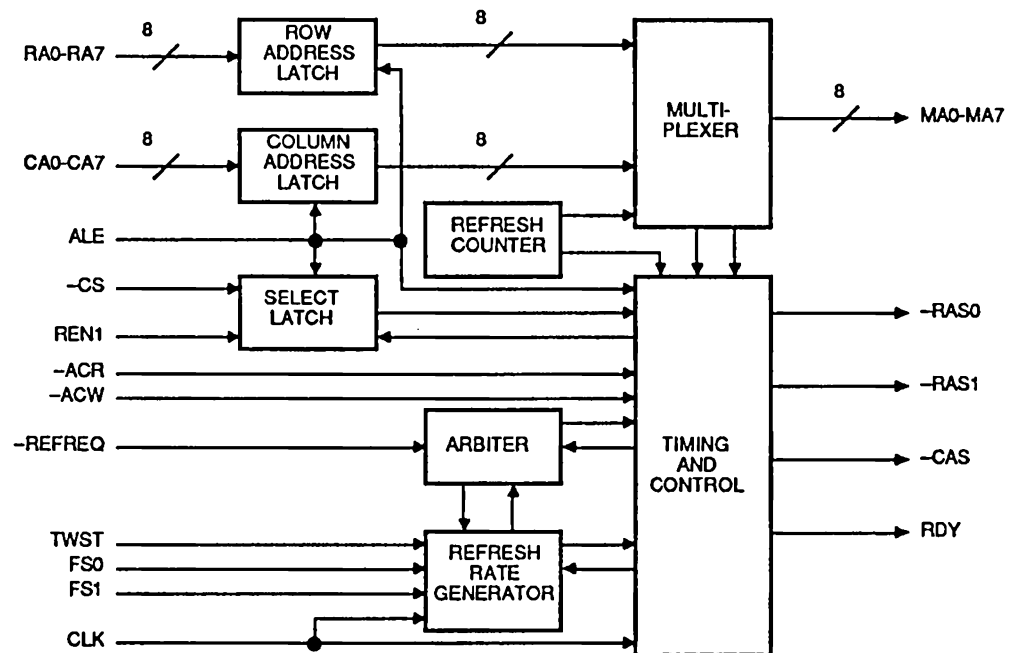
A refresh timer is provided that generates the necessary timing to refresh the dynamic memories and assure data retention.

The VL4500A also contains refresh/access arbitration circuitry to resolve conflicts between memory access requests and memory refresh cycles. The VL4500A is offered in a 40-pin 600-mil dual-in-line plastic package and is guaranteed for operation from 0°C to 70°C.

PIN DIAGRAM



BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Access Time	Package
VL4500-15PC VL4500-15CC	150 ns	Plastic DIP Ceramic DIP
VL4500-20PC VL4500-20CC	200 ns	Plastic DIP Ceramic DIP

Note: Operating temperature range is 0°C to +70°C.

PIN DESCRIPTIONS

RA0-RA7	Input	Row Address — Used to generate the row address for the multiplexer.
CA0-CA7	Input	Column Address — Used to generate the column address for the multiplexer.
MA0-MA7	Output	Memory Address — 3-state outputs designed to drive the addresses of the Dynamic RAM array.
ALE	Input	Address Latch Enable — Used to latch the 16 address inputs, \overline{CS} and REN1. This also initiates an access cycle if Chip Select is valid. The rising edge (LOW-to-HIGH level) of ALE returns \overline{RAS} to HIGH.
\overline{CS}	Input	Chip Select — A LOW on this input enables an access cycle. The trailing edge of ALE latches the Chip Select input.
REN1	Input	RAS Enable 1 — Used to select one of two banks of RAM via the $\overline{RAS0}$ and $\overline{RAS1}$ outputs when chip select is present. When LOW, $\overline{RAS0}$ is selected; when HIGH, $\overline{RAS1}$ is selected.
\overline{ACR} , \overline{ACW}	Input	Access Control, Read; Access Control, Write — A LOW on either of these inputs causes the column address to appear on MA0-MA7 and the Column Address Strobe to pulse active LOW. The rising edge of \overline{ACR} or \overline{ACW} terminates the cycle by ending \overline{RAS} and \overline{CAS} strobes. When \overline{ACR} and \overline{ACW} are both LOW, MA0-MA7, $\overline{RAS0}$, $\overline{RAS1}$, and \overline{CAS} go into a high-impedance (floating) state.
CLK	Input	System Clock — Provides the master timing to generate refresh cycle timings and refresh rate. Refresh rate is determined by the TWST, FS1, FS0 inputs.
\overline{REFREQ}	Input/ Output	Refresh Request — (This input should be driven by an open-collector output.) On input, a LOW-going edge initiates a refresh cycle and will cause the internal refresh timer to be reset on the next falling edge of the CLK. As an output, a LOW-going edge signals an internal refresh request and that the refresh timer will be reset on the next LOW-going edge of CLK. \overline{REFREQ} will remain LOW until the refresh cycle is in progress and the current refresh address is present on MA0-MA7. (Note: \overline{REFREQ} contains an internal pull-up resistor with a nominal resistance of 10 k Ω .)
$\overline{RAS0}$, $\overline{RAS1}$	Output	Row Address Strobe — 3-state outputs used to latch the row address into the bank of DRAMs selected by REN1. On refresh both signals are driven.
\overline{CAS}	Output	Column Address Strobe — 3-state output used to latch the column address into the DRAM array.
RDY	Output	Ready — Totem-pole output used to synchronize memories that are too slow to guarantee microprocessor access time requirements. This output is also used to inhibit access cycles during refresh when in cycle-steal mode.
TWST	Input	Timing/Wait Strap — A HIGH on this input indicates a wait state should be added to each memory cycle. In addition, it is used in conjunction with FS0 and FS1 to determine refresh rate and timing.
FS0, FS1	Inputs	Frequency Select 0; Frequency Select 1 — Strap inputs used to select Mode and Frequency of operation as shown in Table 1.

TABLE 1: STRAP CONFIGURATION

Strap Input Modes			Wait States For Memory Access	Refresh Rate	Minimum Clk Freq (MHz)	Refresh Freq (kHz)	Clock Cycles For Each Refresh
TWST	FS1	FS0					
L	L	L (1)	0	External	—	Refreq.	4
L	L	H	0	Clk ÷ 31	1.984	64-95 (2)	3
L	H	L	0	Clk ÷ 46	2.944	64-85 (2)	3
L	H	H	0	Clk ÷ 61	3.904	64-82 (3)	4
H	L	L	1	Clk ÷ 46	2.944	64-85 (2)	3
H	L	H	1	Clk ÷ 61	3.904	64-80 (2)	4
H	H	L	1	Clk ÷ 76	4.864	64-77 (2)	4
H	H	H	1	Clk ÷ 91	5.824	64-88 (4)	4

Notes:

1. This strap configuration resets the Refresh Timer circuitry.
2. Upper figure in refresh frequency is the frequency produced if the minimum CLK frequency of the next select state is used.
3. Refresh frequency if CLK frequency is 5 MHz.
4. Refresh frequency if CLK frequency is 8 MHz.

FUNCTIONAL DESCRIPTION

VL4500A consists of six basic blocks; address and select latches, refresh rate generator, refresh counter, the multiplexer, the arbiter, and the timing and control block.

ADDRESS AND SELECT LATCHES

The address and select latches allow the DRAM controller to be used in systems that multiplex address and data on the same lines without external latches. The row address latches are transparent, meaning that while ALE is HIGH, the output at MA0-MA7 follows the inputs RA0-RA7.

REFRESH RATE GENERATOR

The refresh rate generator is a counter that indicates to the arbiter that it is time for a refresh cycle. The counter divides the clock frequency according to the configuration straps as shown in Table 1. The counter is reset when a refresh cycle is requested or when TWST, FS1 and FS0 are LOW. The configuration straps allow the matching of memories to the system access time.

Upon power-up it is necessary to provide a reset signal by driving all three straps to the controller LOW to initialize internal counters. A system's LOW-active, power-on reset ($\overline{\text{RESET}}$) can be used to accomplish this by connecting it to those straps that are desired HIGH during operation. During this reset period, at least four clock cycles should occur.

REFRESH COUNTER

The refresh counter contains the address of the row to be refreshed. The counter is decremented after each refresh cycle. [A LOW-to-HIGH transition on TWST sets the refresh counter to FF₁₆ (255₁₀).]

MULTIPLEXER

The multiplexer provides the DRAM array with row, column, and refresh addresses at the proper times. Its inputs are the address latches and the refresh counter. The outputs provide up to 16 multiplexed addresses on eight lines.

ARBITER

The arbiter provides two operational cycles; access and refresh. The arbiter resolves conflicts between cycle requests and cycles in execution, and schedules the inhibited cycle when used in cycle-steal mode.

TIMING AND CONTROL BLOCK

The timing and control block executes the operational cycle at the request of the arbiter. It provides the DRAM array with $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ signals. It provides the CPU with a RDY signal. It controls the multiplexer during all cycles. It resets the refresh rate generator and decrements the refresh counter during refresh cycles.

ABSOLUTE MAXIMUM RATINGS

Operating Ambient Temperature Range	0°C to +70°C
Storage Temperature Range	-65°C to +150°C
Supply Voltage Range, V _{CC} , Note 1	-1.5 to +7 V
Input Voltage Range (any input), Note 1	-1.5 to +7 V
Continuous Power Dissipation	1.2 W

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions

above those listed on the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS: T_A = 0°C to +70°C

Symbol	Parameter	Min	Typ (3)	Max	Unit	Conditions
V _{IL} (except $\overline{\text{REFREQ}}$)	Input LOW Voltage	-1.0 (2)		0.8	V	
V _{IL} ($\overline{\text{REFREQ}}$)	Input LOW Voltage	-1.0 (2)		0.8	V	
V _{IH}	Input HIGH Voltage	2.4		6.0	V	
V _{OL}	Output LOW Voltage			0.4	V	I _{OL} = 4 mA V _{CC} = 4.5 V
V _{OH}	Output HIGH Voltage	MA0-MA7, RDY	2.4			I _{OH} = -1 mA V _{CC} = 4.5 V
		$\overline{\text{RAS0}}$, $\overline{\text{RAS1}}$, $\overline{\text{CAS}}$	2.7		V	
		$\overline{\text{REFREQ}}$	2.4			I _{OH} = -100 μ A V _{CC} = 4.5 V
I _{IH}	Input HIGH Current All pins except $\overline{\text{REFREQ}}$			10	μ A	V _I = 5.5 V
I _{IL}	Input LOW Current	$\overline{\text{REFREQ}}$		-1.25	mA	V _I = 0 V
		All others		-10	μ A	
I _{OZ}	Output Off-State Current			\pm 50	μ A	V _O = 0 to 4.5 V V _{CC} = 5.5 V
I _{CC}	Operating Supply Current		100	140	mA	T _A = 0°C V _{CC} = 5.5 V

CAPACITANCE: T_A = 25°C, f = 1.0 MHz

Symbol	Parameter	Min	Typ (3)	Max	Unit	Conditions
C _I	Input Capacitance		5		pF	V _I = 0 V f = 1 MHz
C _O	Output Capacitance		6		pF	V _O = 0 V f = 1 MHz

Notes:

1. Voltage values are with respect to the ground terminal.
2. The algebraic convention, where the more negative limit is designated as minimum, is used in this data sheet for logic voltage levels only.
3. All typical values are at V_{CC} = 5 V, T_A = 25°C except where otherwise noted.

AC CHARACTERISTICS: $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$

Symbol	Parameter	VL4500A-15		VL4500A-20		VL4500A-25		Unit
		Min	Max	Min	Max	Min	Max	
$t_{C(C)}$	CLK Cycle Time	100		120		140		ns
$t_{W(CH)}$	CLK HIGH Pulse Width	40		40		40		
$t_{W(CL)}$	CLK LOW Pulse Width	40		45		45		
t_t	Transition Time, All Inputs		50		50		50	
t_{AEL-CL}	Time Delay, ALE LOW to CLK Starting LOW, Note 1	10		10		15		
t_{CL-AEL}	Time Delay, CLK LOW to ALE Starting LOW, Note 1	10		10		15		
t_{CL-AEH}	Time Delay, CLK LOW to ALE Starting HIGH, Note 2	15		20		20		
$t_{W(AEH)}$	Pulse Width ALE HIGH	50		60		60		
t_{AV-AEL}	Time Delay, Address, REN1, \overline{CS} Valid to ALE LOW	5		10		15		
t_{AEL-AX}	Time Delay, ALE LOW to Address Not Valid	10		10		10		
$t_{AEL-ACL}$	Time Delay, ALE LOW to \overline{ACX} LOW, Notes 3, 4, 5, 6	$t_{h(RA)} + 30$		$t_{h(RA)} + 40$		$t_{h(RA)} + 50$		
t_{ACH-CL}	Time Delay, \overline{ACX} HIGH to CLK LOW, Notes 3, 7	20		20		20		
t_{ACL-CH}	Time Delay, \overline{ACX} LOW to CLK Starting HIGH (to remove RDY)	30		30		30		
t_{RQL-CL}	Time Delay, \overline{REFREQ} LOW to CLK Starting LOW, Note 8	20		20		20		
$t_{W(RQL)}$	Pulse Width, \overline{REFREQ} LOW	20		20		20		

Notes:

- Coincidence of the trailing edge of CLK and the trailing edge of ALE should be avoided, as the refresh/access occurs on the trailing CLK edge. A trailing edge of CLK should occur during the interval from \overline{ACX} HIGH to ALE LOW.
- If ALE rises before \overline{ACX} and a refresh request is present, the falling edge of CLK after t_{CL-AEH} will output the refresh address to MA0-MA7 and initiate a refresh cycle.
- These specifications relate to system timing and do not directly reflect device performance.
- On the access grant cycle following refresh, the occurrence of \overline{CAS} LOW depends on the relative occurrence of ALE LOW to \overline{ACX} LOW. If \overline{ACX} occurs prior to or coincident with ALE then \overline{CAS} is timed from the CLK HIGH transition that causes RAS LOW. If \overline{ACX} occurs 20 ns or more after ALE then \overline{CAS} is timed from the CLK LOW transition following the CLK HIGH transition causing RAS LOW.
- For maximum speed access (internal delays on both access and access grant cycles), \overline{ACX} should occur prior to or coincident with ALE.
- $t_{h(RA)}$ is the dynamic memory row address hold time. \overline{ACX} should follow ALE by t_{AEL-CL} in systems where the required $t_{h(RA)}$ is greater than $t_{REL-MAX}$ minimum.
- Minimum of 20 ns is specified to ensure arbitration will occur on falling CLK edge. t_{ACH-CL} also affects precharge time such that the minimum t_{ACH-CL} should be equal or greater than: $t_{W(RH)} - t_{W(CL)} + 30$ ns (for cycle where \overline{ACX} HIGH occurs prior to ALE HIGH) where $t_{W(RH)}$ is the DRAM RAS precharge time.
- This parameter is necessary only if refresh arbitration is to occur on this falling edge of CLK (in systems where refresh is synchronized to external events).

AC CHARACTERISTICS: $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$

Symbol	Parameter	VL4500A-15		VL4500A-20		VL4500A-25		Unit	Conditions
		Min	Max	Min	Max	Min	Max		
t _{AEL-REL}	Time Delay, ALE LOW to $\overline{\text{RAS}}$ Starting LOW		35		40		50	ns	C _L = 160 pF
t _{t (REL)}	$\overline{\text{RAS}}$ Fall Time		15		20		25		
t _{RAV-MAV}	Time Delay, Row Address Valid to Memory Address Valid		45		50		60		
t _{AEH-MAV}	Time Delay, ALE HIGH to Valid Memory Address		65		75		90		C _L = 40 pF
t _{AEL-RYL}	Time Delay, ALE to RDY Starting LOW (TWST = 1 or Refresh in Progress)		40		40		40		
t _{AEL-CEL}	Time Delay, ALE LOW to $\overline{\text{CAS}}$ Starting LOW, Note 9	60	150	70	200	80	250		C _L = 160 pF
t _{AEH-REH}	Time Delay, ALE HIGH to $\overline{\text{RAS}}$ Starting HIGH		30		30		40		
t _{t (MAV)}	Address Transition Time		20		20		25		
t _{ACL-MAX}	Row Address Hold from $\overline{\text{ACX}}$ LOW	15		20		25			C _L = 320 pF
t _{MAV-CEL}	Time Delay, Memory Address Valid to $\overline{\text{CAS}}$ Starting LOW	0		0		0			
t _{t (CEL)}	$\overline{\text{CAS}}$ Fall Time		15		20		25		
t _{ACL-CEL}	Time Delay, $\overline{\text{ACX}}$ LOW to $\overline{\text{CAS}}$ Starting LOW, Note 9	40	100	45	130	50	165	ns	C _L = 160 pF
t _{ACH-REH}	Time Delay, $\overline{\text{ACX}}$ to $\overline{\text{RAS}}$ Starting HIGH		30		40		50		
t _{t (REH)}	$\overline{\text{RAS}}$ Rise Time		15		20		25		
t _{ACH-CEH}	Time Delay, $\overline{\text{ACX}}$ HIGH to $\overline{\text{CAS}}$ Starting HIGH	5	30	10	40	15	50		C _L = 320 pF
t _{t (CEH)}	$\overline{\text{CAS}}$ Rise Time		30		35		45		
t _{ACH-MAX}	Column Address Hold from $\overline{\text{ACX}}$ HIGH	10		15		15			C _L = 160 pF
t _{CH-RYH}	Time Delay, CLK HIGH to RDY Starting HIGH (After $\overline{\text{ACX}}$ LOW), Note 10		40		45		60		C _L = 40 pF
t _{RFL-RFL}	Time Delay, $\overline{\text{REFREQ}}$ External Until Supported by $\overline{\text{REFREQ}}$ Internal		30		35		35		
t _{CH-RFL}	Time Delay, CLK HIGH Until $\overline{\text{REFREQ}}$ Internal Starting LOW		30		35		45		
t _{CL-MAV}	Time Delay, CLK LOW Until Refresh Address Valid		75		100		125	ns	C _L = 160 pF
t _{CH-RRL}	Time Delay, CLK HIGH Until Refresh $\overline{\text{RAS}}$ Starting LOW	10	50	15	60	20	80		
t _{MAV-RRL}	Time Delay, Refresh Address Valid Until Refresh $\overline{\text{RAS}}$ LOW	5		5		5			
t _{CL-RFH}	Time Delay, CLK LOW to $\overline{\text{REFREQ}}$ Starting HIGH (3-cycle Refresh)		50		55		75		
t _{CH-RFH}	Time Delay, CLK HIGH to $\overline{\text{REFREQ}}$ Starting HIGH (4-cycle Refresh)		50		55		75		
t _{CH-RRH}	Time Delay, CLK HIGH to Refresh $\overline{\text{RAS}}$ Starting HIGH	5	35	10	45	10	60		
t _{CH-MAX}	Time Delay, Refresh Address Hold After CLK HIGH	15		20		25			

Notes:

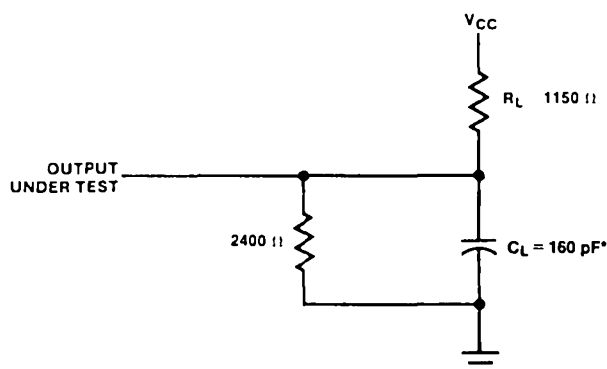
- The falling edge of $\overline{\text{CAS}}$ occurs as soon as both t_{AEL-CEL} and t_{ACL-CEL} have elapsed. If $\overline{\text{ACX}}$ goes LOW prior to (t_{AEL-CEL}) - (t_{ACL-CEL}) after ALE, the $\overline{\text{CAS}}$ timing is determined by t_{AEL-CEL}. Otherwise, the access time increases, and the falling edge of $\overline{\text{CAS}}$ is measured from the falling edge of $\overline{\text{ACX}}$ instead of ALE (t_{ACL-CEL} determines $\overline{\text{CAS}}$ timing).
- RDY returns HIGH on the rising edge of CLK. If TWST = 0, then on an access grant cycle RDY goes HIGH on the same edge that causes access $\overline{\text{RAS}}$ LOW. If TWST = 1, then RDY goes to the HIGH level on the first rising CLK edge after $\overline{\text{ACX}}$ goes LOW on access cycles and on the next rising edge after the edge that causes access $\overline{\text{RAS}}$ LOW on access grant cycles (assuming $\overline{\text{ACX}}$ LOW).

AC CHARACTERISTICS: $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$

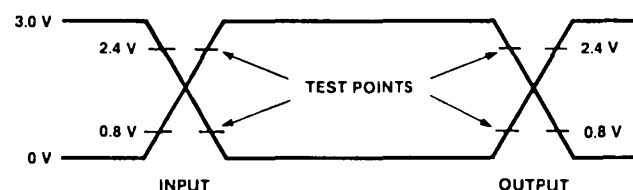
Symbol	Parameter	VL4500A-15		VL4500A-20		VL4500A-25		Unit	Conditions
		Min	Max	Min	Max	Min	Max		
t_{CH-REL}	Time Delay, CLK HIGH Until Access \overline{RAS} Starting LOW		60		70		95	ns	$C_L = 160\text{ pF}$
t_{CL-CEL}	Time Delay, CLK LOW to Access \overline{CAS} Starting LOW, Note 11		125		140		185		
t_{CL-MAX}	Row Address Hold After CLK LOW	25		30		40			
$t_{W(ACL)}$	\overline{ACX} LOW Width, Note 12	110		140		175			
$t_{REL-MAX}$	Row Address Hold From \overline{RAS} LOW	25		30		35			$C_L = 40\text{ pF}$
$t_{f(RYL)}$	RDY Fall Time		10		15		20		
$t_{f(RYH)}$	RDY Rise Time		20		25		35		$C_L = 160\text{ pF}$
t_{dis}	Output Disable Time (3-state Outputs)		100		125		165		
$t_{AEH-MAX}$	Column Address Hold From ALE HIGH	10		15		20			
t_{en}	Output Enable Time (3-state Outputs)		75		80		105		
$t_{CAV-CEL}$	Column Address Setup to \overline{CAS} After Refresh	0		0		0			
t_{CH-CEL}	Time Delay, CLK HIGH to Access \overline{CAS} Starting LOW, Note 11		180		200		235		
t_{ACL-CL}	\overline{ACX} LOW to CLK Starting LOW, Note 13	25		35		45			$C_L = 40\text{ pF}$
$t_{ACL-RYH}$	\overline{ACX} LOW to RDY Starting HIGH, Note 13		40		50		60		
t_{CL-ACL}	CLK LOW to \overline{ACX} Starting LOW, Note 13	0		0		0			

Notes:

- On the access grant cycle following refresh, the occurrence of \overline{CAS} LOW depends on the relative occurrence of ALE LOW to \overline{ACX} LOW. If \overline{ACX} occurs prior to or coincident with ALE then \overline{CAS} is timed from the CLK HIGH transition that causes \overline{RAS} LOW. If \overline{ACX} occurs 20 ns or more after ALE then \overline{CAS} is timed from the CLK LOW transition following the CLK HIGH transition causing \overline{RAS} LOW.
- The specification of $t_{W(ACL)}$ is designed to allow a \overline{CAS} pulse. This assures normal operation of the device in testing and system operation.
- For RDY HIGH transition (during normal access) to be timed from the rising edge of CLK, \overline{ACX} must occur t_{CL-ACL} after the falling edge of CLK. For \overline{ACX} prior to the falling edge of CLK by t_{ACL-CL} , the RDY HIGH transition will be $t_{ACL-RYH}$. Note that t_{ACL-CL} is a limiting parameter for control of RDY to be dependent on \overline{ACX} LOW. During the interval for $t_{ACL-CL} < \text{MINIMUM}$ to $t_{CL-ACL} > \text{MINIMUM}$, the control of RDY may vary between the rising clock edge or falling edge of \overline{ACX} .

LOAD CIRCUIT


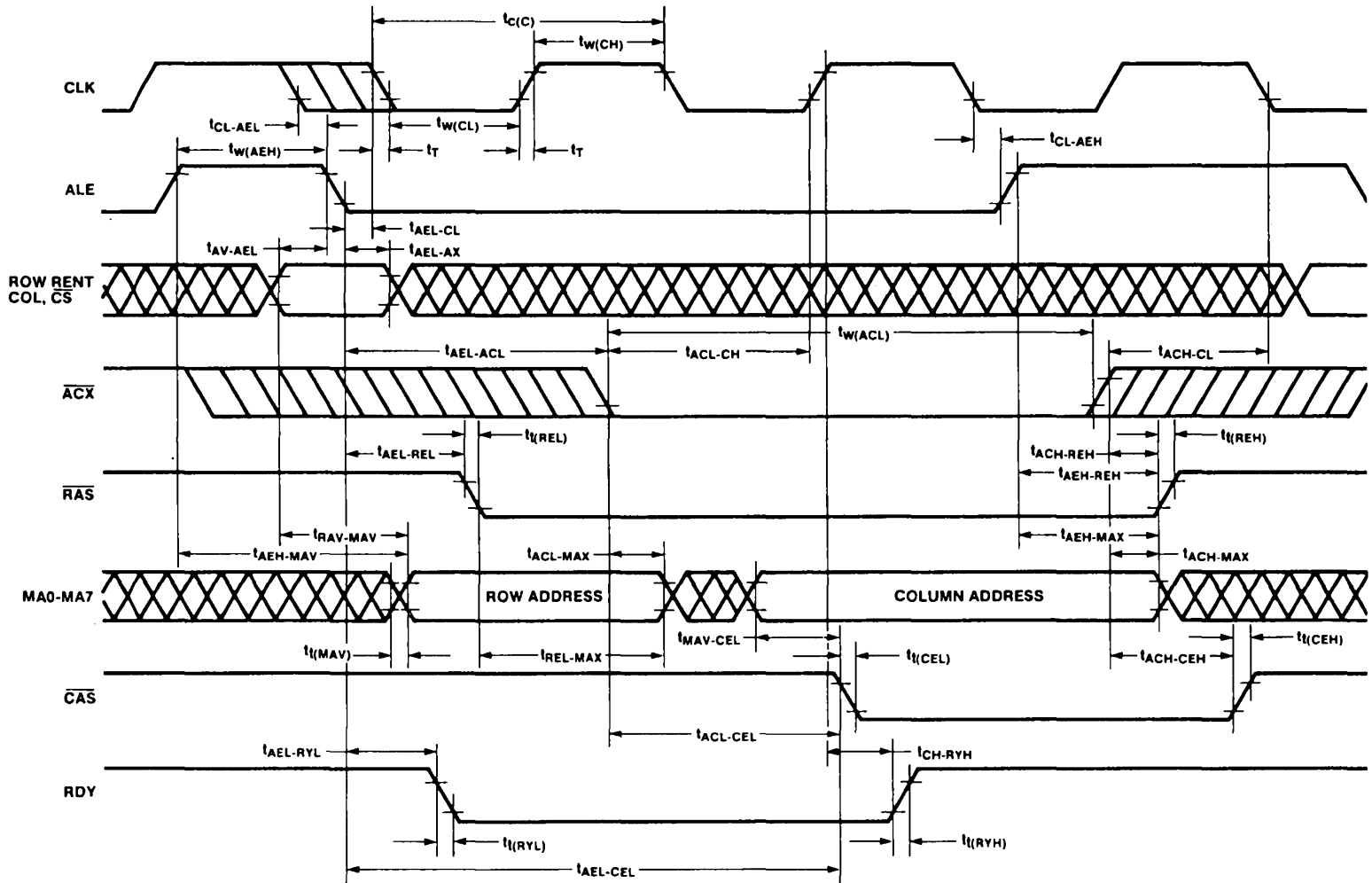
* C_L INCLUDES JIG CAPACITANCE

AC TESTING INPUT, OUTPUT WAVEFORM


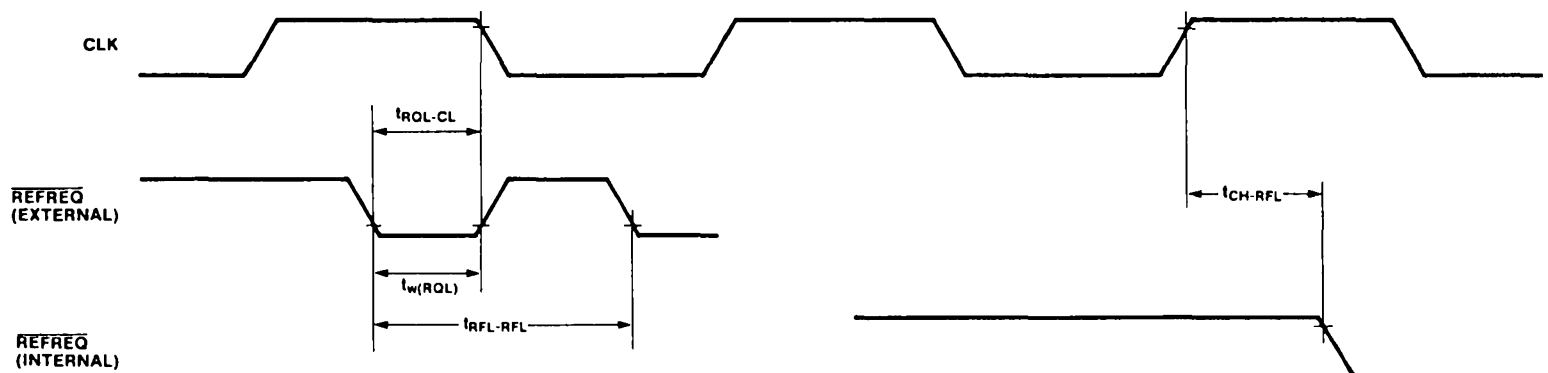
AC testing inputs are driven at 3.0 V for a logic "1" and 0.0 V for a logic "0". Timing measurements are made at 2.2 V for a logic "1" and 0.6 V for a logic "0" at the outputs. The inputs are measured at 2.4 V for a logic "1" and 0.8 V for a logic "0".

TIMING DIAGRAMS

ACCESS CYCLE TIMING



REFRESH REQUEST TIMING



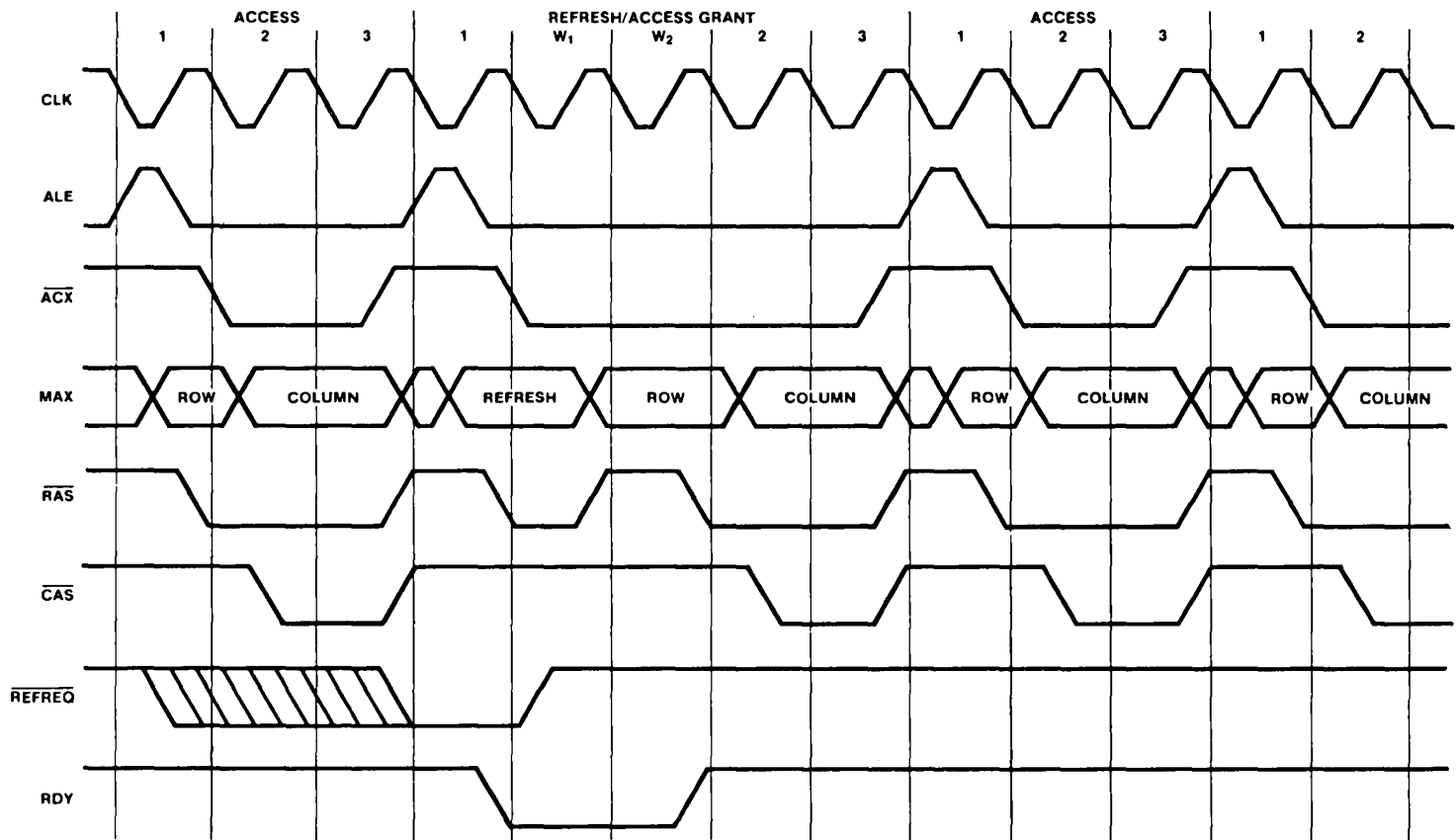


OUTPUT 3-STATE TIMING

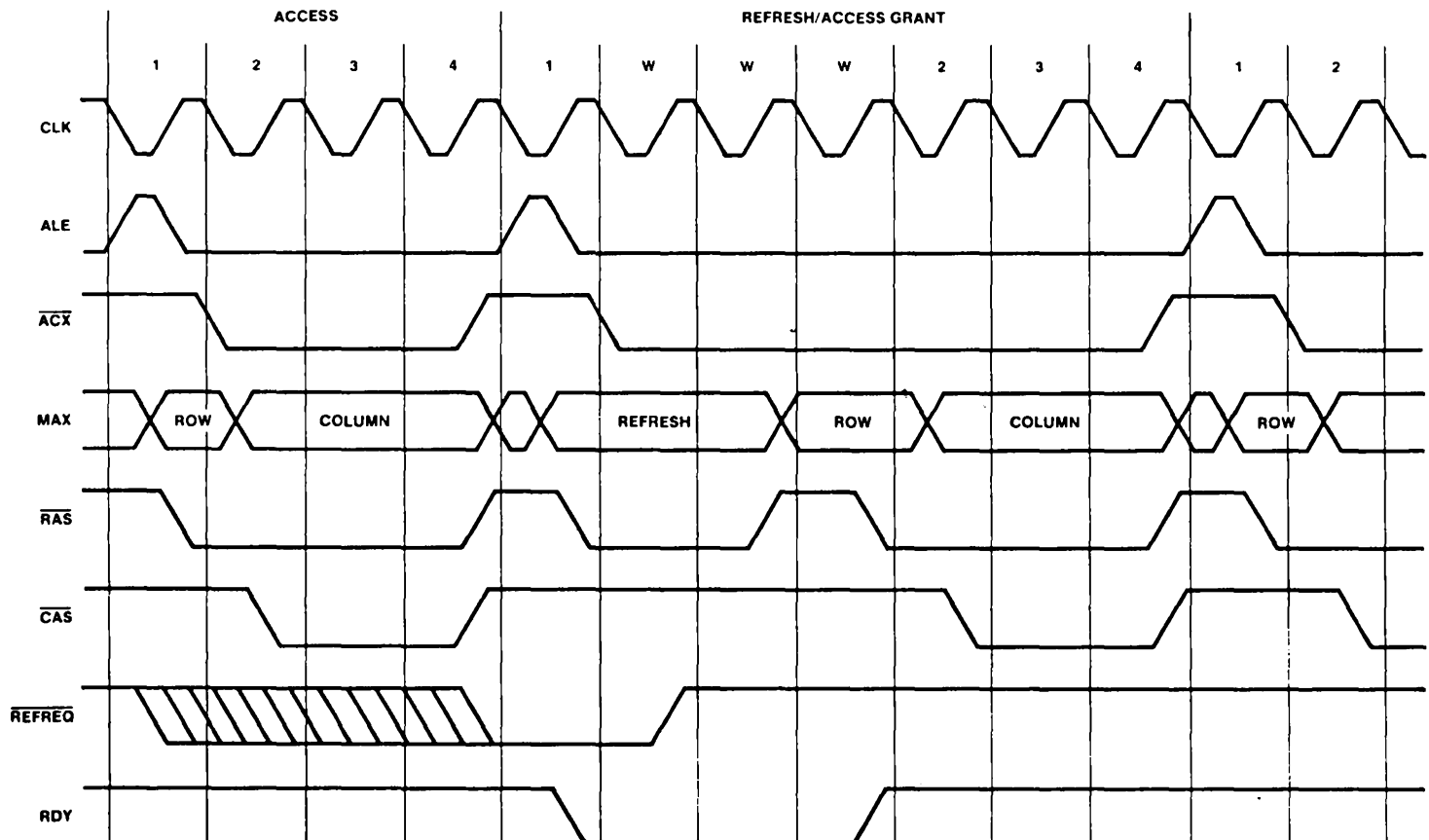


TIMING DIAGRAMS (Cont.)

TYPICAL ACCESS/REFRESH/ACCESS CYCLE (3-CYCLE, TWST = 0)

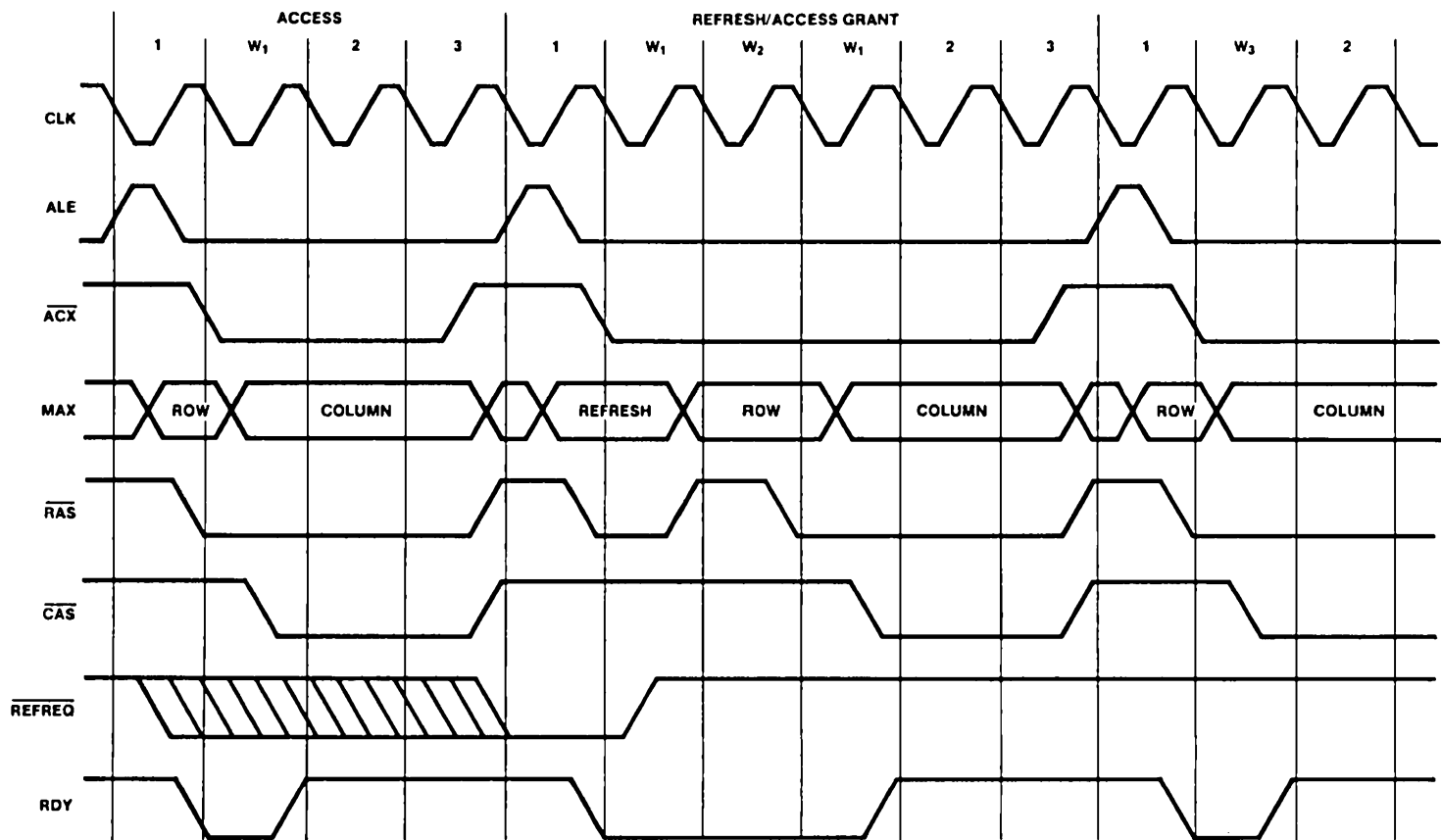


TYPICAL ACCESS/REFRESH/ACCESS CYCLE (4-CYCLE, TWST = 0)

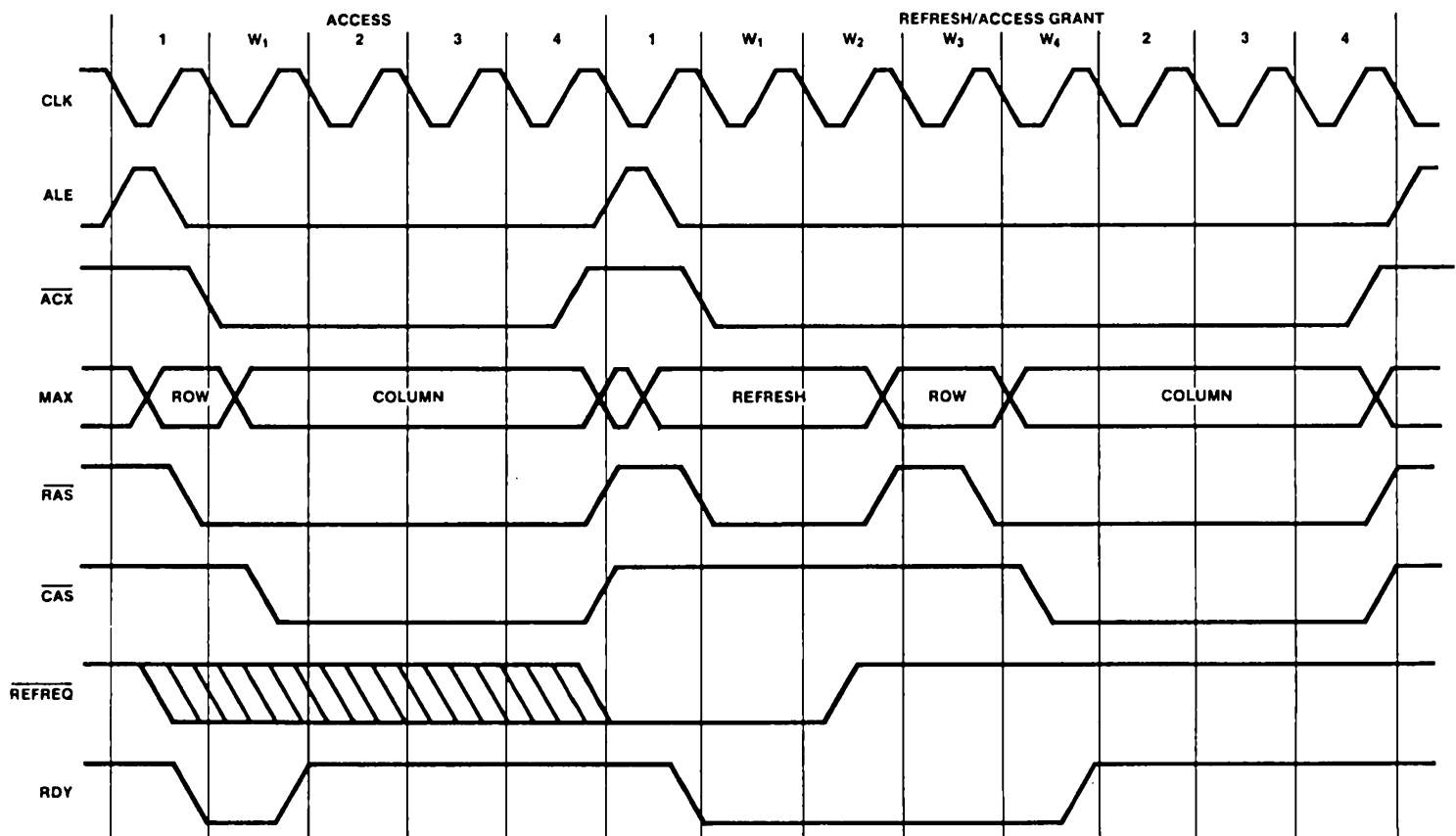


TIMING DIAGRAMS (Cont.)

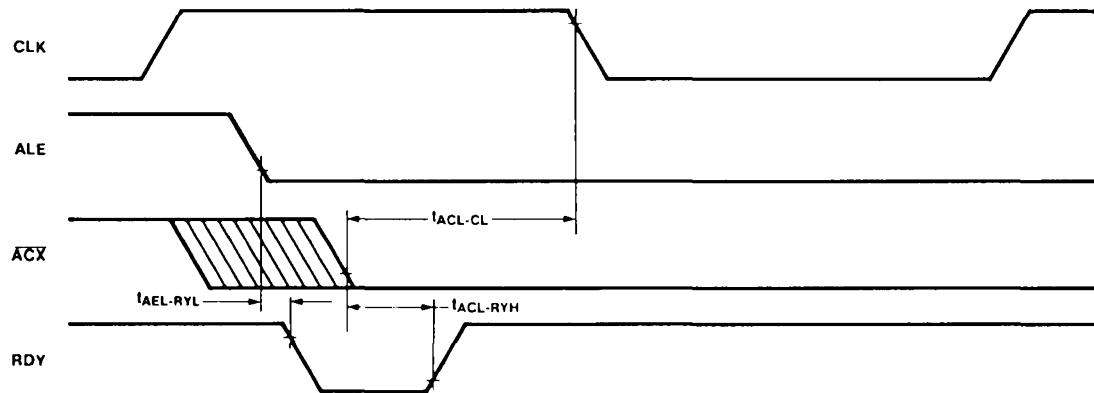
TYPICAL ACCESS/REFRESH/ACCESS CYCLE (3-CYCLE, TWST = 1)



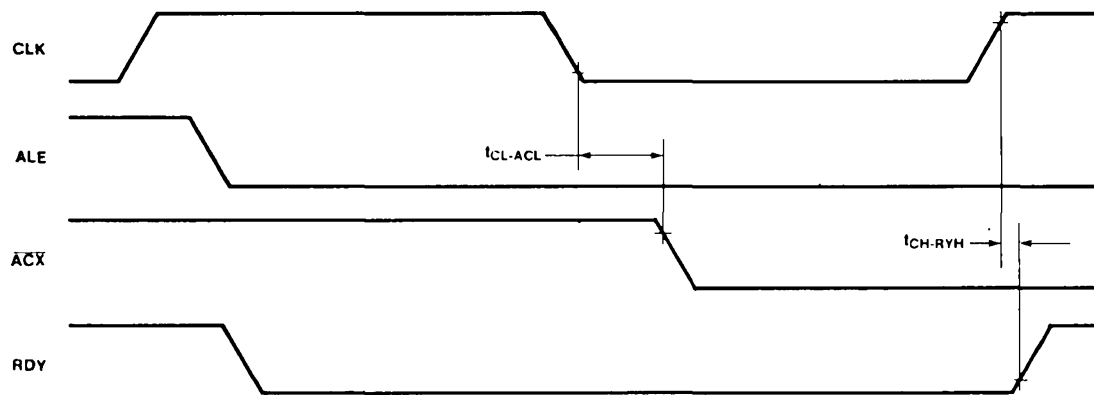
TYPICAL ACCESS/REFRESH/ACCESS CYCLE (4-CYCLE, TWST = 1)



READY (RDY) SIGNAL TIMING (WAIT STATE OPERATION, TWST = 1)



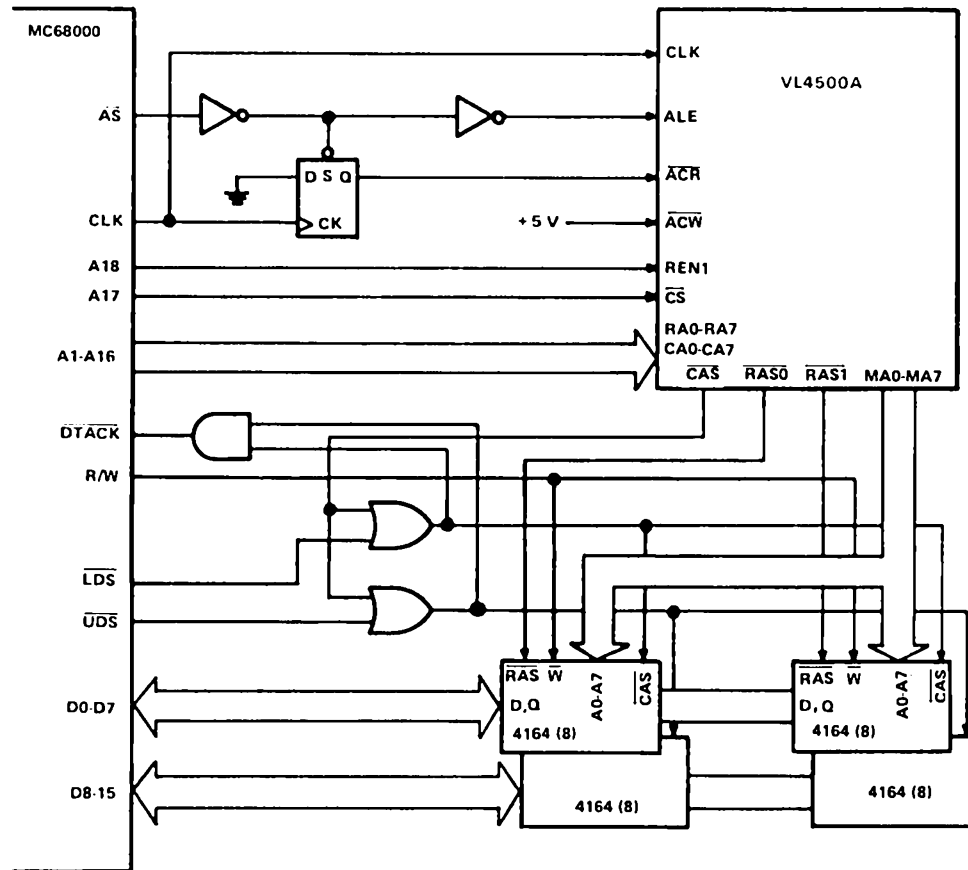
RDY starting HIGH is timed from \overline{ACX} LOW ($t_{ACL-RYH}$) for the condition \overline{ACX} going LOW while CLK HIGH.



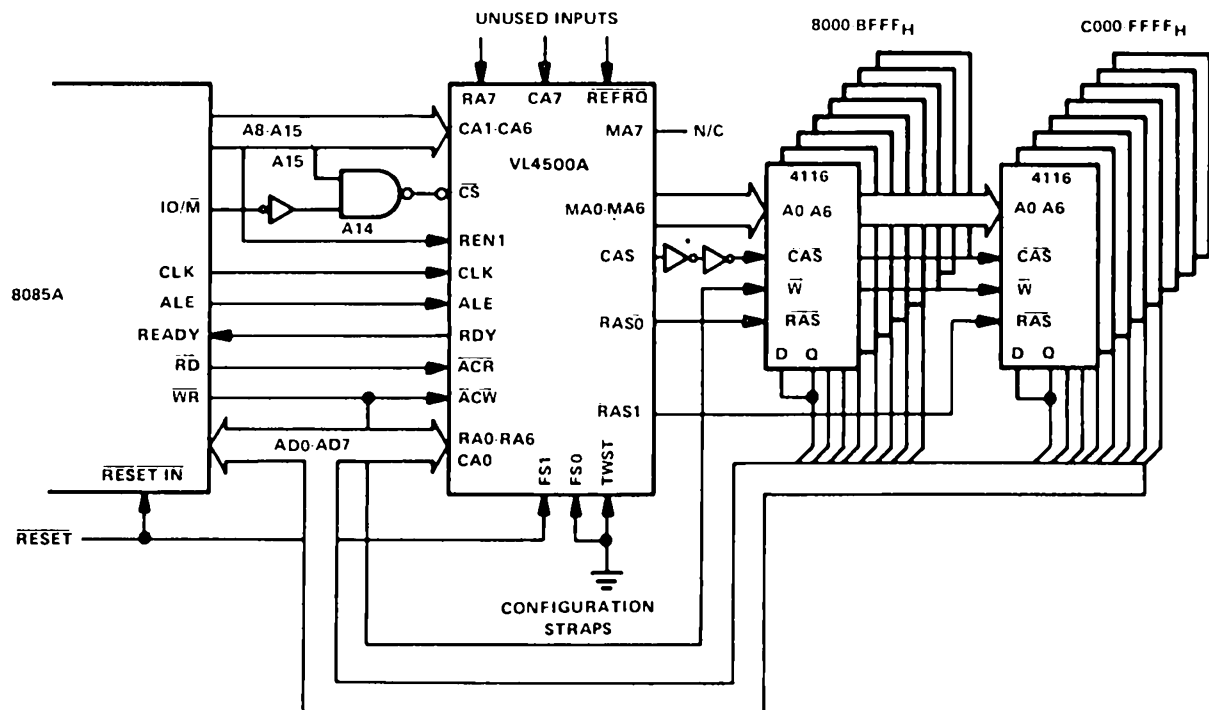
RDY starting HIGH is timed from CLK HIGH (t_{CH-RYH}) for the condition \overline{ACX} going LOW while CLK LOW.

TYPICAL APPLICATIONS

68000 CPU TO VL4500A 128K x 16 MEMORY INTERFACE



8085A CPU INTERFACE TO VL4500A CONTROLLER



*See section 5.1, p. 12.

DYNAMIC RAM CONTROLLER
FEATURES

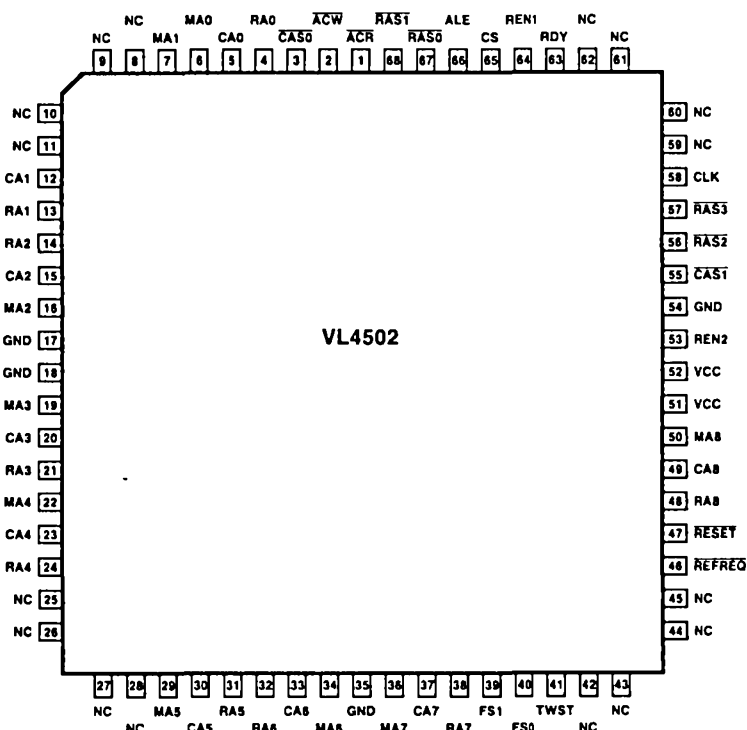
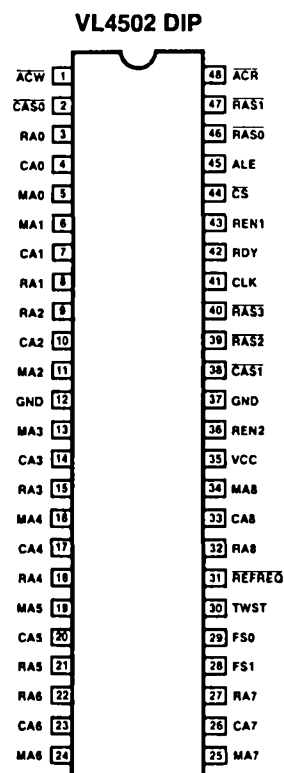
- Inputs are TTL voltage compatible
- Controls operation of 64K and 256K dynamic RAMs
- Creates static RAM appearance
- One package contains address multiplexer, refresh control and timing control
- Directly addresses and drives up to 2 megabytes of memory without external drivers
- Operates from microprocessor clock
 - No crystals, delay lines, or RC networks
 - Eliminates arbitration delays
- Refresh may be internally or externally initiated
- High performance CMOS technology
- Strap-selected wait state generation for microprocessor/memory speed matching
- Ability to synchronize or interleave controller with the microprocessor system (including multiple controllers)
- 3-state outputs allow multiport memory configuration
- Performance ranges of 150 ns/200 ns
- Compatible with VLSI VL4500A and TI TMS4500A, THCT4502

DESCRIPTION

The VL4502 is a monolithic DRAM system controller providing address multiplexing, timing, control and refresh/access arbitration functions to simplify the interface of dynamic RAMs to microprocessor systems.

The controller contains an 18-bit multiplexer that generates the address lines for the memory device from the 18 system address bits and provides the strobe signals required by the memory to decode the address. A 9-bit refresh counter generates up to 512 row addresses required to refresh.

A refresh timer is provided that generates the necessary timing to refresh the dynamic memories and assure data retention.

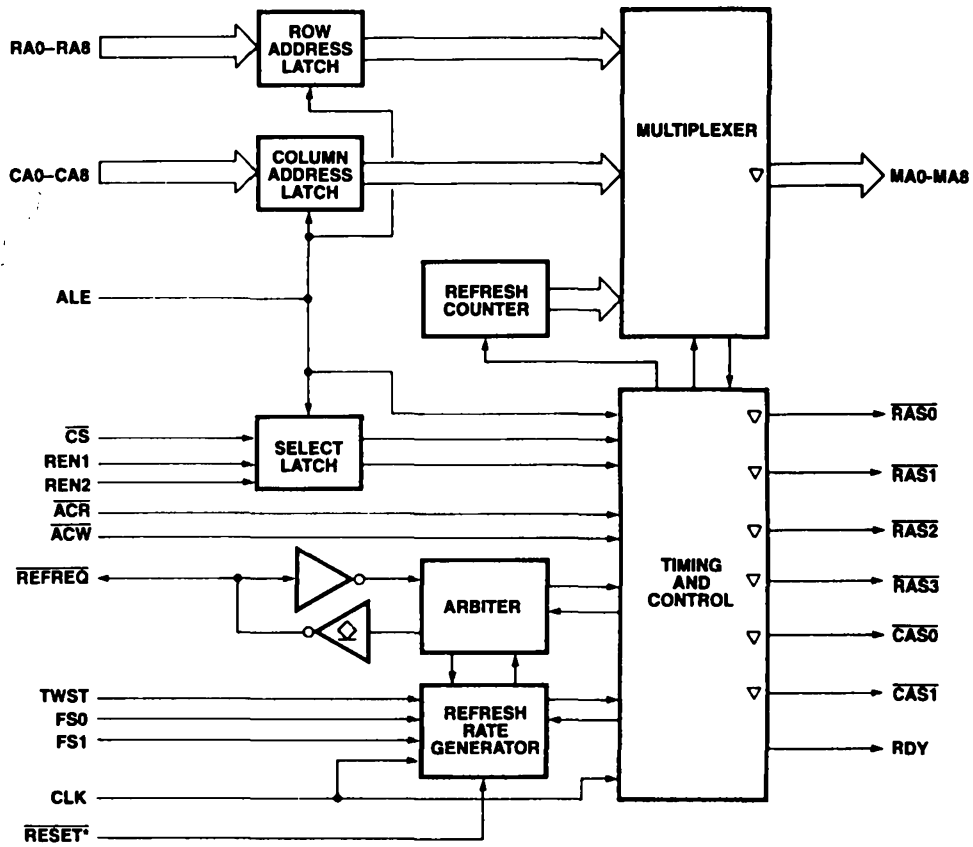
PIN DIAGRAMS

ORDER INFORMATION

Part Number	Access Time	Package
VL4502-15PC VL4502-15CC VL4502-15QC	150 ns	Plastic DIP Ceramic DIP Plastic Leaded Chip Carrier (PLCC)
VL4502-20PC VL4502-20CC VL4502-20QC	200 ns	Plastic DIP Ceramic DIP Plastic Leaded Chip Carrier (PLCC)

Note:

Operating temperature range: 0°C to +70°C.

BLOCK DIAGRAM



PIN DESCRIPTIONS

Pin Name	Pin Number, Note 1	Description
RA0–RA8	3, 8, 9, 15, 18, 21, 22, 27, 32	Row Address—These address inputs are used to generate the row address for the multiplexer.
CA0–CA8	4, 7, 10, 14, 17, 20, 23, 26, 33	Column Address—These address inputs are used to generate the column address for the multiplexer.
MA0–MA8	5, 6, 11, 13, 16, 19, 24, 25, 34	Memory Address—These three-state outputs are designed to drive the addresses of the Dynamic RAM array.
ALE	45	Address Latch Enable—This input is used to latch the 18 address inputs, \overline{CS} and REN1 and REN2. This also initiates an access cycle if chip select is valid. The rising edge (LOW level to HIGH level) of ALE returns \overline{RAS} to the HIGH level.
\overline{CS}	44	Chip Select—A LOW on this input enables an access cycle. The trailing edge of ALE latches the chip select input.
REN1, REN2	43, 36	\overline{RAS} Enable 1 and 2—These inputs are used to select one of four banks of RAM. When REN2 is LOW, the lower banks are enabled via $\overline{CAS0}$, $\overline{RAS0}$, and $\overline{RAS1}$. When REN2 is HIGH, the higher banks are enabled via $\overline{CAS1}$, $\overline{RAS2}$, and $\overline{RAS3}$. REN1 selects $\overline{RAS0}$, $\overline{RAS2}$ or $\overline{RAS1}$, $\overline{RAS3}$ when chip select is present.
\overline{ACR} , \overline{ACW}	48, 1	Access Control, Read; Access Control, Write—A LOW on either of these inputs causes the column addresses to appear on MA0–MA8 and the column address strobe. The rising edge of \overline{ACR} or \overline{ACW} terminates the cycle by ending \overline{RAS} and \overline{CAS} strobes. When \overline{ACR} and \overline{ACW} are both LOW, MA0–MA8, $\overline{RAS0}$, $\overline{RAS1}$, $\overline{RAS2}$, $\overline{RAS3}$, $\overline{CAS0}$, and $\overline{CAS1}$ go into a HIGH impedance (floating) state.
CLK	41	System Clock—This input provides the master timing to generate refresh cycle timings and refresh rate. Refresh rate is determined by the TWST, FS1, FS0 inputs.
\overline{REFREQ}	31	Refresh Request—(This input is driven by an open-collector output.) On input, a LOW-going edge initiates a refresh cycle and will cause the internal refresh timer to be reset on the next falling edge of the CLK. As an output, a LOW-going edge signals an internal refresh request and that the refresh timer will be reset on the next LOW-going edge of CLK. \overline{REFREQ} will remain LOW until the refresh cycle is in progress and the current refresh address is present on MA0–MA8. (Note: \overline{REFREQ} contains an internal pull-up resistor with a nominal resistance of 10 kilohms.)
$\overline{RAS0}$, $\overline{RAS1}$ $\overline{RAS2}$, $\overline{RAS3}$	46, 47 39, 40	Row Address Strobe—These three-state outputs are used to latch the row address into the bank of DRAMs selected by REN1 and REN2. On refresh, all \overline{RAS} signals are active.
$\overline{CAS0}$, $\overline{CAS1}$	2, 38	Column Address Strobe—these three-state outputs are used to latch the column address into the DRAM array.
RDY	42	Ready—This totem-pole output synchronizes memories that are too slow to guarantee microprocessor access time requirements. This output is also used to inhibit access cycles during refresh when in cycle-steal mode.
TWST	30	Timing/Wait Strap—A HIGH on this input indicates a wait state should be added to each memory cycle. In addition it is used in conjunction with FS0 and FS1 to determine refresh rate and timing.
FS0, FS1	29, 28	Frequency Select 0; Frequency Select 1—These are strap inputs to select Mode and Frequency of operation as shown in Table 1.
\overline{RESET}	(PLCC only)	\overline{RESET} —Active LOW input to initialize the controller asynchronously. Refresh Address is set to 1FFH, internal refresh requests, synchronizer, and frequency divider are cleared. This input is driven by an open collector driver. \overline{RESET} contains an internal pull-up with a nominal resistance of 100 K Ω . This allows the pin to be left open, if desired.

Note:

1. Pin numbers are for dual in-line package only.

TABLE 1: STRAP CONFIGURATION

Strap Input Modes, Note 1			Memory Access Wait States	Refresh Rate, Note 2	Refresh Clock Cycles
TWST	FS1	FS0			
L	L	L(3)	0	External	4
L	L	H	0	External	3
L	H	L	0	Clk ÷ 61	3
L	H	H	0	Clk ÷ 91	4
H	L	L	1	Clk ÷ 61	3
H	L	H	1	Clk ÷ 91	4
H	H	L	1	Clk ÷ 106	4
H	H	H	1	Clk ÷ 121	4

TABLE 2: OUTPUT STROBE SELECTION

Control		Input		Selected Output			
REN2	REN1	RAS0	RAS1	RAS2	RAS3	CAS0	CAS1
0	0	X				X	
0	1		X			X	
1	0			X			X
1	1				X		X

Notes:

1. If the strap configuration is changed, the device should be reset in order to insure normal refresh operation.
2. The maximum refresh rate is a function of the applicable maximum clock frequency (see AC Characteristics).
3. This strap configuration resets the refresh timer circuitry.

FUNCTIONAL DESCRIPTION

VL4502 consists of six basic blocks; address and select latches, refresh rate generator, refresh counter, the multiplexer, the arbiter, and the timing and control block.

ADDRESS AND SELECT LATCHES

The address and select latches allow the DRAM controller to be used in systems that multiplex address and data on the same lines without external latches. The row address latches are transparent, meaning that while ALE is HIGH, the output at MA0–MA8 follows the inputs RA0–RA8.

REFRESH RATE GENERATOR

The refresh rate generator is a counter that indicates to the arbiter that it is time for a refresh cycle. The counter divides the clock frequency according to the configuration straps as shown in Table 1. The counter is reset when a refresh cycle is requested or when TWST, FS1 and FS0 are LOW. The configuration straps allow the matching of memories to the system access time. Upon Power-Up, a reset may be accomplished by

driving all three strap inputs LOW, or by driving RESET LOW. During this reset period, at least four clock cycles should occur. (See RESET, below.)

REFRESH COUNTER

The refresh counter contains the address of the row to be refreshed. The counter is decremented after each refresh cycle. (A LOW-to-HIGH transition on TWST sets the refresh counter to 1FF₁₆ (511₁₀).

MULTIPLEXER

The multiplexer provides the DRAM array with row, column, and refresh addresses at the proper times. Its inputs are the address latches and the refresh counter. The outputs provide up to 18 multiplexed addresses on nine lines.

STATIC OPERATION

The VL4502 is designed for static operation. As a result, the user can use a CLK frequency as low as needed, as long as maximum transition times are not exceeded. As the CLK rate is changed, the refresh rate will change accordingly, in keeping with the frequency-divider specifications above.

ARBITER

The arbiter provides two operational cycles; access and refresh. The arbiter resolves conflicts between cycle requests and cycles in execution, and schedules the inhibited cycle when used in cycle-steal mode.

TIMING AND CONTROL BLOCK

The timing and control block executes the operational cycle at the request of the arbiter. It provides the DRAM array with $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ signals. It provides the CPU with a RDY signal. It controls the multiplexer during all cycles. It resets the refresh rate generator and decrements the refresh counter during refresh cycles.

RESET

The VL4502 is reset by bringing the timing straps TWST, FS1, and FS0 LOW. The refresh address is set to 1FF, internal refresh requests are synchronized, and the frequency divider is cleared. This reset can occur asynchronously with respect to CLK and control signals. In the PLCC package, the VL4502 can be reset with the $\overline{\text{RESET}}$ signal. In either case, at least four clock cycles should occur during the reset period.

ABSOLUTE MAXIMUM RATINGS

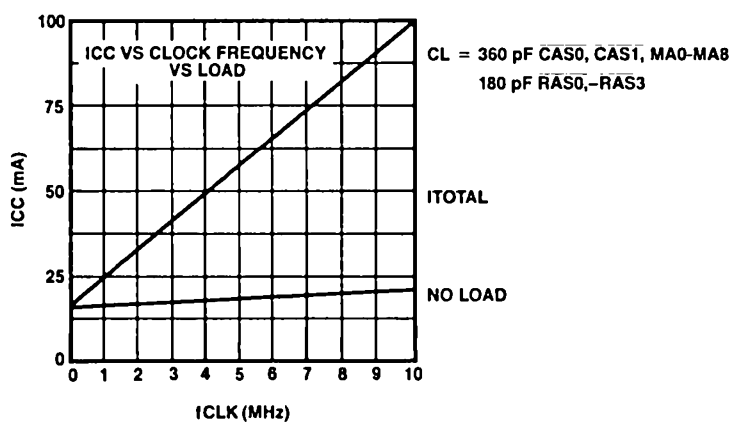
Ambient Temperature
 Under Bias -10°C to $+80^{\circ}\text{C}$
 Storage Temperature
 Range -65°C to $+140^{\circ}\text{C}$
 Supply Voltage
 Range, VCC, Note 1 -0.5 to $+7.0$ V
 Input Voltage Range
 (any input), Note 1 -0.5 to $+7.0$ V
 Continuous Power
 Dissipation 1.2 W

Stresses above those listed under
 "Absolute Maximum Ratings" may
 cause permanent damage to the
 device. These are stress ratings
 only. Functional operation of this
 device at these or any other

conditions above those indicated on
 the operational sections of this
 specification is not implied and
 exposure to absolute maximum
 rating conditions for extended
 periods may affect device reliability.

DC CHARACTERISTICS: $T_A = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$

Symbol	Parameter	Min	Typ(3)	Max	Unit	Conditions
V_{IH}	Input HIGH Voltage	2.4			V	
V_{IL} (except $\overline{\text{REFREQ}}$)	Input LOW Voltage	$V_{SS} - 0.5$		0.8	V	
V_{IL} ($\overline{\text{REFREQ}}$)	Input LOW Voltage	$V_{SS} - 0.5$		1.2	V	
V_{OH}	Output HIGH Voltage	MA0–MA8 RDY	2.4		V	$I_{OH} = -1\text{ mA}$ $V_{CC} = 4.5\text{ V}$ $I_{OH} = -100\text{ }\mu\text{A}$ $V_{CC} = 4.5\text{ V}$
		RASX, CASX	2.7			
		$\overline{\text{REFREQ}}$	2.4			
V_{OL}	Output LOW Voltage			0.4	V	$I_{OL} = 4\text{ mA}$ $V_{CC} = 4.5\text{ V}$
I_{IH}	Input HIGH Current	$\overline{\text{REFREQ}}$		100	μA	$V_I = 5.5\text{ V}$
		All Others		10		
I_{IL}	Input LOW Current	$\overline{\text{REFREQ}}$, $\overline{\text{RESET}}$		-1.25	mA	$V_I = 0\text{ V}$
		All others		-10		
I_{OZ}	Off-state Output Current			± 50	μA	$V_O = 0$ to 4.5 V $V_{CC} = 5.5\text{ V}$
$I_{CC}(4)$	Operating Supply Current DC			20	mA	$T_A = 0^{\circ}\text{C}$ $V_{CC} = 5.5\text{ V}$
CI	Input Capacitance		5		pF	$V_I = 0\text{ V}$ $f = 1\text{ MHz}$
CO	Output Capacitance		6		pF	$V_O = 0\text{ V}$ $f = 1\text{ MHz}$

GRAPH 1

Notes:

1. Voltage values are with respect to the ground terminal.
2. The algebraic convention, where the more negative limit is designated as minimum, is used in this data sheet for logic voltage levels only.
3. All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^{\circ}\text{C}$ except where otherwise noted.
4. Refer to Graph 1 for AC Power Consumption Guarantee. In testing, all inputs except CLK are held LOW.

AC CHARACTERISTICS: TA = 0°C to +70°C, VCC = 5 V ± 10%

Symbol	Parameter	VL4502-15		VL4502-20		Unit
		Min	Max	Min	Max	
tC(C)	CLK Cycle Time	100		100		ns
tW(CH)	CLK HIGH Pulse Width	25		25		
tW(CL)	CLK LOW Pulse Width	35		35		
tt	Transition Time, All Inputs		30		30	
tAEL-CL	Time Delay, ALE LOW to CLK Starting LOW, Note 1	10		10		
tCL-AEL	Time Delay, CLK LOW to ALE Starting LOW, Note 1	10		10		
tCL-AEH	Time Delay, CLK LOW to ALE Starting HIGH, Note 1	15		20		
tW(AEH)	Pulse Width ALE HIGH	50		60		
tAV-AEL	Time Delay, Address, REN _{1,2} CS Valid to ALE LOW	5		10		
tAEL-AX	Time Delay, ALE LOW to Address Not Valid	10		10		
tAEL-ACL	Time Delay, ALE LOW to ACX LOW, Notes 3, 4, 5, 6	th(RA) + 30		th(RA) + 40		
tACH-CL	Time Delay, ACX HIGH to CLK LOW, Notes 3, 7	20		20		
tACL-CH	Time Delay, ACX LOW to CLK Starting HIGH (to remove RDY)	40		40		
tRQL-CL	Time Delay, REFREQ LOW to CLK Starting LOW, Note 8	35		35		
tW(RQL)	Input Pulse Width, REFREQ LOW	20		20		

Notes:

1. Coincidence of the trailing edge of CLK and the trailing edge of ALE should be avoided as the refresh/access occurs during the interval from ACX HIGH to ALE LOW.
2. If ALE rises before ACX and a refresh request is present, the falling edge of CLK after tCL-AEH will output the refresh address to MA0–MA8 and initiate a refresh cycle.
3. These specifications relate to system timing and do not directly reflect device performance.
4. On the access grant cycle following refresh, the occurrence of $\overline{\text{CAS}}$ LOW depends on the relative occurrence of ALE LOW to $\overline{\text{ACX}}$ LOW. If $\overline{\text{ACX}}$ occurs prior to or coincident with ALE then $\overline{\text{CAS}}$ is timed from the CLK HIGH transition that causes RAS LOW. If ACX occurs 20 ns or more after ALE then $\overline{\text{CAS}}$ is timed from the CLK LOW transition following the CLK HIGH transition causing RAS LOW.
5. For maximum speed access (internal delays on both access and access grant cycles), $\overline{\text{ACX}}$ should occur prior to or coincident with ALE.
6. th(RA) is the dynamic memory row address hold time. $\overline{\text{ACX}}$ should follow ALE by tAEL-CEL in systems where the required th(RA) is greater than tREL-MAX minimum.
7. Minimum of 20 ns is specified to ensure arbitration will occur on falling CLK edge. tACH-CL also affects precharge time such that the minimum tACH-CL should be equal or greater than: tW(RH) – tW(CL) + 30 ns (for cycle where $\overline{\text{ACX}}$ HIGH occurs prior to ALE HIGH) where tW(RH) is the DRAM RAS precharge time.
8. This parameter is necessary only if refresh arbitration is to occur on this LOW-going CLK edge (in systems where refresh is synchronized to external events).

AC CHARACTERISTICS: TA = 0°C to +70°C, VCC = 5 V ± 10%

Symbol	Parameter	VL4502-15		VL4502-20		Unit
		Min	Max	Min	Max	
tAEL-REL	Time Delay, ALE LOW to RAS Starting LOW		30		40	ns
tt(REL)	RAS Fall Time		15		20	
tRAV-MAV	Time Delay, Row Address Valid to Memory Address Valid		45		50	
tAEH-MAV	Time Delay, ALE HIGH to Valid Memory Address		55		70	
tAEL-RYL	Time Delay, ALE to RDY Starting LOW (TWST = 1 or Refresh in Progress)		25		25	
tAEL-CEL	Time Delay, ALE LOW to $\overline{\text{CAS}}$ Starting LOW	60	150	70	200	
tAEH-REH	Time Delay, ALE HIGH to RAS Starting HIGH		35		35	
tt(MAV)	Address Transition Time		15		20	
tACL-MAX	Row Address Hold from $\overline{\text{ACX}}$ LOW	15		20		
tMAV-CEL	Time Delay, Memory Address Valid to $\overline{\text{CAS}}$ Starting LOW	0		0		
tt(CEL)	CAS Fall Time		15		20	
tACL-CEL	Time Delay, $\overline{\text{ACX}}$ LOW to CAS Starting LOW	50	90	65	130	
tACH-REH	Time Delay, $\overline{\text{ACX}}$ to RAS Starting HIGH		40		40	
tt(REH)	RAS Rise Time		15		20	
tACH-CEH	Time Delay, $\overline{\text{ACX}}$ HIGH to $\overline{\text{CAS}}$ Starting HIGH	5	35	10	40	
tt(CEH)	CAS Rise Time		30		35	
tACH-MAX	Column Address Hold from $\overline{\text{ACX}}$ HIGH	15		20		
tCH-RYH	Time Delay, CLK HIGH to RDY Starting HIGH (After $\overline{\text{ACX}}$ LOW), Note 9		35		45	
tRFL-RFL	Time Delay, $\overline{\text{REFREQ}}$ External Until Supported by $\overline{\text{REFREQ}}$ Internal		25		30	
tCH-RFL	Time Delay, CLK HIGH Until $\overline{\text{REFREQ}}$ Internal Starting LOW		30		35	
tCL-MAV	Time Delay, CLK LOW Until Refresh Address Valid		75		100	
tCH-RRL	Time Delay, CLK HIGH Until Refresh RAS Starting LOW	10	50	15	60	
tMAV-RRL	Time Delay, Refresh Address Valid Until Refresh RAS LOW	0		0		
tCL-RFH	Time Delay, CLK LOW to $\overline{\text{REFREQ}}$ Starting HIGH (3 Cycle Refresh)		50		55	
tCH-RFH	Time Delay, CLK HIGH to $\overline{\text{REFREQ}}$ Starting HIGH (4 Cycle Refresh)		45		55	
tCH-RRH	Time Delay, CLK HIGH to Refresh RAS Starting HIGH	5	40	10	45	
tCH-MAX	Time Delay, Refresh Address Hold After CLK HIGH	15		20		

Note:

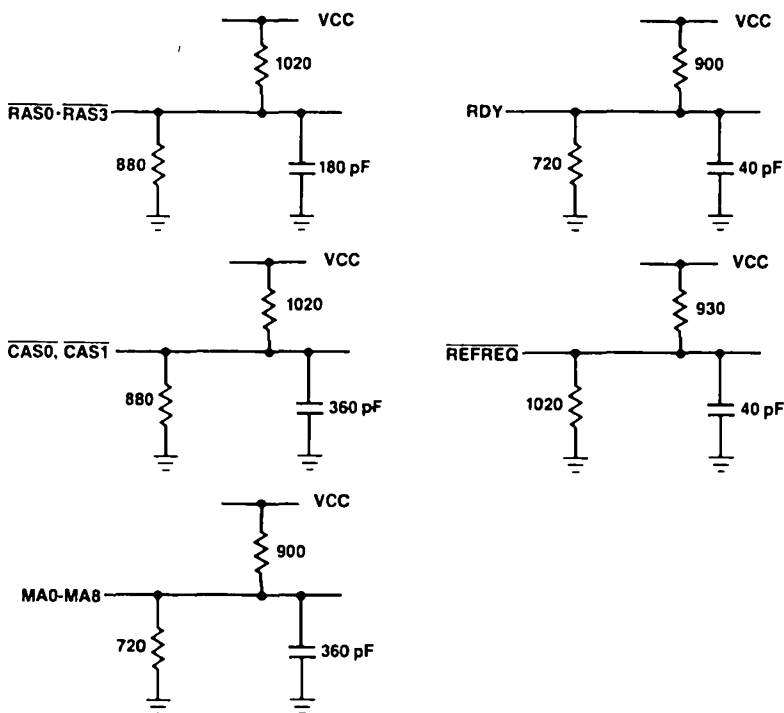
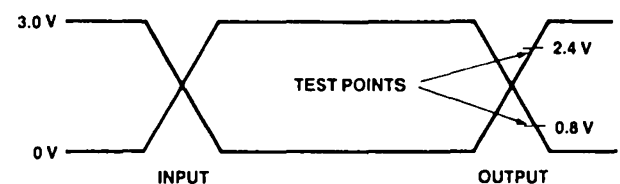
9. RDY returns HIGH on the rising edge of CLK. If TWST = 0, then on an access grant cycle RDY goes HIGH on the same edge that causes access RAS LOW. If TWST = 1, then RDY goes to the HIGH level on the first rising CLK edge after $\overline{\text{ACX}}$ goes LOW on access cycles and on the next rising edge after the edge that causes access RAS LOW on access grant cycles (assuming $\overline{\text{ACX}}$ LOW).

AC CHARACTERISTICS: $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$

Symbol	Parameter	VL4502-15		VL4502-20		Unit
		Min	Max	Min	Max	
t _{CH-REL}	Time Delay, CLK HIGH Until Access RAS Starting LOW		60		70	ns
t _{CL-CEL}	Time Delay, CLK LOW to Access CAS Starting LOW, Note 10		125		140	
t _{CL-MAX}	Row Address Hold After CLK LOW	25		30		
t _{W(ACL)}	ACX LOW Width	95		120		
t _{REL-MAX}	Row Address Hold From RAS LOW	25		30		
t _{t(RYL)}	RDY Fall Time		10		15	
t _{t(RYH)}	RDY Rise Time		20		25	
t _{dis}	Output Disable time (3-State Outputs)		100		125	
t _{AEH-MAX}	Column Address Hold From ALE HIGH	10		15		
t _{en}	Output Enable Time (3-State Outputs)		65		80	
t _{CAV-CEL}	Column Address Setup to CAS After Refresh	0		0		
t _{CH-CEL}	Time Delay, CLK HIGH to Access CAS Starting LOW, Note 9		140		180	
t _{RESET}	Power Up RESET	Four (4) Clock Cycles				

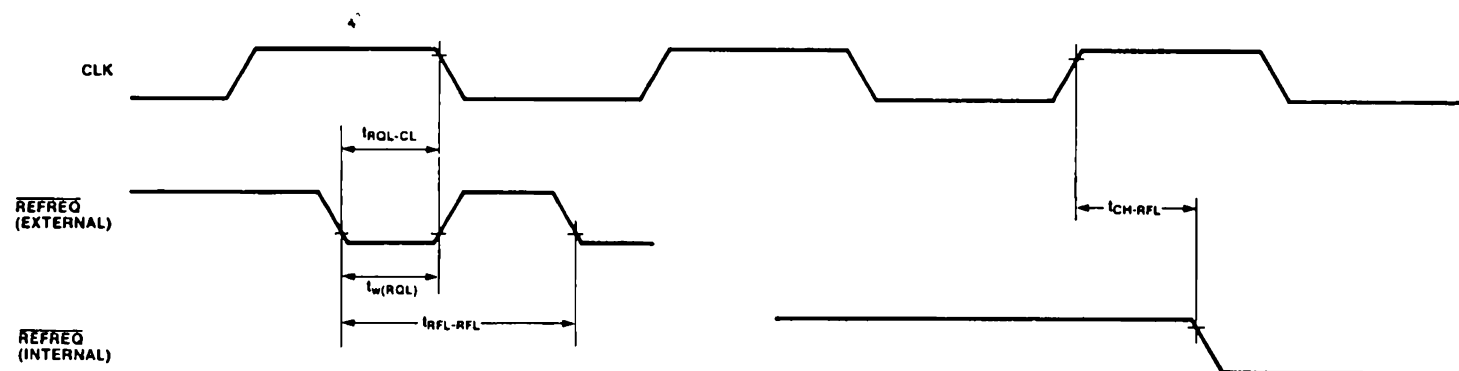
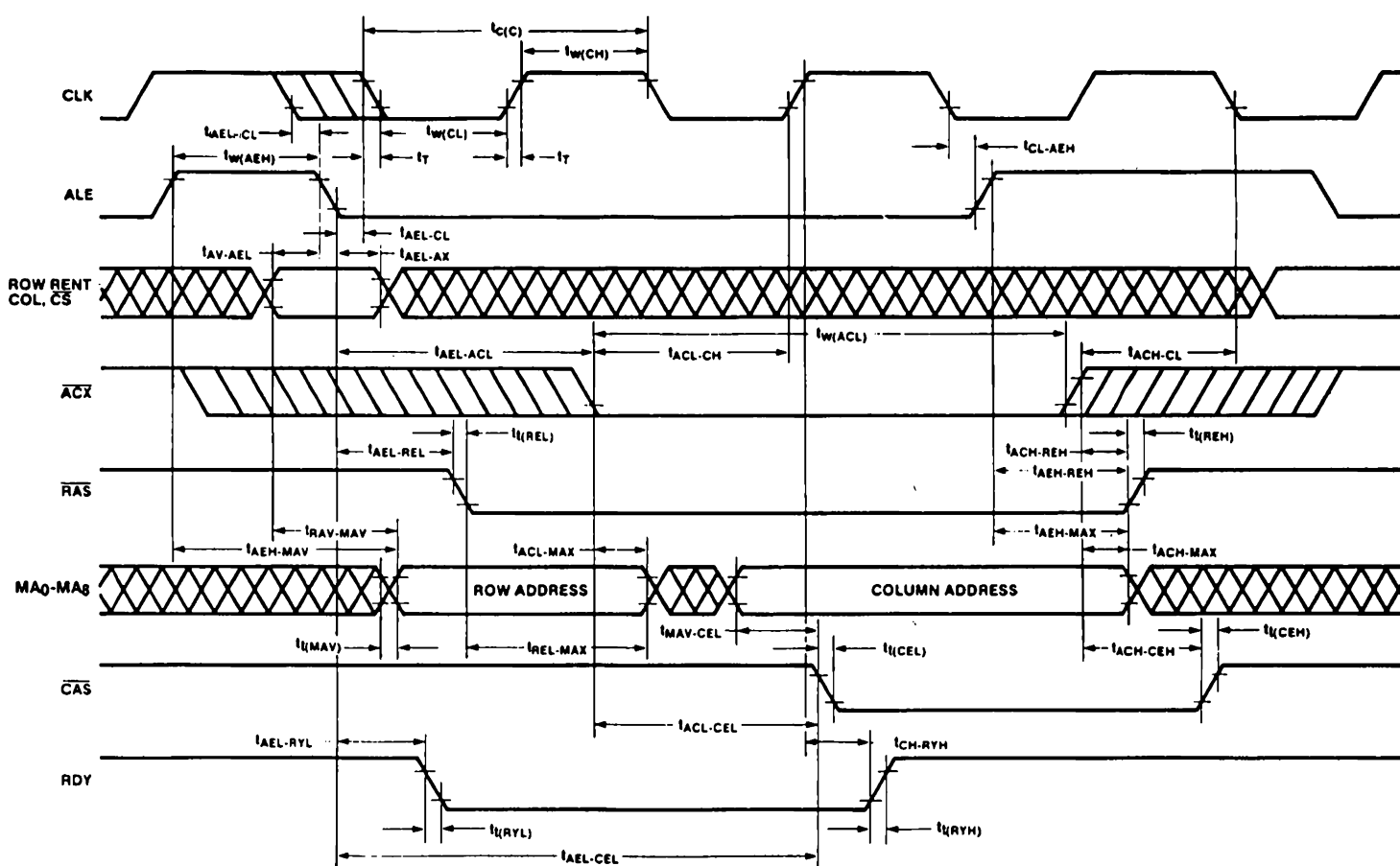
Notes:

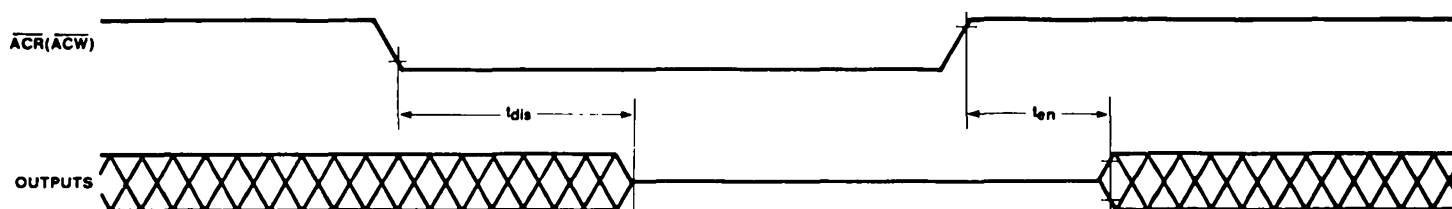
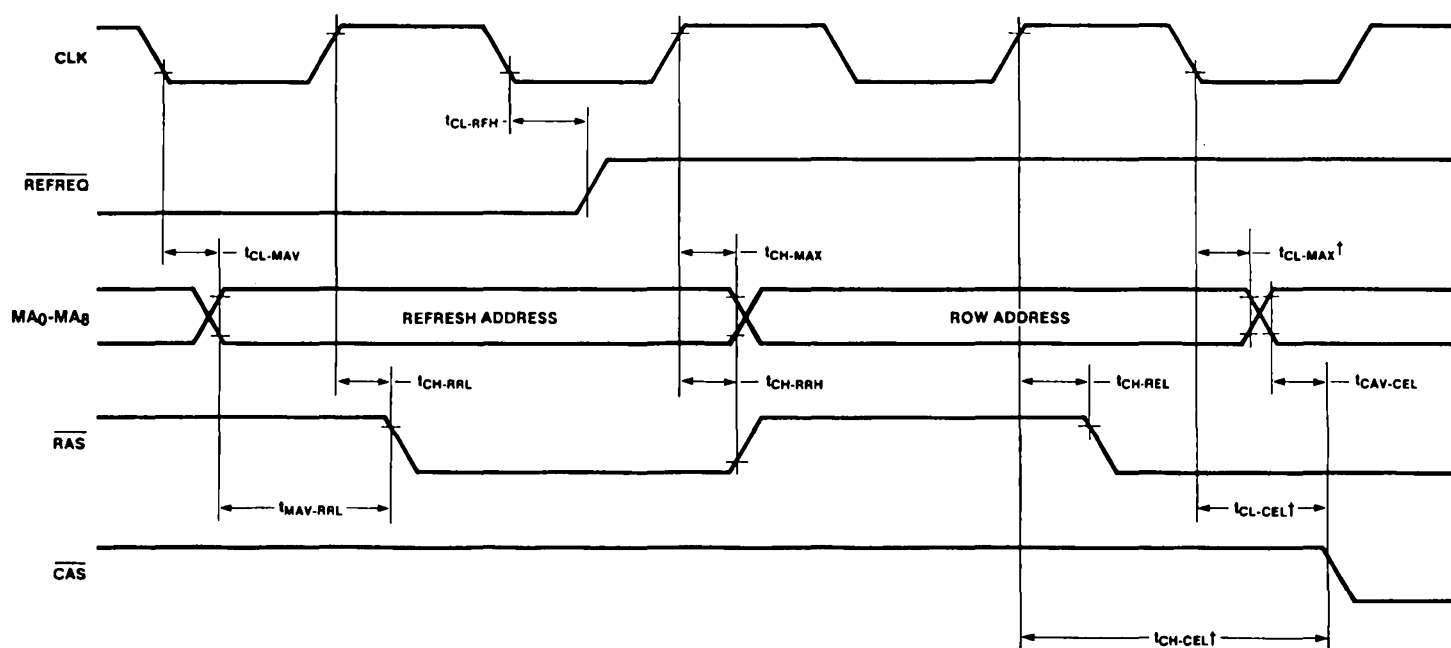
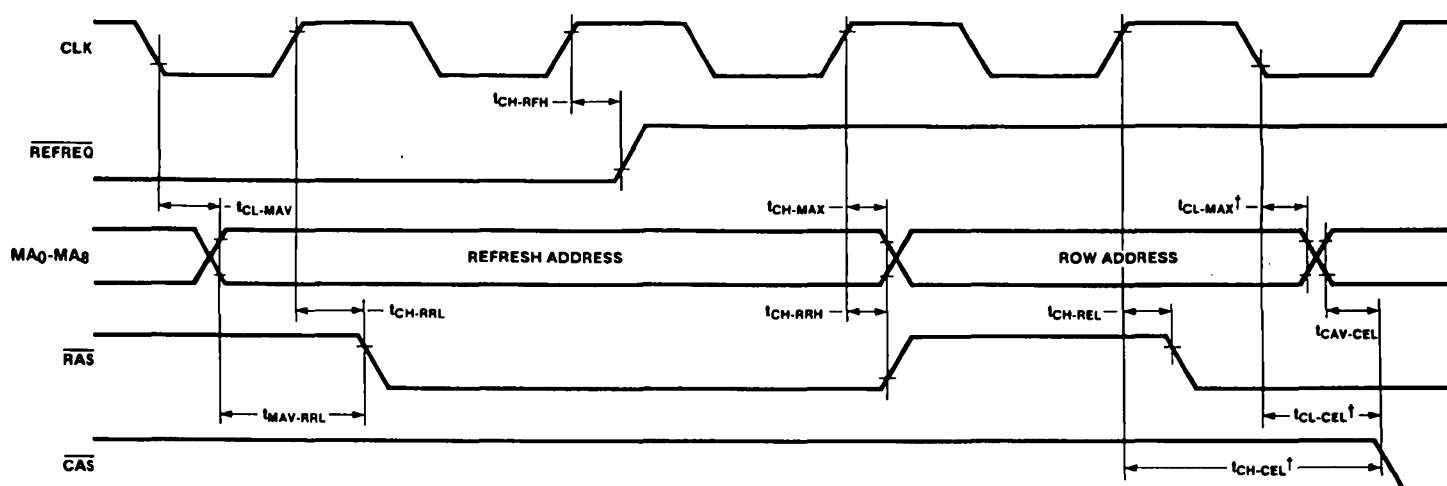
10. On the access grant cycle following refresh, the occurrence of CAS LOW depends on the relative occurrence of ALE LOW to ACX LOW. If ACX occurs prior to or coincident with ALE then CAS is timed from the CLK LOW transition that causes RAS LOW. If ACX occurs 20 ns or more after ALE then CAS is timed from the CLK LOW transition following the CLK HIGH transition causing RAS LOW.

OUTPUT LOAD CONDITIONS: $V_{CC} = 5.0\text{ V}$

AC TESTING INPUT, OUTPUT WAVEFORM


AC TESTING INPUTS ARE DRIVEN AT 3.0 V FOR A LOGIC "1" AND 0.0 V FOR A LOGIC "0". TIMING MEASUREMENTS ARE MADE AT 2.4 V FOR A LOGIC "1" AND 0.8 V FOR A LOGIC "0" AT THE OUTPUTS.

ACCESS CYCLE TIMING

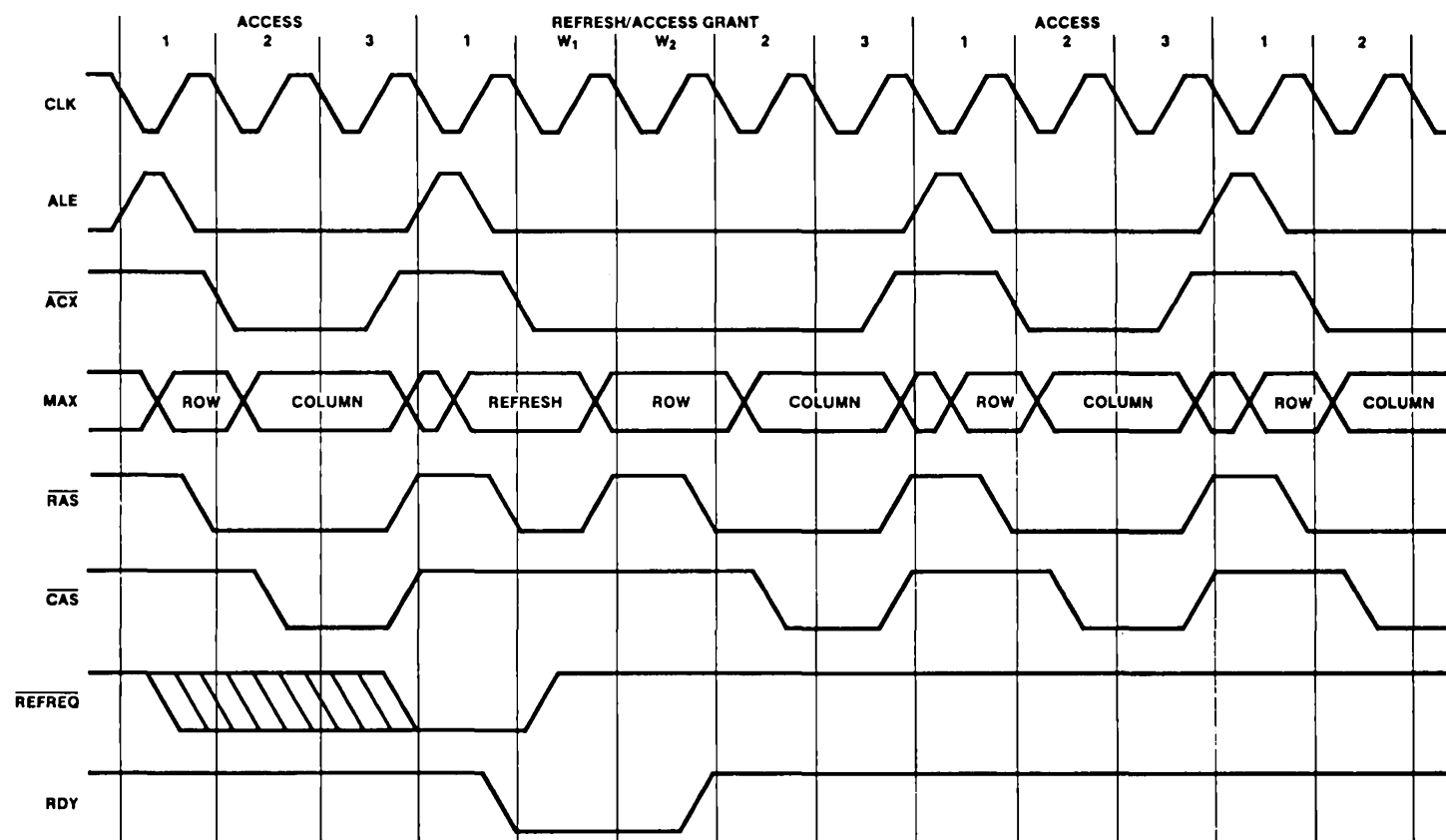


TIMING DIAGRAMS (Cont.)
OUTPUT 3-STATE TIMING

REFRESH CYCLE TIMING (3-CYCLE)

REFRESH CYCLE TIMING (4-CYCLE)


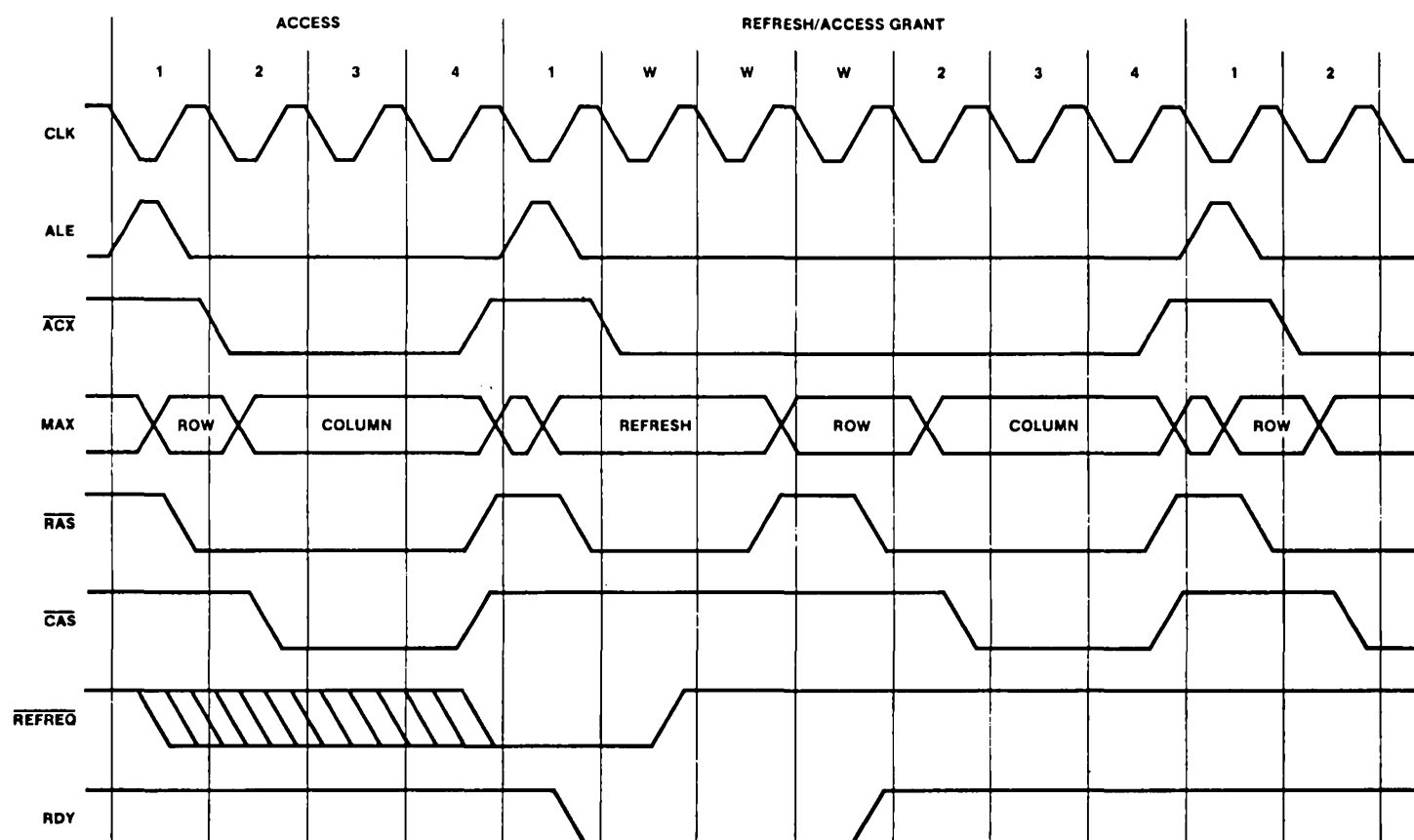
ON THE ACCESS GRANT CYCLE FOLLOWING REFRESH, THE OCCURRENCE OF $\overline{\text{CAS}}$ LOW DEPENDS ON THE RELATIVE OCCURRENCE OF ALE LOW TO $\overline{\text{ACX}}$ LOW. IF $\overline{\text{ACX}}$ OCCURS PRIOR TO OR COINCIDENT WITH ALE THEN $\overline{\text{CAS}}$ IS TIMED FROM THE CLK HIGH TRANSITION THAT CAUSES $\overline{\text{RAS}}$ LOW. IF $\overline{\text{ACX}}$ OCCURS 20 NS OR MORE AFTER ALE THEN $\overline{\text{CAS}}$ IS TIMED FROM THE CLK LOW TRANSITION FOLLOWING THE CLK HIGH TRANSITION CAUSING $\overline{\text{RAS}}$ LOW.

TIMING DIAGRAMS (Cont.)

TYPICAL ACCESS/REFRESH/ACCESS CYCLE (3-CYCLE, TWST = 0)

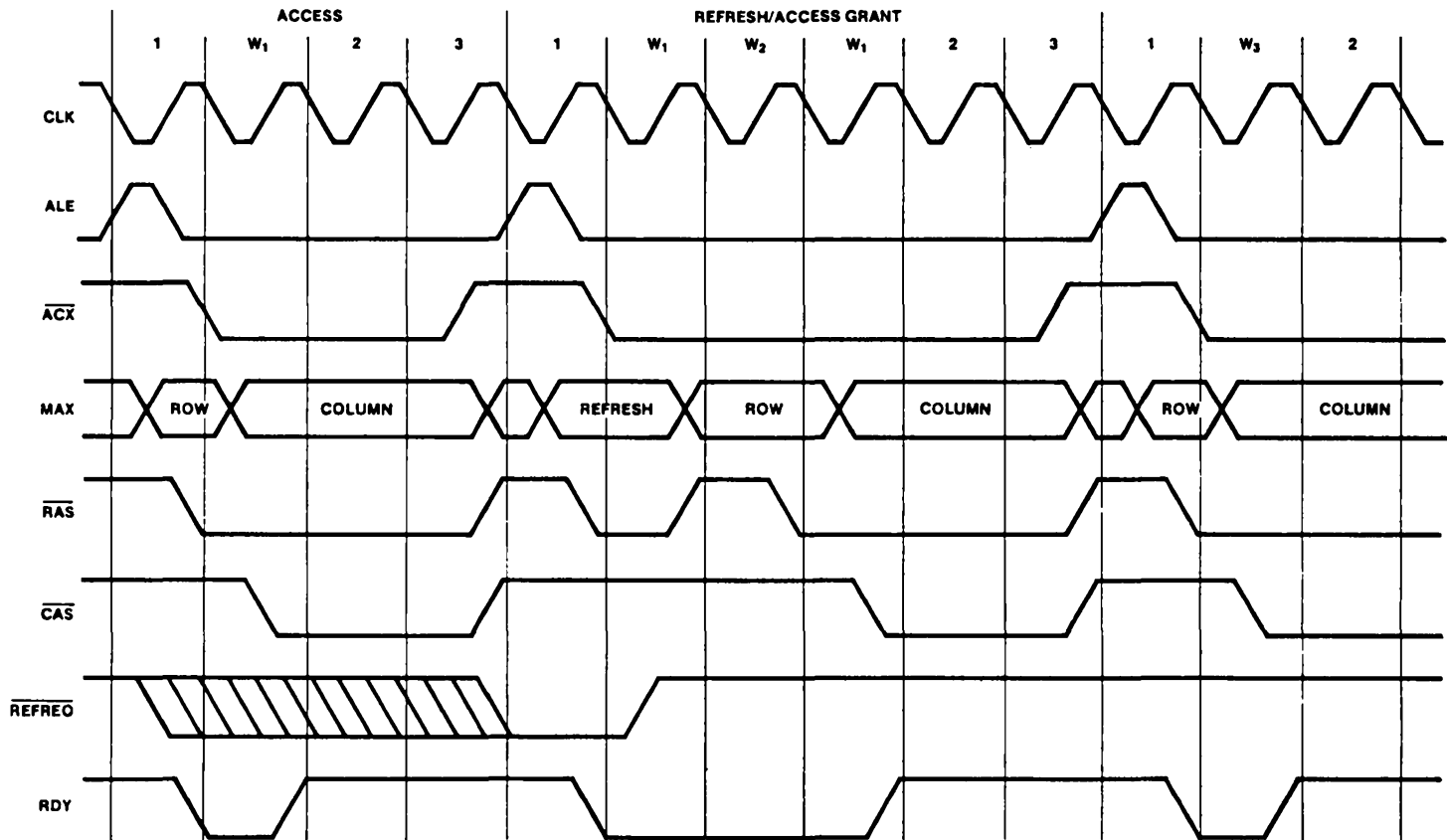


TYPICAL ACCESS/REFRESH/ACCESS CYCLE (4-CYCLE, TWST = 0)

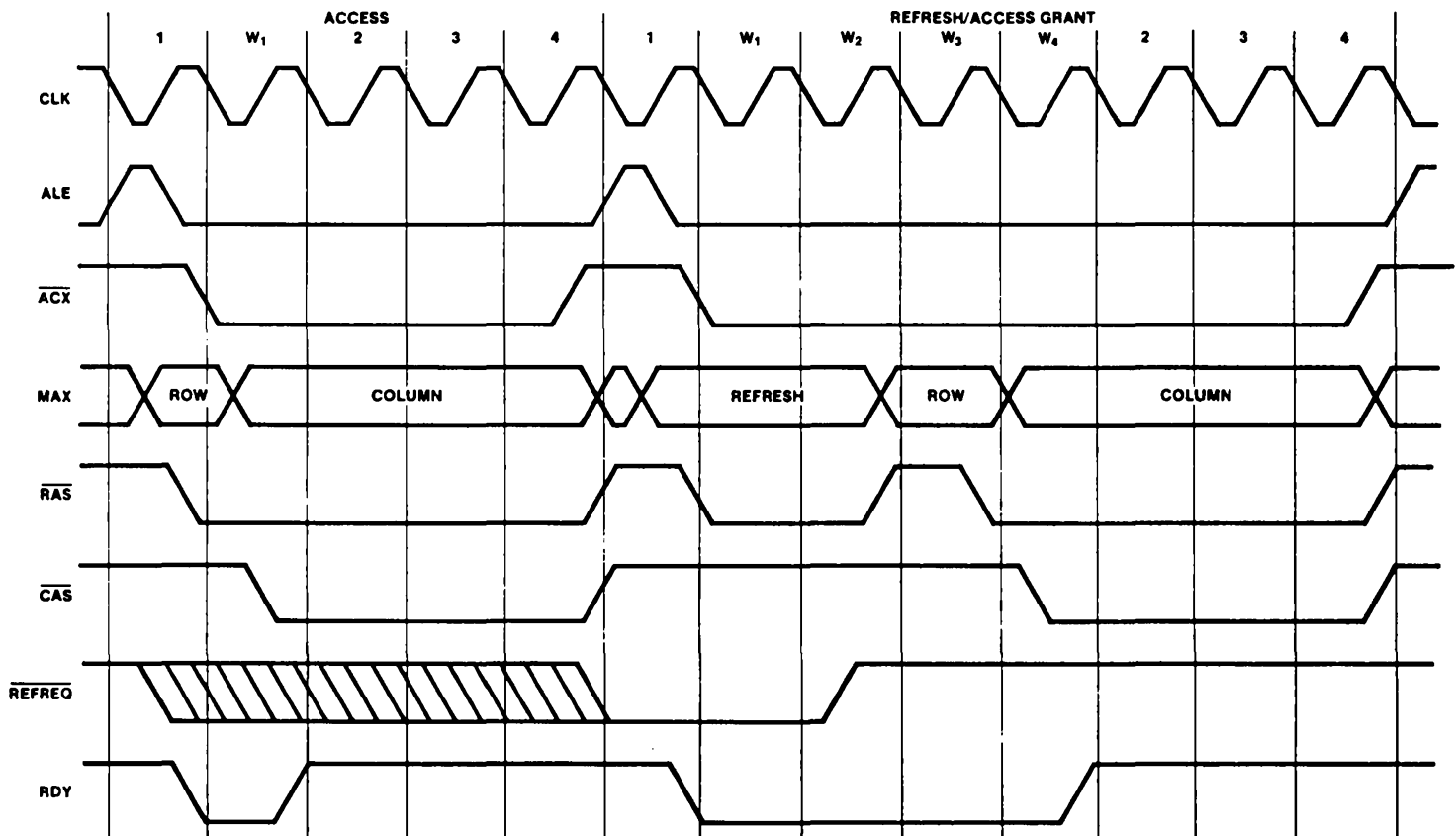


TIMING DIAGRAMS (Cont.)

TYPICAL ACCESS/REFRESH/ACCESS CYCLE (3-CYCLE, TWST = 1)

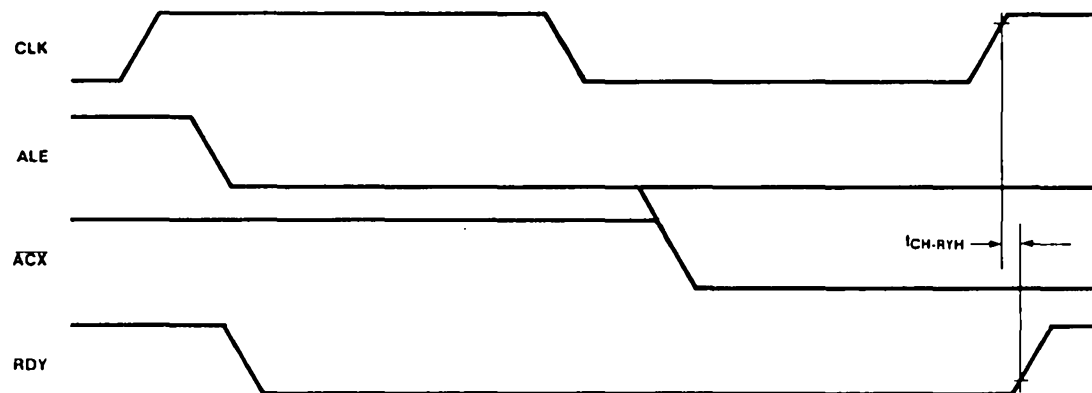


TYPICAL ACCESS/REFRESH/ACCESS CYCLE (4-CYCLE, TWST = 1)





READY (RDY) SIGNAL TIMING (WAIT STATE OPERATION, TWST = 1)



RDY starting HIGH is timed from CLK HIGH (t_{CH-RYH})

.

SMALL COMPUTER SYSTEM INTERFACE (SCSI)

FEATURES

SCSI INTERFACE

- Interface to 1.5M bps (asynchronous)
- Supports initiator and target roles
- Parity generation with optional checking
- Arbitration support
- Direct control of all bus signals
- High current outputs drive SCSI bus

MPU INTERFACE

- Memory or I/O mapped interface
- DMA of programmed I/O
- Normal or block mode DMA
- Optional MPU interrupts

DESCRIPTION

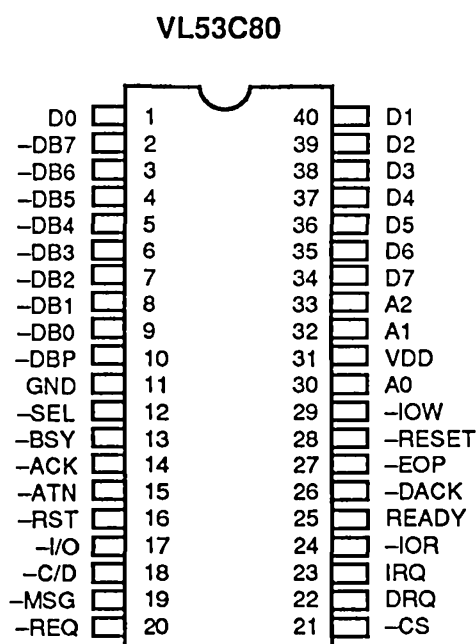
The VLSI Technology VL53C80 SCSI device is a 40-pin CMOS device designed to accommodate the Small Computer Systems Interface (SCSI) as defined by the ANSI X3T9.2 committee. The VL53C80 operates as both the initiator and the target and can therefore be used in host adapter, host port, and formatter designs. This device supports arbitration, including reselection. Special high-current open-collector output drivers, capable of sinking 48 mA at 0.5 V, connect directly to the SCSI bus.

The VL53C80 interfaces with the system microprocessor as a peripheral.

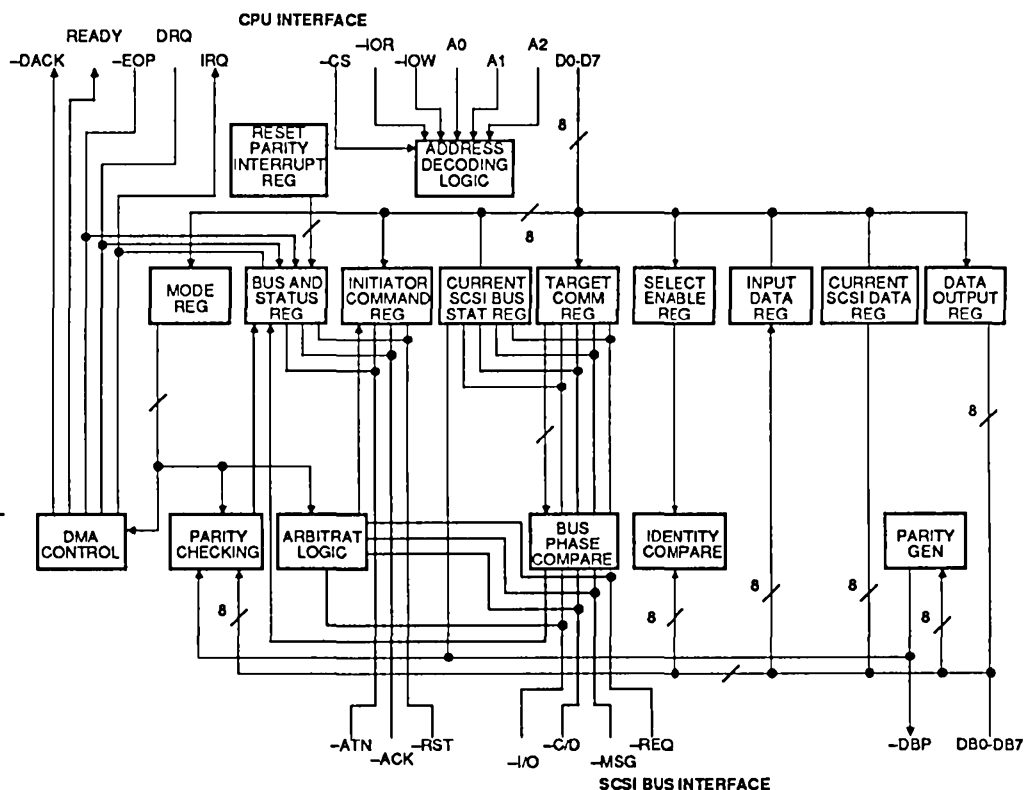
The device is controlled by reading and writing several internal registers which are addressed as standard or memory mapped I/O. DMA transfers require little CPU support because the VL53C80 controls the necessary handshake signals. The VL53C80 interrupts the MPU when it detects a bus condition requiring service. Normal and block mode DMA is also available to match several popular DMA controllers.

The VL53C80 is available in a 40-pin plastic or ceramic DIP as well as a 44-pin plastic leaded chip carrier.

PIN DIAGRAM



BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Package
VL53C80-PC	Plastic DIP
VL53C80-CC	Ceramic DIP
VL53C80-QC	Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range is 0°C to +70°C.

SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Type	Signal Description
D0-D7	1, 40-47	I/O*	Three-state microprocessor data bus lines. Active high when an output.
A0-A2	30, 32, 33	I*	These signals are used with $\overline{\text{CS}}$, $\overline{\text{IOR}}$, or $\overline{\text{IOW}}$ to address the internal registers.
$\overline{\text{RESET}}$	28	I*	Reset - Clears all registers. It does not force the SCSI signal $\overline{\text{RST}}$ to the active state. $\overline{\text{RESET}}$ is active low.
$\overline{\text{EOP}}$	27	I*	End Of Process - Used to terminate a DMA transfer. If asserted during a DMA cycle, the current byte will be transferred but no additional bytes will be requested.
$\overline{\text{IOR}}$	24	I*	I/O Read - Used to read an internal register selected by $\overline{\text{CS}}$ and A0-A2. It also selects the Input Data Register when used with $\overline{\text{DACK}}$. $\overline{\text{IOR}}$ is active low.
$\overline{\text{IOW}}$	29	I*	I/O Write - Used to write an internal register selected by $\overline{\text{CS}}$ and A0-A2. When used with $\overline{\text{DACK}}$ it selects the Output Data Register. $\overline{\text{IOW}}$ is active low.
$\overline{\text{CS}}$	21	I*	Chip Select - An active low signal that enables a read or write of the internal register selected by address lines A0-A2.
$\overline{\text{DACK}}$	26	I*	DMA Acknowledge - This active low signal resets DRQ and selects the data register for input or output of data transfers.
IRQ	23	O*	Interrupt Request - Informs the microprocessor of an error condition or an event completion.
DRQ	22	O*	DMA Request - Indicates that the data register is ready to be read or written. DRQ occurs only if DMA mode is true in the Command Register. It is cleared by $\overline{\text{DACK}}$.
READY	25	O*	Ready - Can be used to control the speed of block mode DMA transfers. It goes active to indicate the chip is ready to send/receive data and remains false after a transfer until the last byte is sent or until the DMA Mode bit is reset.
VDD	31		+5 V.
GND	11		Ground.

*All pins interface directly with the microprocessor.

SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Type	Signal Description
–ACK	14	I/O*	Acknowledge - Driven by an initiator, –ACK shows an acknowledgment for a REQ/ACK data transfer handshake. In the target role, –ACK is received as a response to the –REQ signal.
–ATN	15	I/O*	Attention - Driven by an initiator, –ATN indicates an attention condition. This signal is received in the target role.
–BSY	13	I/O*	Busy - Indicates that the SCSI bus is being used and can be driven by both the initiator and the target device.
–C/D	18	I/O*	Control or Data - Driven by the target, –C/D indicates Control or Data information is on the data bus. It is received by the initiator.
–DB0- –DB7, –DBP	9-2, 10	I/O*	Data Bus - These eight data bits (–DB0- –DB7), plus a parity bit (–DBP) form the data bus. –DB7 is the most significant bit and has the highest priority during the Arbitration phase. Data parity is odd. Parity is always generated and optionally checked. Parity is not valid during arbitration.
–I/O	17	I/O*	Input/Output - Driven by a target which controls the direction of data movement on the SCSI bus. True (low) indicates input to the initiator. It is also used to distinguish between Selection and Reselection phases.
–MSG	19	I/O*	Message - Received by the initiator, and driven by the target during the Message phase.
–REQ	20	I/O*	Request - Driven by a target, –REQ indicates a request for a REQ/ACK data transfer handshake. It is received by the initiator.
–RST	16	I/O*	Reset - Indicates an SCSI bus reset condition.
–SEL	12	I/O*	Select - Used by an initiator to select a target or by a target to reselect an initiator.

*Bidirectional, active low, open collector signals with 48 mA sink capability. All pins interface directly with the SCSI bus.

FUNCTIONAL DESCRIPTION

The VL53C80 Small Computer Systems Interface (SCSI) device is seen as a set of eight registers to the controlling MPU. By reading and writing the correct registers, the MPU may start any SCSI Bus function or may sample and assert any signal on the SCSI Bus. This permits the user to use all or portions of the SCSI protocol in software. These registers are read (written) by activating $\overline{\text{CS}}$ with an address on A0-A2, and then issuing an $\overline{\text{IOR}}$ ($\overline{\text{IOW}}$) pulse. The following section will describe the operation of the internal registers.

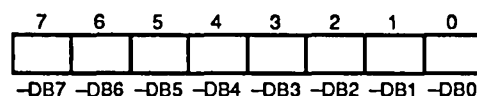
SCSI signal names are used to define the contents of the internal registers. Even though the bus is active low, a one (1) is used to indicate signal assertion and a zero (0) is used to indicate the inactive state. See Table 1.

DATA REGISTERS

The data registers are used for the transfer of SCSI commands, data, status, and message bytes between the microprocessor Data Bus and the SCSI Bus. The VL53C80 does not handle any information that passes through the data registers. The data registers consist of the transparent Current SCSI Data Register, the Output Data Register, and the Input Data Register.

Current SCSI Data Register

Address 0 (Read Only) - The Current SCSI Data Register is a read only register which permits the microprocessor to read the active SCSI Data Bus. This is done by activating $\overline{\text{CS}}$ with an address on A2-A0 of 000, and issuing an $\overline{\text{IOR}}$ pulse. If parity checking is enabled, the SCSI Bus parity is checked at the beginning of the read cycle. This register is active during a programmed I/O data read, or during Arbitration to inspect for higher priority arbitrating devices. Parity is not assured valid during Arbitration.



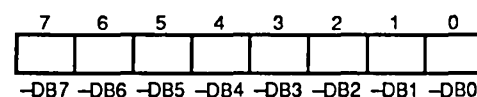
Output Data Register

Address 0 (Write Only) - The Output Data Register is a write only register that is used to send data to the SCSI Bus. This done by either using a

TABLE 1. REGISTER SUMMARY

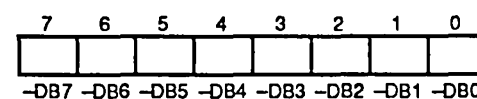
Address			R/W	Register Name
A2	A1	A0		
0	0	0	R	Current SCSI Data
0	0	0	W	Output Data
0	0	1	R/W	Initiator Command
0	1	0	R/W	Mode
0	1	1	R/W	Target Command
1	0	0	R	Current SCSI Bus Status
1	0	0	W	Select Enable
1	0	1	R	Bus and Status
1	0	1	W	Start DMA Send
1	1	0	R	Input Data
1	1	0	W	Start DMA Target Receive
1	1	1	R	Reset Parity/Interrupts
1	1	1	W	Start DMA Initiator Receive

normal MPU write, or under DMA control, by using $\overline{\text{IOW}}$ and $\overline{\text{DACK}}$. This register is further used to assert the correct ID bits on the SCSI Bus during the Arbitration and Selection phases.



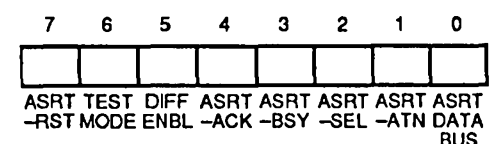
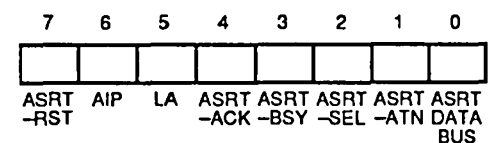
Input Data Register

Address 6 (Read Only) - The Input Data Register is a read only register that is used to read latched data from the SCSI Bus. Data is latched either during a DMA Target receive operation as $\overline{\text{ACK}}$ goes active, or during a DMA Initiator receive when $\overline{\text{REQ}}$ goes active. The DMA Mode bit (port 2, bit 1) is to be set before data can be latched in the Input Data Register. This register may be read under DMA control using $\overline{\text{IOR}}$ and $\overline{\text{DACK}}$. Parity may be checked when the Input Data Register is loaded, if desired.



Initiator Command Register

Address 1 (Read/Write) - The Initiator Command Register is a read/write register that is used to assert some SCSI Bus signals, to monitor those signals, and to monitor the progress of bus arbitration. Many of these bits are significant only when being used as an Initiator. However, most can be used during Target role operation. Values for the Read and Write registers are shown below, respectively.



The following is a description of the operation of all bits in the Initiator Command Register.

Bit 7 - Assert $\overline{\text{RST}}$ - Whenever a one (1) is written to bit 7 of the Initiator Command Register, the $\overline{\text{RST}}$ signal is



asserted on the SCSI Bus. The -RST signal stays asserted until this bit is reset or an external -RESET occurs. After this bit is set (1), IRQ goes active. Then, all internal logic and control registers are reset (except for the interrupt latch and the Assert -RST bit). Writing a zero (0) to bit 7 of the Initiator Command Register releases the -RST signal. Reading this register shows the status of this bit.

Bit 6 - AIP (Arbitration in Progress) (Read Bit) - This bit is used to determine if arbitration is in progress. For this bit to be active, the Arbitrate bit (port 2, bit 0) must have been previously set. It indicates that a "bus free" condition has been detected, that the chip has asserted -BSY , and the contents of the Output Data Register (port 0) onto the SCSI Bus. AIP will remain active until the Arbitrate bit is reset.

Bit 6 - Test Mode (Write Bit) - This bit may be written during a test environment to disable all output drivers, thereby removing the VL53C80 from the circuit. Resetting this bit returns the device to normal operation.

Bit 5 - LA (Lost Arbitration) (Read Bit) - This bit, when active, indicates that the VL53C80 has found a bus free condition, arbitrated for use of the bus by asserting -BSY and its ID on the Data Bus, and lost Arbitration due to -SEL being asserted by another bus device. For this bit to be active, the Arbitrate bit (port 2, bit 0) must be active.

Bit 5 - DIFF ENBL (Differential Enable) (Write Bit) - This bit must be written with a zero (0) for proper operation.

Bit 4 - Assert -ACK - This bit is used by the bus initiator to assert -ACK on the SCSI Bus. To assert -ACK , the Target Mode bit (port 2, bit 6) must be false. Writing a zero (0) to this bit resets -ACK on the SCSI Bus. Reading this register simply reflects the status of this bit.

Bit 3 - Assert -BSY - Writing a one (1) into this bit position asserts -BSY onto the SCSI Bus. Conversely, a zero (0) resets the -BSY signal. Asserting -BSY indicates a successful selection or reselection and resetting this bit creates a bus disconnect condition.

Reading this register simply reflects the status of this bit.

Bit 2 - Assert -SEL - Writing a one (1) into this bit position asserts -SEL onto the SCSI Bus. -SEL is normally asserted after Arbitration has been correctly completed. -SEL may be released by resetting this bit to a zero (0). A read of this register shows the status of this bit.

Bit 1 - Assert -ATN - -ATN may be asserted on the SCSI Bus by setting this bit to a one (1) if the Target Mode bit (port 2, bit 6) is false. -ATN is normally asserted, by the initiator, to request a Message Out bus phase. Note that since Assert -SEL and Assert -ATN are in the same register, a select with -ATN may be implemented with one MPU write. -ATN may not be asserted by resetting this bit to zero (0). A read of this register simply reflects the status of this bit.

Bit 0 - Assert Data Bus - The Assert Data Bus bit, when set, allows the contents of the Output Data Register to be enabled as chip outputs on the signals -DB0 through -DB7 . Parity is generated and asserted on -DBP also.

Connected as an Initiator, the outputs are only enabled if the Target Mode bit (port 2, bit 6) is false, the received signal -I/O is false, and the phase signals (-C/D , -I/O , and -MSG) match the contents of the Assert -C/D , Assert -I/O , and Assert -MSG in the Target Command Register.

This bit should also be set during DMA send operations.

Mode Register Address 2 (Read/Write)

The Mode Register is used to control the operation of the chip. This register decides whether the VL53C80 operates as an Initiator or a Target, whether DMA transfers are being used, whether parity is checked, and whether interrupts are generated on various external conditions. This register may be read to inspect the value of these internal control bits. The operation of these control bits are shown below.

7	6	5	4	3	2	1	0
<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
BLK MODE	TAR- GET	EN PAR	EN PAR	EN EOP	MONI- TOR	DMA MODE	ARB
		DMA	MODECHKG	INT	INT	BSY	

Bit 7 - Block Mode DMA - The Block Mode DMA bit controls the characteristics of the DMA DRQ/-DACK handshake. When this bit is reset (0), and the DMA Mode bit is active (1), the DMA handshake uses the normal interlocked handshake. The rising edge of -DACK shows the end of each byte being transferred. In block mode operations, Block Mode DMA bit set (1) and DMA Mode bit set (1), the end of -IOR or -LOW signifies the end of each byte transferred and -DACK is allowed to remain active throughout the DMA operation. READY can then be used to request the next transfer.

Bit 6 - Target Mode - The Target Mode bit allows the VL53C80 to operate as either an SCSI Bus Initiator, bit reset (0), or as an SCSI bus Target device, bit set (1). In order for the signals -ATN and -ACK to be asserted on the SCSI Bus, the Target Mode bit must be reset (0). In order for the signals -DC , -I/O , -MSG , and -REQ to be asserted on the SCSI Bus, the Target Mode bit should be set (1).

Bit 5 - Enable Parity Checking - The Enable Parity Checking bit decides whether parity errors will be ignored or saved in the parity error latch. If this bit is reset (0), parity will be ignored; if this bit is set (1), parity errors will be saved.

Bit 4 - Enable Parity Interrupt - The Enable Parity Interrupt bit, when set (1), will cause an interrupt (IRQ) to occur if a parity error is detected. A parity interrupt will only be generated if the Enable Parity Checking bit (bit 5) is also enabled (1).

Bit 3 - Enable EOP Interrupt - The Enable EOP Interrupt, when set (1), causes an interrupt to occur when an -EOP (End of Process) signal is received from the DMA controller logic.

Bit 2 - Monitor Busy - The Monitor Busy bit, when true (1) causes an interrupt to be generated for an unplanned loss of -BSY . When the interrupt is generated due to loss of -BSY , the lower six bits of the Initiator Command Register are reset (0) and all signals are removed from the SCSI Bus.

Bit 1 - DMA Mode - The DMA Mode bit is normally used to enable a DMA transfer and must be set (1) prior to

writing ports 5 through 7. Ports 5 through 7 are used to initiate DMA transfers. The Target Mode bit (port 2, bit 6) must be consistent with writes to port 6 and 7 (i.e., set (1) for a write to port 6 and reset (0) for a write to port 7). The control bit Assert Data Bus (port 1, bit 0) must be true (1) for all DMA send operations. In the DMA mode, $\overline{\text{REQ}}$ and $\overline{\text{ACK}}$ are controlled automatically.

The DMA Mode bit is not reset when the receipt of an $\overline{\text{EOP}}$ signal occurs. Any DMA transfer may be stopped by writing a zero (0) into this bit. Care must be taken not to cause $\overline{\text{CS}}$ and $\overline{\text{DACK}}$ to become active simultaneously. $\overline{\text{BSY}}$ must be active to set the DMA Mode bit.

Bit 0 - Arbitrate - The Arbitrate bit is set (1) to start the Arbitration process. Prior to setting this bit, the Output Data Register should contain the proper SCSI device ID value. Only one data bit should be active for SCSI Bus arbitration. The VL53C80 will wait for a bus free condition before entering the arbitration phase. The results of the arbitration phase are determined by reading the status bits LA and AIP (port 1, bits 5 and 6, respectively).

Target Command Register

Address 3 (Read/Write) - When connected as a target device, the Target Command Register allows the MPU to control the SCSI Bus Information Transfer phase and also to assert $\overline{\text{REQ}}$ simply by writing this register. The Target Mode bit (port 2, bit 6) must be true (1) for bus assertion to occur. The SCSI Bus phases are described in Table 2.

When connected as an Initiator with DMA Mode true and if the phase lines ($\overline{\text{I/O}}$, $\overline{\text{C/D}}$, and $\overline{\text{MSG}}$) do not match the phase bits in the Target Command Register, a phase mismatch interrupt is caused when $\overline{\text{REQ}}$ goes active. In order to send data as an Initiator, the Assert $\overline{\text{I/O}}$, Assert $\overline{\text{C/D}}$, and Assert $\overline{\text{MSG}}$ bits must match the corresponding bits in the Current SCSI Bus Status Register (port 4). The Assert $\overline{\text{REQ}}$ bit (bit 3) has no meaning when operating as an Initiator.

7	6	5	4	3	2	1	0
<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
X	X	X	X	ASRT	ASRT	ASRT	ASRT
				$\overline{\text{REQ}}$	$\overline{\text{MSG}}$	$\overline{\text{C/D}}$	$\overline{\text{I/O}}$

TABLE 2. SCSI INFORMATION TRANSFER PHASES

Bus Phase	Assert $\overline{\text{I/O}}$	Assert $\overline{\text{C/D}}$	Assert $\overline{\text{MSG}}$
Data Out	0	0	0
Unspecified	0	0	1
Command	0	1	0
Message Out	0	1	1
Data In	1	0	0
Unspecified	1	0	1
Status	1	1	0
Message In	1	1	1

The VL53C80 uses bit 7 of this register to determine when the last byte of DMA transfer is sent to the SCSI Bus. This flag is needed since the End of DMA bit in the Bus and Status Register only display when the last byte was received from the DMA.

Current SCSI Bus Status Register

Address 4 (Read Only) - The Current SCSI Bus Status Register is a read only register which is used to monitor seven SCSI Bus control signals plus the Data Bus parity bit. An Initiator device can use this register to determine the current bus phase and poll $\overline{\text{REQ}}$ for pending data transfers. This register may also be used to determine why a certain interrupt occurred. Values for the Current SCSI Bus Status Register are shown below.

7	6	5	4	3	2	1	0
<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
$\overline{\text{RST}}$	$\overline{\text{BSY}}$	$\overline{\text{REQ}}$	$\overline{\text{MSG}}$	$\overline{\text{C/D}}$	$\overline{\text{I/O}}$	$\overline{\text{SEL}}$	$\overline{\text{DBP}}$

Select Enable Register

Address 4 (Write Only) - The Select Enable Register is a write only register which is used as a mask to monitor a signal ID during a selection attempt. The simultaneous occurrence of the correct ID bit, $\overline{\text{BSY}}$ false, and $\overline{\text{SEL}}$ true will cause an interrupt. This interrupt can be disabled by resetting all bits in this register. If the Enable Parity Checking bit (port 2, bit 5) is active (1), parity will be examined during selection.

7	6	5	4	3	2	1	0
<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
$\overline{\text{DB7}}$	$\overline{\text{DB6}}$	$\overline{\text{DB5}}$	$\overline{\text{DB4}}$	$\overline{\text{DB3}}$	$\overline{\text{DB2}}$	$\overline{\text{DB1}}$	$\overline{\text{DB0}}$

Bus and Status Register

Address 5 (Read Only) - The Bus and Status Register is a read only register which may be used to monitor the remaining SCSI control signals not found in the Current SCSI Bus Status Register ($\overline{\text{ATN}}$ and $\overline{\text{ACK}}$), and six other status bits. Below is a description of each bit of the Bus and Status Register.

7	6	5	4	3	2	1	0
<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
END OF DMA	DMA RQST	PAR ERR	INT RQST	\emptyset MCH	$\overline{\text{BSY}}$ ERR	$\overline{\text{ATN}}$	$\overline{\text{ACK}}$
			ACT				

Bit 7 - End of DMA Transfer - The End of DMA Transfer bit is set if $\overline{\text{EOP}}$, $\overline{\text{DACK}}$, and either $\overline{\text{IOR}}$ or $\overline{\text{IOW}}$ are both active for at least 100 ns. Since the $\overline{\text{EOP}}$ signal can occur during the last byte sent to the Output Data Register (port 0), the $\overline{\text{REQ}}$ and $\overline{\text{ACK}}$ signals must be monitored to insure that the last byte has been transferred. This bit is reset when the DMA Mode bit is reset (0) in the Mode Register (port 2).

Bit 6 - DMA Request - The DMA Request bit permits the MPU to sample the output pin DRQ. DRQ can be cleared by asserting $\overline{\text{DACK}}$ or by resetting the DMA Mode bit (bit 1) in the Mode Register (port 2). The DRQ signal does not reset when a phase mismatch interrupt occurs.

Bit 5 - Parity Error - This bit is set if a parity error occurs during a data receive or a device selection. The Parity Error bit can only be set (1) if the Enable



Parity Check bit (port 2, bit 5) is active (1). This bit may be cleared by reading the Reset Parity/Interrupt Register (port 7).

Bit 4 - Interrupt Request Active - This bit is set if an enabled interrupt condition occurs. It reflects the current state of the IRQ output and can be cleared by reading the Reset Parity/Interrupt Register (port 7).

Bit 3 - Phase Match - The SCSI signals, -MSG, -C/D, and -I/O, represent the current information transfer phase. The Phase Match bit indicates whether the current SCSI Bus phase matches the lower three bits of the Target Command Register. Phase Match is continuously updated and is only significant when operating as a bus initiator. A phase match is required for data transfers to occur on the SCSI Bus.

Bit 2 - Busy Error - The Busy Error bit is active if an unexpected loss of the -BSY signal has occurred. This latch is set whenever the Monitor Busy bit (port 2, bit 2) is true and -BSY is false. An unexpected loss of -BSY will disable any SCSI outputs and will reset the DMA Mode bit (port 2, bit 1).

Bit 1 - ATN - This bit reflects the condition of the SCSI Bus control signal -ATN. This signal is normally monitored by the Target device.

Bit 0 - ACK - This bit reflects the condition of the SCSI Bus control signal -ACK. This signal is normally monitored by the Target device.

DMA REGISTERS

Three write only registers are used to initiate all DMA activity. They are Start DMA Send (port 5), Start DMA Target Receive (port 6) and Start DMA Initiator Receive (port 7). Simply writing these registers starts the DMA transfers. Data presented to the VL53C80 on signals D0 through D7 during the register write is meaningless and has no effect on the operation. Prior to writing these registers, the Block Mode DMA bit (bit 7), the DMA Mode bit (bit 1) and the Target Mode Bit (bit 6) in the Mode Register (port 2) must be appropriately set. The individual registers are briefly described as follows.

Start DMA Send

Address 5 (Write Only) - This register is written to initiate a DMA send, from the DMA to the SCSI Bus, for either initiator or target role operations. The DMA Mode bit (port 2, bit 1) must be set prior to writing this register.

Start DMA Target Receive

Address 6 (Write Only) - This register is written to initiate a DMA receive, from the SCSI Bus to the DMA, for Target operation only. The DMA Mode bit (bit 1) and the Target Mode bit (bit 6) in the Mode Register (port 2) must both be set (1) prior to writing this register.

Start DMA Initiator Receive

Address 7 (Write Only) - This register is written to initiate a DMA receive, from the SCSI Bus to the DMA, for initiator operation only. The DMA Mode bit (bit 6) must be false (0) in the Mode Register (port 2) prior to writing this register.

Reset Parity/Interrupt

Address 7 (Read Only) - Reading this register resets the Parity Error bit (bit 5), the Interrupt Request bit (bit 4), and the Busy Error bit (bit 2) in the Bus and Status Register (port 5).

ON-CHIP SCSI HARDWARE SUPPORT

The device allows direct control and monitoring of the SCSI Bus by providing a latch for each signal. Portions of the protocol define timings which are much too quick for traditional microprocessors to control. Therefore, hardware support has been provided for DMA transfers, bus arbitration, phase change monitoring, bus disconnection, bus reset, parity generation, parity checking, and device selection/reselection.

Arbitration is performed using a bus free filter to continuously inspect -BSY. If -BSY stays inactive for at least 400 ns, then the SCSI Bus is free, and arbitration may begin. Arbitration starts if the bus is free, -SEL is inactive, and the Arbitration bit (port 2, bit 0) is active. Once arbitration has started (-BSY asserted), an arbitration delay of 2.2 μ s should elapse before the Data Bus can be examined to determine if arbitration has been won. This delay is implemented in the control software driver.

The VL53C80 is a clockwise device. Delays such as bus free delay, bus set delay, and bus-settle delay are implemented using gate delays. These delays may differ between devices because of inherent process variations, but are well within the proposed ANSI X3T9.2 specification (Revision 17).

INTERRUPTS

The VL53C80 provides an interrupt output (IRQ) to display a task completion or an unusual bus event. The use of interrupts is optional. They may be disabled by resetting the assigned bits in the Mode Register (port 2) or the Select Enable Register (port 4).

When an interrupt occurs, the Bus and Status Register and the Current SCSI Bus Status Register should be read to determine which condition caused the interrupt. IRQ can be reset simply by reading the Reset Parity/Interrupt Register (port 7) or by an external chip reset (-RESET active for 200 ns).

When the VL53C80 has been correctly initialized, an interrupt will be generated if the chip is selected or reselected, if an -EOP signal occurs during a DMA transfer, if an SCSI Bus reset occurs, if a parity error occurs during a data transfer, if a bus phase mismatch occurs, or if an SCSI Bus disconnection takes place.

Selection/Reselection

The VL53C80 can generate a select interrupt if -SEL is true (1), its device ID is true (1), and -BSY is false for at least one bus-settle delay (400 ns). If -I/O is active, this should be considered a reselect interrupt. The correct ID bit is determined by a match in the Select Enable Register (port 4). Only a single bit match is necessary to generate an interrupt. This interrupt may be disabled by writing zeros (0's) into all bits of the Select Enable Register.

If parity is supported, parity should also be good during the selection phase. Therefore, if the Enable Parity bit (port 2, bit 5) is active then the Parity Error bit should be checked to ensure that a proper selection has occurred. The Enable Parity Interrupt bit need not be set for this interrupt to be generated.

The proposed SCSI specification also requires that no more than two device IDs be active during the selection processor. To ensure this, the Current SCSI Data Register (port 0) should be read.

Values for the Bus and Status Register (port 5) and the Current SCSI Bus Status Register (port 4) are displayed below, respectively.

7	6	5	4	3	2	1	0
0	0	0	1	X	0	X	0
END OF DMA	DMA RQST	PAR ERR	INT RQST ACT	Ø MCH	BSY ERR	-ATN	-ACK

7	6	5	4	3	2	1	0
0	0	0	X	X	X	1	X
-RST	-BSY	-REQ	-MSG	-C/D	-I/O	-SEL	-DBP

End of Process (EOP) Interrupt

An End of Process signal (-EOP) which occurs during a DMA transfer (DMA Mode true) will set the End Of DMA Status bit (port 5, bit 7) and may generate an interrupt if Enable EOP Interrupt bit (port 2, bit 3) is true. The -EOP pulse will not be recognized (End of DMA bit set) unless -EOP, -DACK, and either -I/O or -LOW are simultaneously active for at least 100 ns. DMA transfers can still occur if -EOP was asserted at the correct time. This interrupt can be disabled by resetting the Enable EOP Interrupt bit.

Values for the Bus and Status Register (port 5) and the Current SCSI Bus Status Register (port 4) for this interrupt are shown below, respectively.

7	6	5	4	3	2	1	0
1	0	0	1	0	0	0	X
END OF DMA	DMA RQST	PAR ERR	INT RQST ACT	Ø MCH	BSY ERR	-ATN	-ACK

7	6	5	4	3	2	1	0
0	1	X	X	X	X	0	X
-RST	-BSY	-REQ	-MSG	-C/D	-I/O	-SEL	-DBP

The End Of DMA bit is used to determine when a block transfer is complete. Receive operations are complete when there is no data left in the chip and no additional handshakes occurring. The only exception to this is receiving data as an Initiator and the Target opts to send additional data for the same phase. In this case, -REQ goes active

and the new data appears in the Input Data Register. Since a phase mismatch interrupt will not occur, -REQ and -ACK must be sampled to determine that the Target is attempting to send more data.

For send operations, the End Of DMA bit is set when the DMA completes its transfer, but the SCSI transfer may still be in progress. If connected as a Target, -REQ and -ACK should be sampled until both are false. If connected as an Initiator, a phase change interrupt can be used to signal the completion of the previous phase. It is possible for the Target to request more data for the same phase. Then, a phase change will not occur and both -REQ and -ACK must be sampled to determine when the last byte was transferred.

SCSI Bus Reset

The VL53C80 generates an interrupt when the -RST signal changes to true. The device releases all bus signals within a bus clear delay (800 ns) of this transition. This interrupt also occurs after setting the Assert -RST bit (port 1, bit 7). This interrupt cannot be disabled. (Note: -RST is not latched in bit 7 of the Current SCSI Bus Status Register and may not be active when this port is read. For this case, the Bus Reset interrupt may be determined by default.)

Values for the Bus and Status Register (port 5) and the Current SCSI Bus Status Register (port 4) are displayed below, respectively.

7	6	5	4	3	2	1	0
0	X	0	1	X	0	X	X
END OF DMA	DMA RQST	PAR ERR	INT RQST ACT	Ø MCH	BSY ERR	-ATN	-ACK

7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X
-RST	-BSY	-REQ	-MSG	-C/D	-I/O	-SEL	-DBP

Parity Error

An interrupt is generated for a received parity error if the Enable Parity Check (bit 5) and the Enable Parity Interrupt (bit 4) bits are set (1) in the Mode Register (port 2). Parity is checked while reading the Current SCSI Data Register (port 0) and during a DMA receive operation. A parity error can be

detected without generating an interrupt by disabling the Enable Parity Interrupt bit and checking the Parity Error flag (port 5, bit 5).

Values for the Bus and Status Register (port 5) and the Current SCSI Bus Status Register (port 4) are displayed below, respectively.

7	6	5	4	3	2	1	0
0	X	1	1	1	0	X	X
END OF DMA	DMA RQST	PAR ERR	INT RQST ACT	Ø MCH	BSY ERR	-ATN	-ACK

7	6	5	4	3	2	1	0
0	1	1	X	X	X	0	X
-RST	-BSY	-REQ	-MSG	-C/D	-I/O	-SEL	-DBP

Bus Phase Mismatch

The SCSI phase lines contain the signals -I/O, -C/D, and -MSG. These signals are compared with the corresponding bits in the Target Command Register: Assert -I/O (bit 0), Assert -C/D (bit 1), and Assert -MSG (bit 2). The comparison continually occurs, and is reflected in the Phase Match bit (bit 3) of the Bus and Status Register (port 5). An interrupt (IRQ) is generated if the DMA Mode bit (port 2, bit 1) is active and a phase mismatch occurs when -REQ transitions from false to true.

A phase mismatch prevents the recognition of -REQ and also removes the chip from the bus during an Initiator send operation. -DB0 through -DB7, and -DBP will not be driven even though the Assert Data Bus bit (port 1, bit 0) is active. This interrupt is only active when connected as an Initiator and may be disabled by resetting the DMA Mode bit. (Note: It is possible for this interrupt to occur when connected as a Target if another device is driving the phase lines to a different state.)

Values for the Bus and Status Register (port 5) and the Current SCSI Bus Status Register (port 4) are displayed below, respectively.

7	6	5	4	3	2	1	0
0	0	0	1	0	0	X	0
END OF DMA	DMA RQST	PAR ERR	INT RQST ACT	Ø MCH	BSY ERR	-ATN	-ACK

7	6	5	4	3	2	1	0
0	1	X	X	X	X	0	X
-RST	-BSY	-REQ	-MSG	-C/D	-I/O	-SEL	-DBP

Loss of -BSY

When the Monitor Busy bit (bit 2) in the Mode Register (port 2) is active, an interrupt will be generated if the -BSY signal goes false for at least one bus-settle delay (400 ns). This interrupt may be disabled by resetting the Monitor Busy bit. Values are displayed below for the Bus and Status Register and Current SCSI Bus Status Register, respectively.

7	6	5	4	3	2	1	0
0	0	0	1	X	1	0	0
END OF DMA	DMA RQST	PAR ERR	INT RQST ACT	Ø MCH	BSY ERR	-ATN	-ACK

7	6	5	4	3	2	1	0
0	0	0	X	X	X	0	0
-RST	-BSY	-REQ	-MSG	-C/D	-I/O	-SEL	-DBP

RESET CONDITIONS

There are three reset situations that apply to the VL53C80:

Hardware Chip Reset

When the signal -RST is active for at least 200 ns, the VL53C80 device is re-initialized and all internal logic and control registers are cleared. This is only a chip reset, and does not cause and SCSI Bus reset condition.

SCSI Bus Reset (-RST) Received

When an SCSI -RST signal is detected, an IRQ interrupt is generated and a chip reset occurs. All internal logic and registers are cleared, except for the IRQ interrupt latch and the Assert -RST bit (bit 7) in the Initiator Command Register (port 1). (Note: The -RST signal may be sampled by reading the Current SCSI Bus Status Register (port 4). This signal is not latched and may not be present when this port is read.)

SCSI Bus Reset (-RST) Issued

If the MPU sets the Assert -RST bit (bit 7) in the Initiator Command Register (port 1), the -RST signal goes active on the SCSI Bus and an internal reset occurs. All internal logic and registers are cleared except for the IRQ interrupt latch and the Assert -RST bit (bit 7) in the Initiator Command Register (port 1). The -RST signal continues to be active until the Assert -RST bit is reset or until a hardware reset occurs.

DATA TRANSFERS

Data may be transferred between SCSI Bus devices in one of four modes:

- 1) Programmed I/O
- 2) Normal DMA
- 3) Block Mode DMA
- 4) Pseudo DMA.

The following sections describe these modes in detail. (Note: For all data transfer operations -DACK and -CS can never be active at the same time).

Programmed I/O Transfers

Programmed I/O is the most basic form of data transfer. The -REQ and -ACK handshake signals are individually examined and asserted by reading and writing the appropriate register bits. This type of transfer is usually used when transferring small blocks of data (e.g. command blocks or message and status bytes).

An initiator send operation will begin by setting the -C/D, -I/O, and -MSG bits in the Target Command Register to the correct state so that a phase match exists. In addition to the phase match condition, it is necessary for the Assert Data Bus bit (port 1, bit 0) to be true and the received I/O signal to be false for the VL53C80 to send data.

For every transfer, the data is loaded to the Output Data Register (port 0). The MPU then waits for the -REQ bit (port 4, bit 5) to become active. Once -REQ goes active, the Phase Match bit (port 5, bit 3) is checked and the Assert -ACK bit (port 1, bit 4) is set. The -REQ bit is sampled until it becomes false and the MPU resets the Assert -ACK bit to complete the transfer.

Normal DMA Mode

DMA transfers are usually used for large block transfers. The SCSI chip outputs a DMA request (DRQ) whenever it is ready for a byte transfer. External DMA logic uses this DRQ signal to generate -DACK and an -IOR or an -IOW pulse to the VL53C80. DRQ becomes inactive when -DACK is asserted and -DACK goes inactive some time after the minimum read or write pulse width. This process is repeated for every byte. In this mode, -DACK should not be allowed to cycle unless a transfer is occurring.

Block Mode DMA

Popular DMA controllers such as the 9517A provide a Block Mode DMA transfer. This type of transfer allows the DMA controller to transfer blocks of data without giving up the use of the Data Bus to the MPU after each byte is transferred. This way, faster transfer rates are achieved by eliminating the repetitive access and release of the MPU Bus.

If the Block Mode DMA bit (port 2, bit 7) is active, the VL53C80 begins the transfer by asserting DRQ. The DMA controller then asserts -DACK for the duration of the block transfer. DRQ becomes inactive for the remainder of the transfer. The READY output can be used to control the transfer rate.

Non-block mode DMA transfers terminate when -DACK goes false, whereas Block Mode transfers end when -IOR or -IOW becomes inactive. DMA transfers may be started sooner in a Block Mode transfer.

To obtain the best performance in Block Mode operation, the DMA logic should use the normal DMA mode interlocking handshake. READY is available to throttle the DMA transfer, but DRQ is 30 to 40 ns faster than READY, and may be used to start the cycle sooner.

The methods described under "Halting a DMA Operation" apply for all DMA operations.

Pseudo DMA Mode

In order to avoid monitoring and asserting the request/acknowledge handshake signals for programmed I/O transfers, the system may be designed to implement a pseudo DMA mode. This mode initiated by programming the VL53C80 to operating in the DMA mode, by using the MPU to emulate the DMA handshake. DRQ may be detected by polling the DMA Request bit (bit 6) in the Bus and Status Register (port 5), by sampling the signal through an external port or by using it to cause a MPU interrupt. Once DRQ is detected, the MPU can perform a read or write data transfer. This MPU read/write is externally decoded to generate the correct -DACK and -IOR or -IOW signals.



Frequently, external decoding logic is needed to generate the VL53C80 $\overline{\text{CS}}$ signal. This same logic may be used to generate $\overline{\text{DACK}}$ at no extra system cost and provide an increased performance in programmed I/O transfers.

Halting a DMA Operation

The $\overline{\text{EOP}}$ signal is one way to halt a DMA transfer. A bus phase mismatch or a reset of the DMA Mode bit (port 2, bit 1) can also end a DMA cycle for the current bus phase.

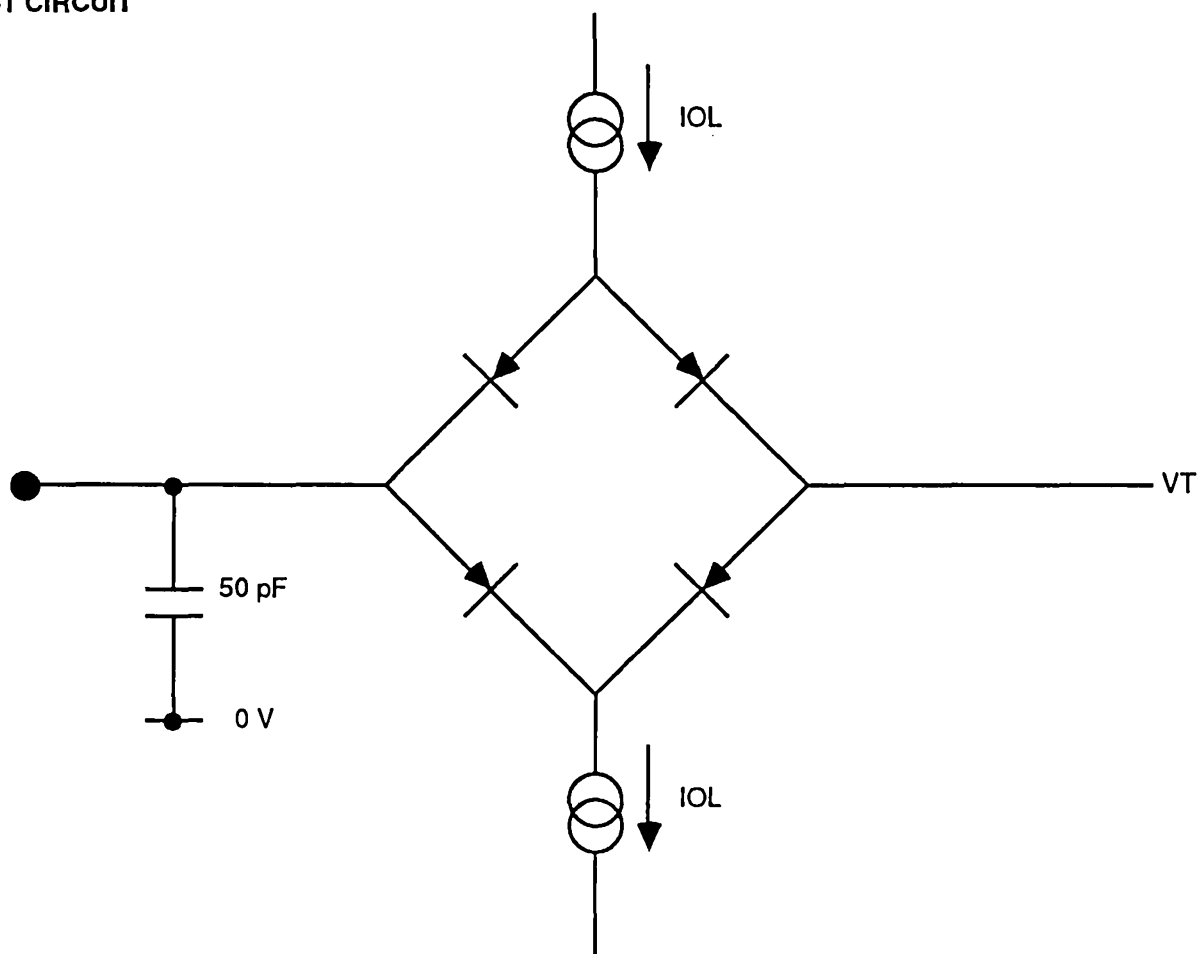
Using the $\overline{\text{EOP}}$ Signal - If $\overline{\text{EOP}}$ is used, it should be asserted for at least 100 ns while $\overline{\text{DACK}}$ and $\overline{\text{IOR}}$ or $\overline{\text{IOW}}$ are both active. If either $\overline{\text{IOR}}$ or $\overline{\text{IOW}}$ are not active, an interrupt will be generated, but the DMA activity will continue. The $\overline{\text{EOP}}$ signal does not reset the DMA Mode bit. The $\overline{\text{EOP}}$ signal can occur during the last byte sent to the Output Data Register (port 0). The $\overline{\text{REQ}}$ and $\overline{\text{ACK}}$ signals should be monitored to ensure that the last byte has transferred.

Bus Phase Mismatch Interrupt - A bus phase mismatch interrupt may be used to halt the transfer if operating as an Initiator. Using this method frees the host from maintaining a data length counter and frees the DMA logic from providing the $\overline{\text{EOP}}$ signal. If performing an Initiator send operation, the VL53C80 requires $\overline{\text{DACK}}$ to cycle before $\overline{\text{ACK}}$ goes inactive. Since phase changes cannot occur if $\overline{\text{ACK}}$ is active, either $\overline{\text{DACK}}$ must be cycled after the last byte is sent or the DMA Mode bit must be reset in order to receive the phase mismatch interrupt.

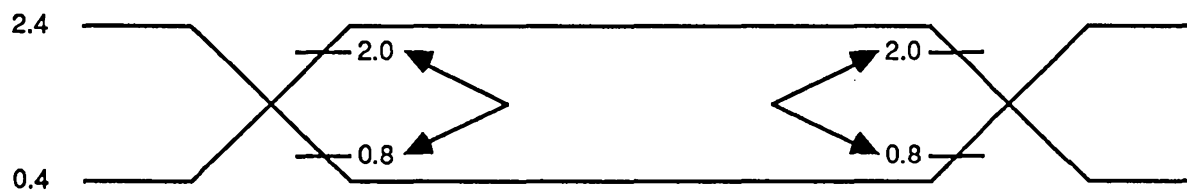
Resetting the DMA Mode Bit - A DMA operation may be stopped at any time simply by resetting the DMA Mode bit. It is recommended that the DMA Mode bit be reset after receiving an $\overline{\text{EOP}}$ or bus phase mismatch interrupt. The DMA Mode bit must then be set before writing any of the start DMA register for later bus phases.

If resetting the DMA Mode bit is used instead of $\overline{\text{EOP}}$ for Target role operation, then care must be exercised to reset this bit at the proper time. When receiving data as a Target device, the DMA Mode bit must be reset once the last DRQ is received and before $\overline{\text{DACK}}$ is asserted to prevent an additional $\overline{\text{REQ}}$ from taking place. Resetting this bit causes DRQ to go inactive. The last byte received remains in the Input Data Register and may be obtained either by performing a normal MPU read or by cycling $\overline{\text{DACK}}$ or $\overline{\text{IOR}}$. Frequently, $\overline{\text{EOP}}$ is easier to use when operating as a Target device.

SWITCHING TEST CIRCUIT

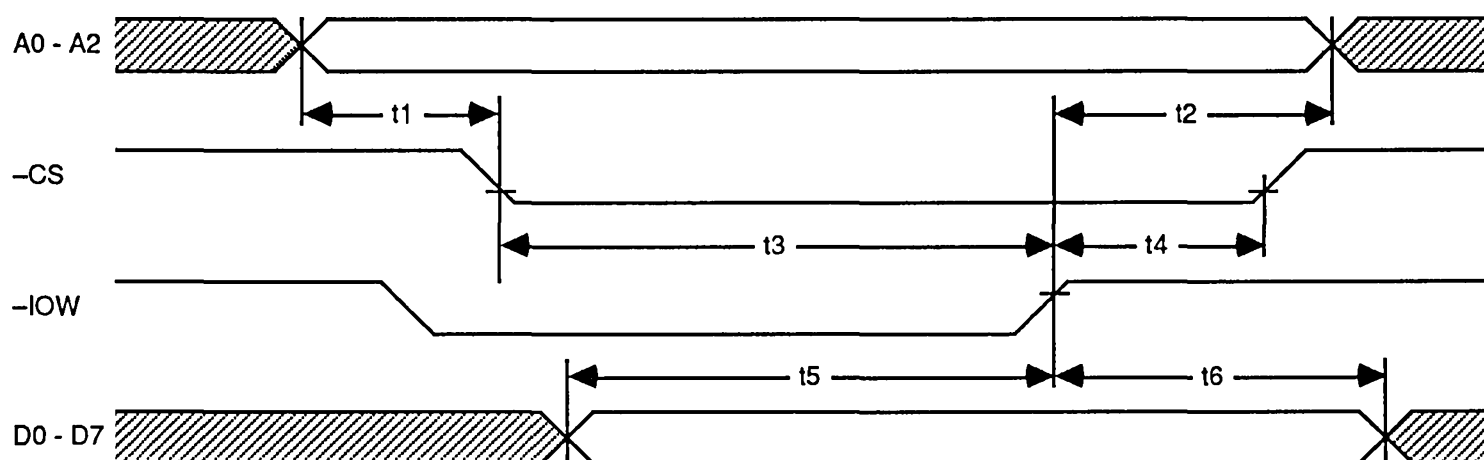


SWITCHING TEST WAVEFORM

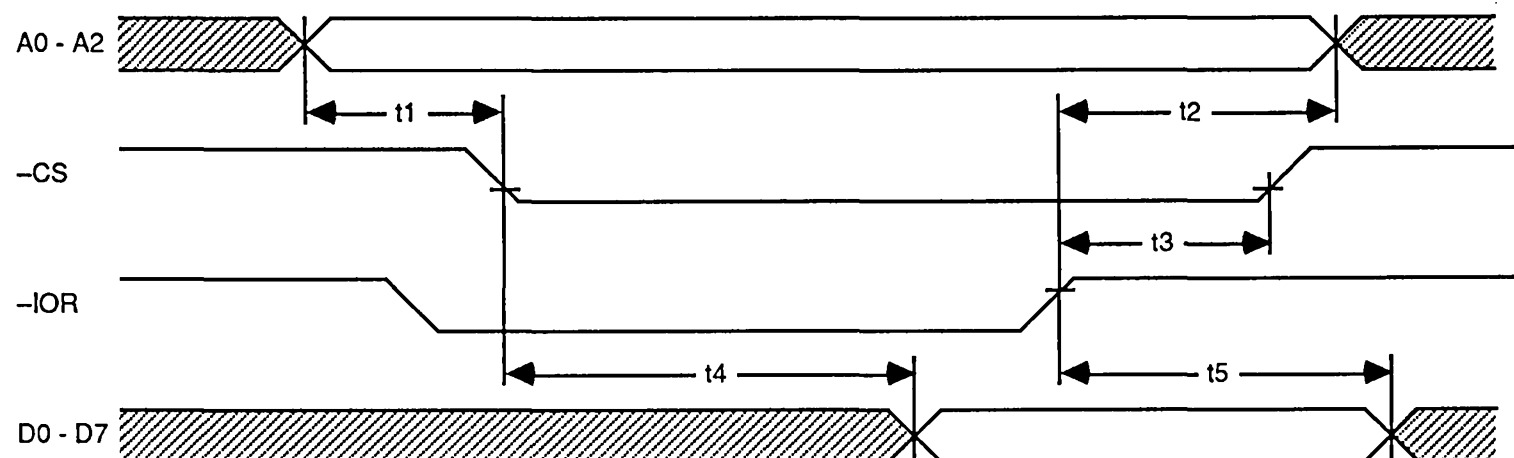


SWITCHING CHARACTERISTICS/WAVEFORMS
CPU WRITE

Symbol	Description	Min	Max	Units	Condition
t1	Address Setup to Write Enable	20		ns	Write Enable Occurs When --IOW and --CS
t2	Address Hold from End Write Enable	20		ns	Write Enable Occurs When --IOW and --CS
t3	Write Enable Width	70		ns	Write Enable Occurs When --IOW and --CS
t4	Chip Select Hold from End of --IOW	0		ns	
t5	Data Setup to End of Write Enable	50		ns	Write Enable Occurs When --IOW and --CS
t6	Data Hold Time from End of --IOW	30		ns	


CPU READ

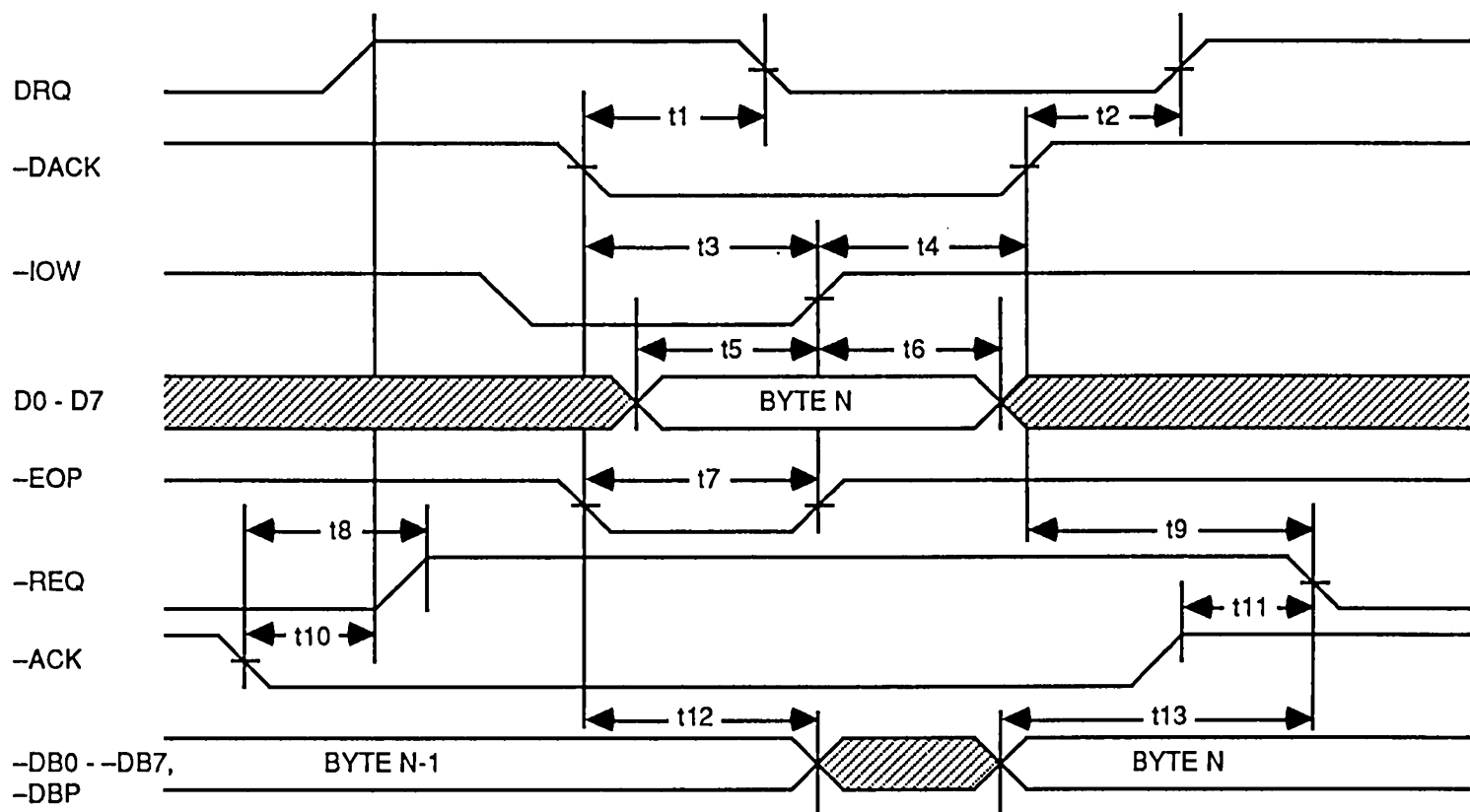
Symbol	Description	Min	Max	Units	Condition
t1	Address Setup to Read Enable	20		ns	Read Enable Occurs When --IOR and --CS
t2	Address Hold from End Read Enable	20		ns	Read Enable Occurs When --IOR and --CS
t3	Chip Select Hold from End of --IOR	0		ns	
t4	Data Access Time from Read Enable		130	ns	Read Enable Occurs When --IOR and --CS
t5	Data Hold Time from End of --IOR	20		ns	



SWITCHING CHARACTERISTICS/WAVEFORMS (Cont.)
DMA WRITE (NON-BLOCK MODE) TARGET SEND

Symbol	Description	Min	Max	Units	Condition
t1	DRQ False from $\overline{\text{DACK}}$ True		130	ns	
t2	$\overline{\text{DACK}}$ False to DRQ True	30		ns	
t3	Write Enable Width	100		ns	Write Enable Occurs When $\overline{\text{IOW}}$ and $\overline{\text{DACK}}$
t4	DACK Hold from End of $\overline{\text{IOW}}$	0		ns	
t5	Data Setup to End of Write Enable	50		ns	Write Enable Occurs When $\overline{\text{IOW}}$ and $\overline{\text{DACK}}$
t6	Data Hold Time from End of $\overline{\text{IOW}}$	40		ns	
t7	Width of $\overline{\text{EOP}}$ Pulse (Note)	100		ns	
t8	$\overline{\text{ACK}}$ True to $\overline{\text{REQ}}$ False	25	125	ns	
t9	$\overline{\text{REQ}}$ from End of $\overline{\text{DACK}}$ ($\overline{\text{ACK}}$ False)	30	150	ns	
t10	$\overline{\text{ACK}}$ True to DRQ True (Target)	15	110	ns	
t11	$\overline{\text{REQ}}$ from End of $\overline{\text{ACK}}$ ($\overline{\text{DACK}}$ False)	20	150	ns	
t12	Data Hold from Write Enable	15		ns	
t13	Data Setup to $\overline{\text{REQ}}$ True (Target)	60		ns	

Note: $\overline{\text{EOP}}$, $\overline{\text{IOW}}$, and $\overline{\text{DACK}}$ must be concurrently true for at least t7 for proper recognition of the $\overline{\text{EOP}}$ pulse.

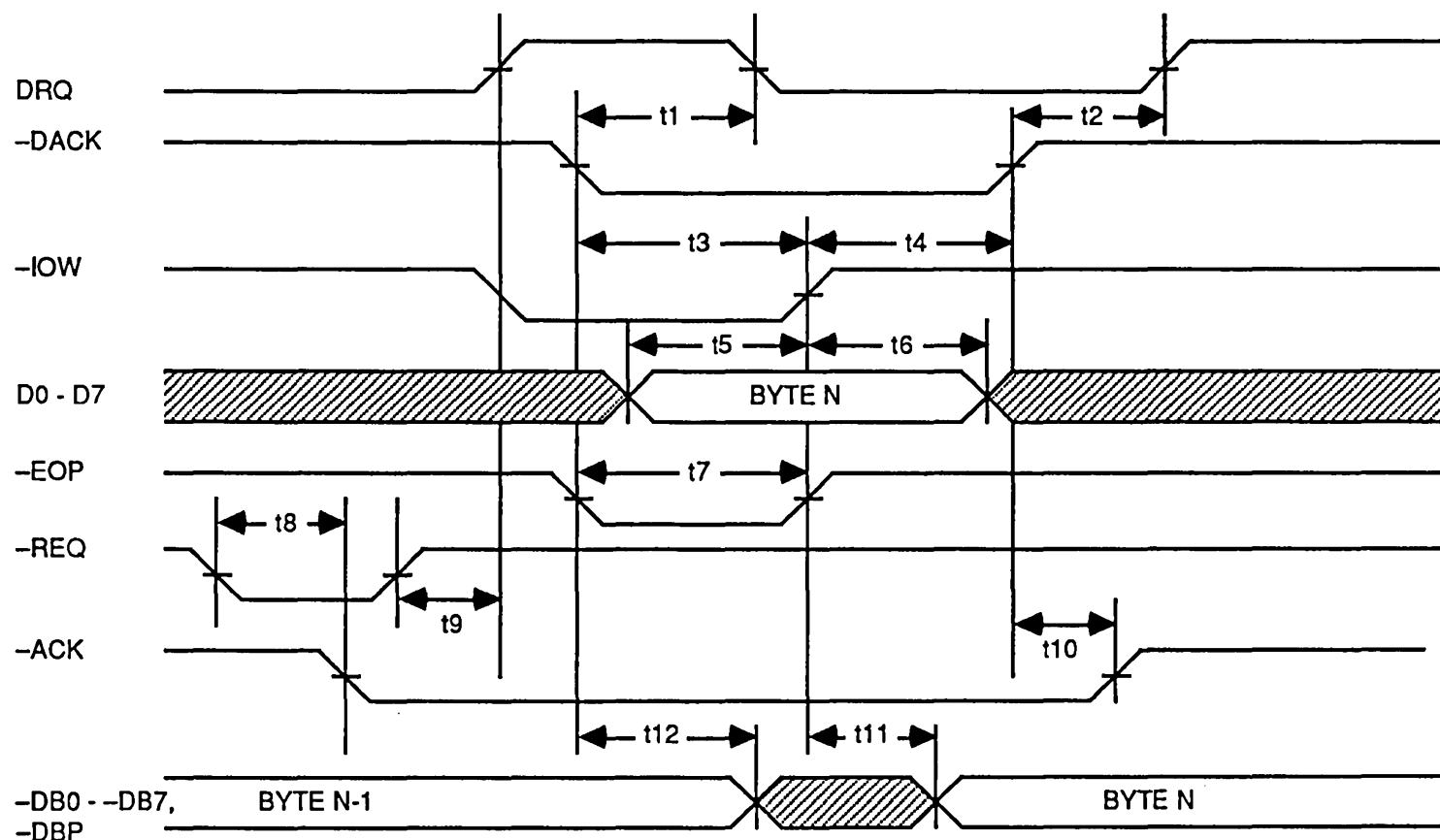


SWITCHING CHARACTERISTICS/WAVEFORMS(Cont.)

DMA WRITE (NON-BLOCK MODE) INITIATOR SEND

Symbol	Description	Min	Max	Units	Condition
t1	DRQ False from -DACK True		130	ns	
t2	-DACK False to DRQ True	30		ns	
t3	Write Enable Width	100		ns	Write Enable Occurs When -IOW and -DACK
t4	-DACK Hold from End of -IOW	0		ns	
t5	Data Setup to End of Write Enable	50		ns	Write Enable Occurs When -IOW and -DACK
t6	Data Hold Time from End of -IOW	40		ns	
t7	Width of -EOP Pulse (Note)	100		ns	
t8	-REQ True to -ACK True	20	160	ns	
t9	-REQ False to DRQ True	20	110	ns	
t10	-DACK False to -ACK False	25	150	ns	
t11	-IOW False to Valid SCSI Data		100	ns	
t12	Data Hold from Write Enable	15		ns	

Note: -EOP, -IOW, and -DACK must be concurrently true for at least t7 for proper recognition of the -EOP pulse.



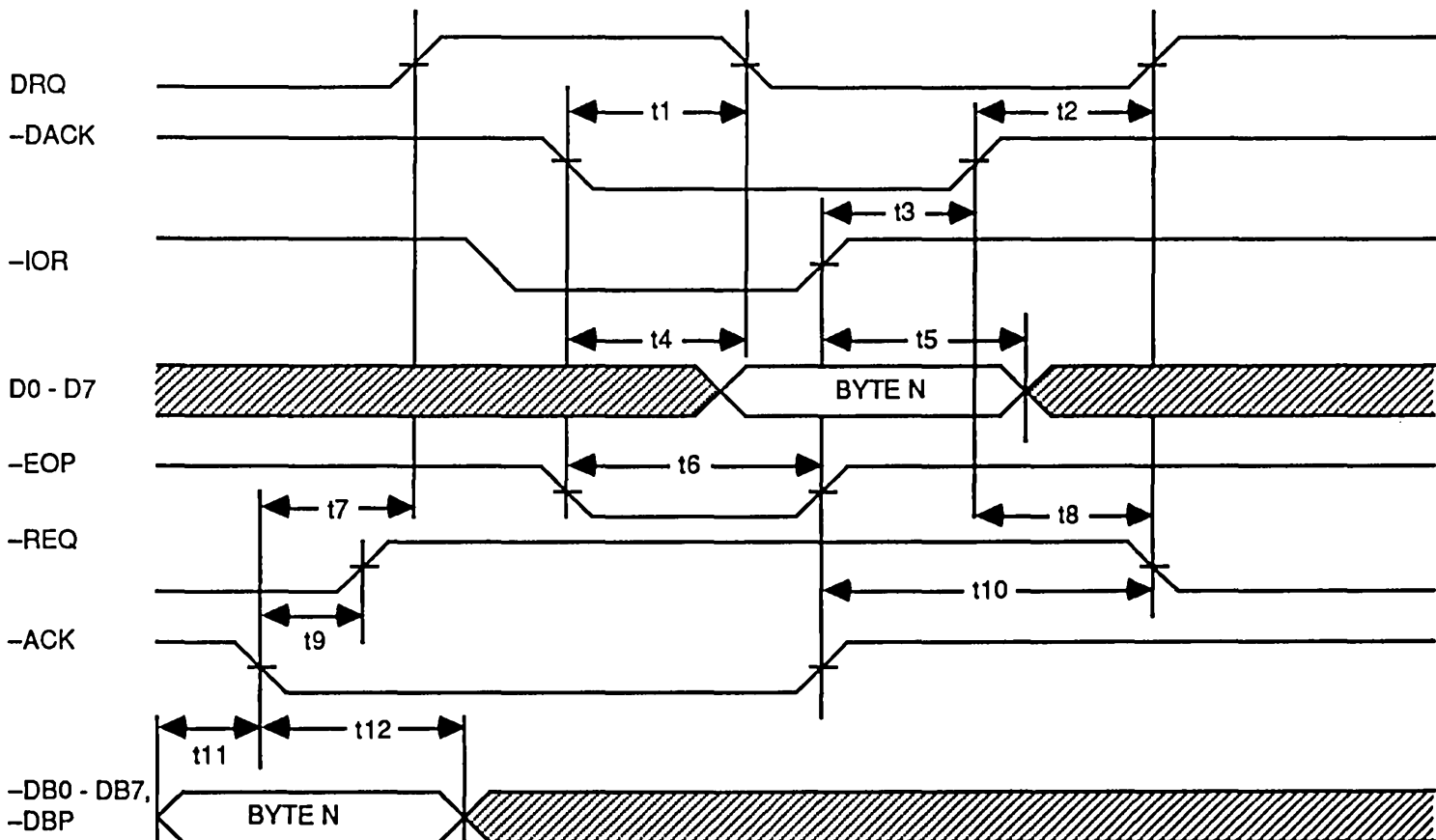


SWITCHING CHARACTERISTICS/WAVEFORMS (Cont.)

DMA READ (NON-BLOCK MODE) TARGET RECEIVE

Symbol	Description	Min	Max	Units	Condition
t1	DRQ False from -DACK True		130	ns	
t2	-DACK False to DRQ True	30		ns	
t3	-DACK Hold Time from End of -IOR	0		ns	
t4	Data Access Time from Read Enable		115	ns	Read Enable Occurs When -IOR and -DACK
t5	Data Hold Time from End of -IOR	20		ns	
t6	Width of -EOP Pulse (Note)	100		ns	
t7	-ACK True to DRQ True	15	110	ns	
t8	-DACK False to -REQ True (-ACK False)	30	150	ns	
t9	-ACK True to -REQ False	25	125	ns	
t10	-ACK False to -REQ True (-DACK False)	20	150	ns	
t11	Data Setup Time to -ACK	20		ns	
t12	Data Hold Time from -ACK	50		ns	

Note: -EOP, -IOR, and -DACK must be concurrently true for at least t6 for proper recognition of the -EOP pulse.

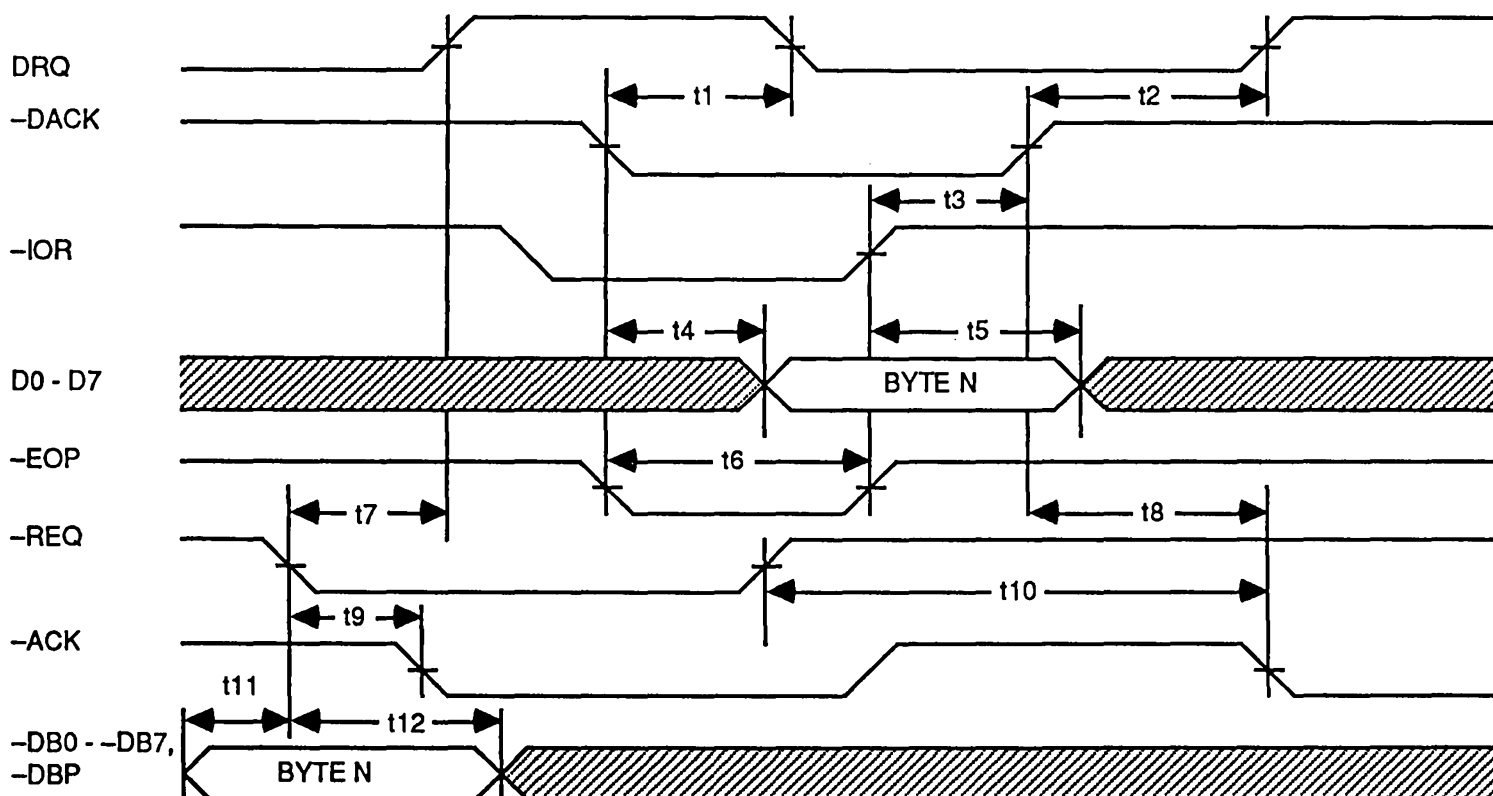


SWITCHING CHARACTERISTICS/WAVEFORMS (Cont.)

DMA READ (NON-BLOCK MODE) INITIATOR RECEIVE

Symbol	Description	Min	Max	Units	Condition
t1	DRQ False from -DACK True		130	ns	
t2	-DACK False to DRQ True	30		ns	
t3	-DACK Hold Time from End of -IOR	0		ns	
t4	Data Access Time from Read Enable		115	ns	Read Enable Occurs When -IOR and -DACK
t5	Data Hold Time from End of -IOR	20		ns	
t6	Width of -EOP Pulse (Note)	100		ns	
t7	-REQ True to DRQ True	20	150	ns	
t8	-DACK False to -ACK False (-REQ False)	25	160	ns	
t9	-REQ True to -ACK True	20	160	ns	
t10	-REQ False to -ACK False (-DACK False)	15	140	ns	
t11	Data Setup Time to -REQ	20		ns	
t12	Data Hold Time from -REQ	50		ns	

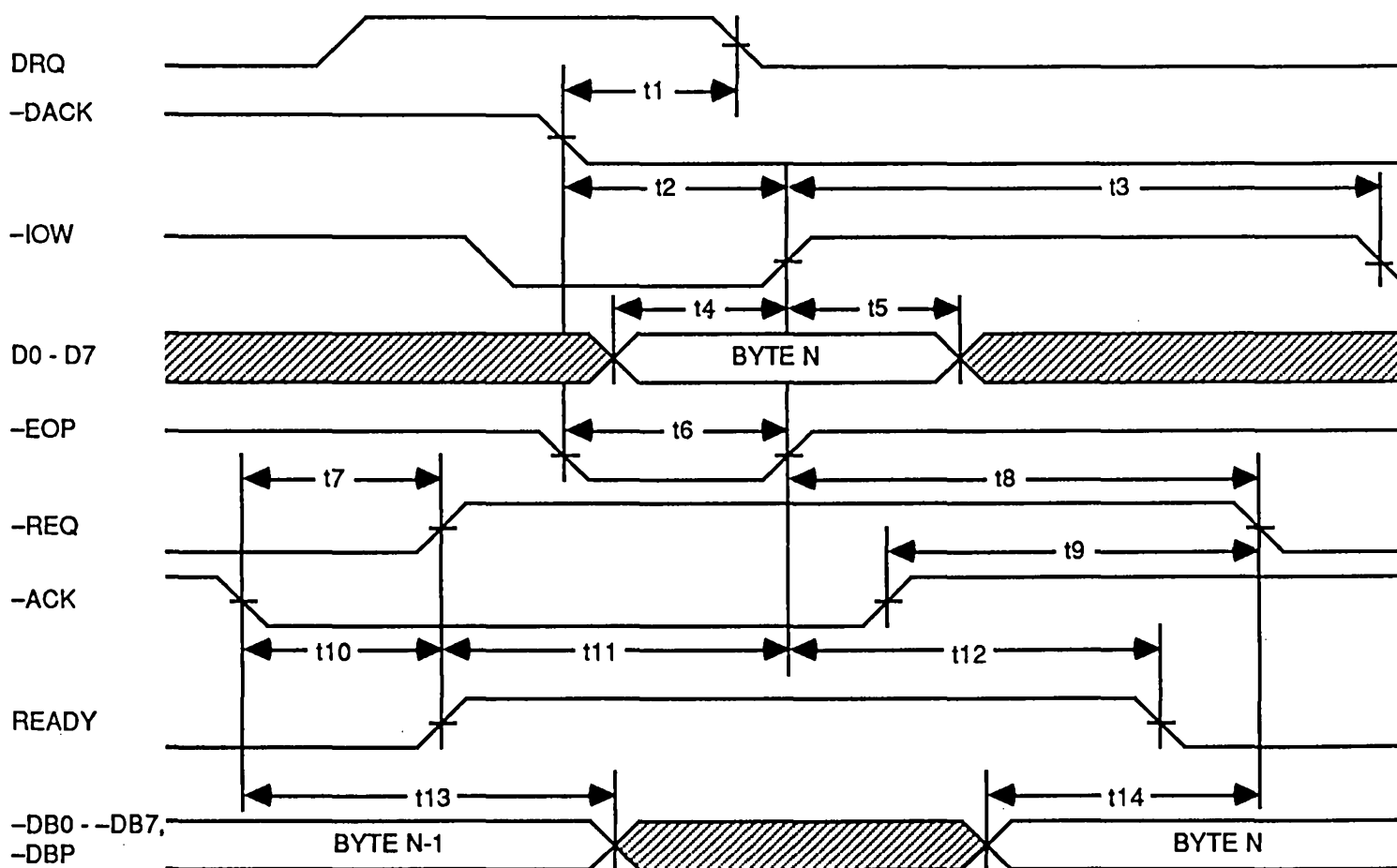
Note: -EOP, -IOR, and -DACK must be concurrently true for at least t6 for proper recognition of the -EOP pulse.



SWITCHING CHARACTERISTICS/WAVEFORMS (Cont.)
DMA WRITE (BLOCK MODE) TARGET SEND

Symbol	Description	Min	Max	Units	Condition
t1	DRQ False from \neg DACK True		130	ns	
t2	Write Enable Width	100		ns	Write Enable Occurs When \neg IOW and \neg DACK
t3	Write Recovery Time	120		ns	
t4	Data Setup to End of Write Enable	50		ns	Write Enable Occurs When \neg IOW and \neg DACK
t5	Data Hold Time from End of \neg IOW	40		ns	
t6	Width of \neg EOP Pulse (Note)	100		ns	
t7	\neg ACK True to \neg REQ False	25	125	ns	
t8	\neg REQ from End of \neg ACK (\neg ACK False)	40	180	ns	
t9	\neg REQ from End of \neg ACK (\neg IOW False)	20	170	ns	
t10	\neg ACK True to READY True	20	140	ns	
t11	READY True to \neg IOW False	70		ns	
t12	\neg IOW False to READY False	20	140	ns	
t13	Data Hold from \neg ACK True	40		ns	
t14	Data Setup to \neg REQ True	60		ns	

Note: \neg EOP, \neg IOW, and \neg DACK must be concurrently true for at least t6 for proper recognition of the \neg EOP pulse.

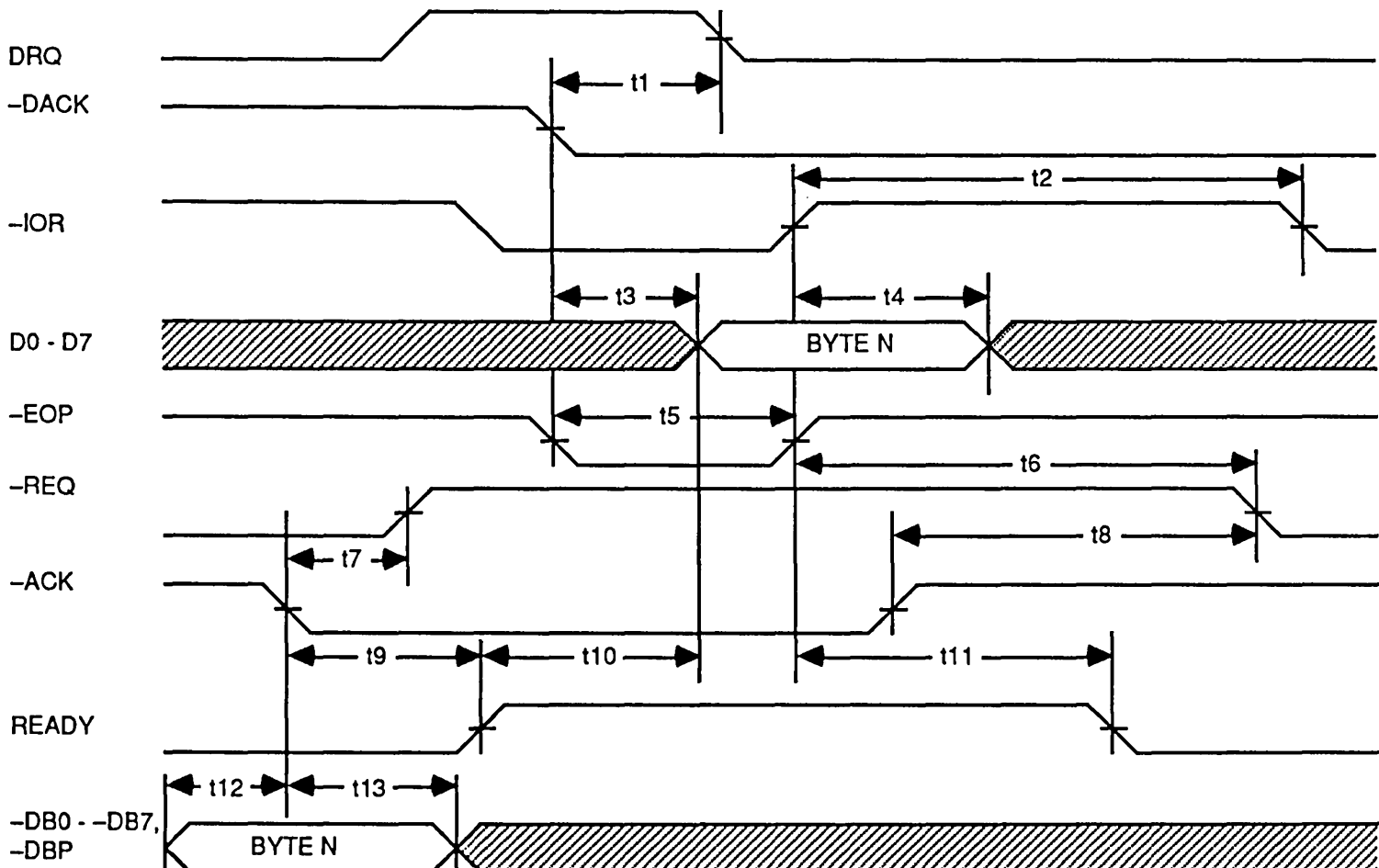


SWITCHING CHARACTERISTICS/WAVEFORMS(Cont.)

DMA READ (BLOCK MODE) TARGET RECEIVE

Symbol	Description	Min	Max	Units	Condition
t1	DRQ False from $\overline{\text{DACK}}$ True		130	ns	
t2	$\overline{\text{IOR}}$ Recovery Time	120		ns	
t3	Data Access Time from Read Enable		110	ns	Read Enable Occurs When $\overline{\text{IOR}}$ and $\overline{\text{DACK}}$
t4	Data Hold Time from End of $\overline{\text{IOR}}$	20		ns	
t5	Width of $\overline{\text{EOP}}$ Pulse (Note)	100		ns	
t6	$\overline{\text{IOR}}$ False to $\overline{\text{REQ}}$ True ($\overline{\text{ACK}}$ False)	30	190	ns	
t7	$\overline{\text{ACK}}$ True to $\overline{\text{REQ}}$ False	20	125	ns	
t8	$\overline{\text{ACK}}$ False to $\overline{\text{REQ}}$ True ($\overline{\text{IOR}}$ False)	20	170	ns	
t9	$\overline{\text{ACK}}$ True to READY True	20	140	ns	
t10	READY true to Valid Data		50	ns	
t11	$\overline{\text{IOR}}$ False to READY False	20	140	ns	
t12	Data Setup Time to $\overline{\text{ACK}}$	20		ns	
t13	Data Hold Time from $\overline{\text{ACK}}$	50		ns	

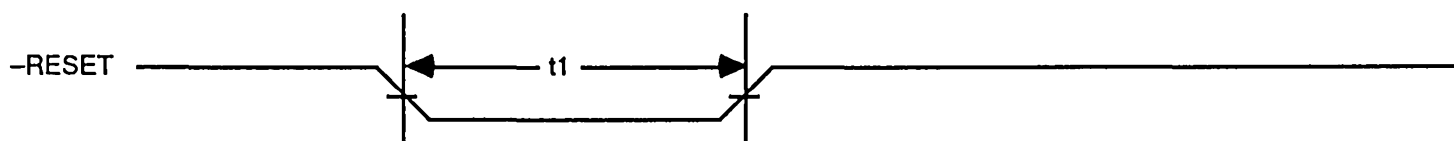
Note: $\overline{\text{EOP}}$, $\overline{\text{IOR}}$, and $\overline{\text{DACK}}$ must be concurrently true for at least t5 for proper recognition of the $\overline{\text{EOP}}$ pulse.



SWITCHING CHARACTERISTICS/WAVEFORMS (Cont.)

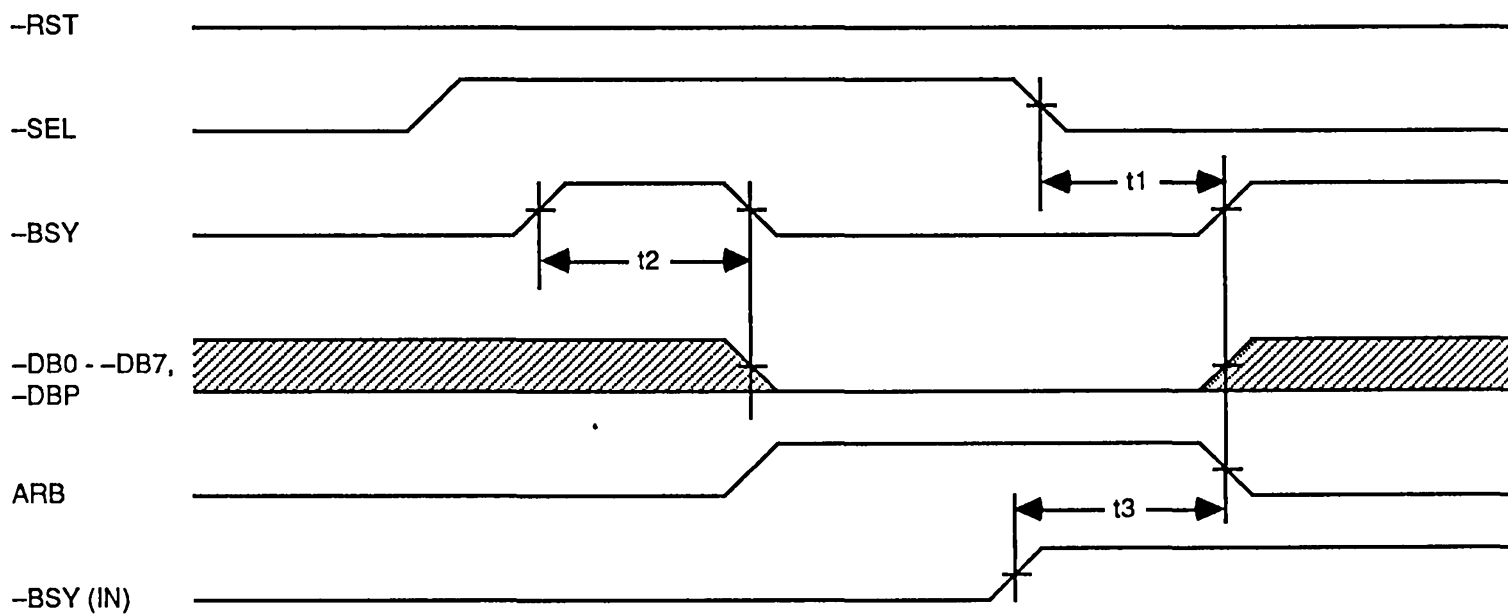
RESET

Symbol	Description	Min	Max	Units	Condition
t1	Minimum Width of Reset	200		ns	



ARBITRATION

Symbol	Description	Min	Max	Units	Condition
t1	Bus Clear from -SEL True		600	ns	
t2	Arbitrate Start from -BSY False	1200	2200	ns	
t3	Bus Clear from -BSY False		1100	ns	



**ABSOLUTE MAXIMUM RATINGS**

Ambient Operating Temperature 0°C to $+70^{\circ}\text{C}$
 Storage Temperature -65°C to $+150^{\circ}\text{C}$
 Supply Voltage to Ground Potential $+6\text{ V}$
 Applied Input Voltage -0.6 V to $\text{VCC} + 0.6\text{ V}$
 Power Dissipation 0.8 W

Stresses above those listed may cause permanent damage to the device. These are stress ratings only, functional operation of this device at these or any other conditions above those indicated

in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS: $T_A = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$, $\text{VCC} = 5\text{ V} \pm 5\%$

Symbol	Parameter	Min	Max	Units	Condition
V_{IH}	High Level Input Voltage	2.0	5.25	V	
V_{IL}	Low Level Input Voltage	-0.3	0.8	V	
I_{IH}	High Level Input Current on:				$V_{IH} = 5.25\text{ V}$, $V_{IL} = 0$
	SCSI Bus Pins		50	μA	
	All Other Pins		10	μA	
I_{IL}	Low Level Input Current on:				$V_{IH} = 5.25\text{ V}$, $V_{IL} = 0$
	SCSI Bus Pins		-50	μA	
	All Other Pins		-10	μA	
V_{OH}	High Level Output Voltage	2.4		V	$V_{DD} = 4.75\text{ V}$, $I_{OH} = -3.0\text{ mA}$
V_{OL}	Low Level Output Voltage on:				
	SCSI Bus Pins		0.5	V	$V_{DD} = 4.75\text{ V}$, $I_{OL} = 48.0\text{ mA}$
	All Other Pins		0.5	V	$V_{DD} = 4.75\text{ V}$, $I_{OL} = 7.0\text{ mA}$

CMOS 8-BIT MICROPROCESSOR
FEATURES

- CMOS silicon-gate technology
- Low power
 - 1.1 mA/MHz
- Software compatible with the NMOS 6502
- Single 5 V power supply required
- 8-bit parallel processing
- True indexing capability
- Programmable stack pointer
- Interrupt capability
- Non-maskable interrupt
- 8-bit bidirectional data bus
- Addressable memory range of up to 64K bytes
- Ready input
- Direct memory access (DMA) capability
- Clock speeds up to 4 MHz
- Pipelined architecture
- On-chip clock options:
 - External single-input clock
 - On-board clock, single external crystal

DESCRIPTION

The VL65NC02 is an 8-bit microprocessor device produced using CMOS silicon-gate technology. This device provides advanced system architecture for enhancements in system performance, speed, and value over its NMOS counterparts, the 65XX family of microprocessor devices. The VL65NC02 is the CMOS equivalent of the NMOS 6502, and contains some enhancements. This CMOS type may exhibit different intermediate cycle information from that resident in the NMOS 6502. Intermediate cycle information is not specified, and should not be used.

The VL65NC02 provides 64K bytes of addressable memory and an interrupt input, as well as options for on-chip oscillators and drivers. It is bus and software compatible with the 65XX CPU family.

CLOCK GENERATOR

The clock generator develops all internal clock signals and (where applicable) external clock signals associated with the device. It is the clock generator that drives the timing control unit and the external timing for slave mode operations.

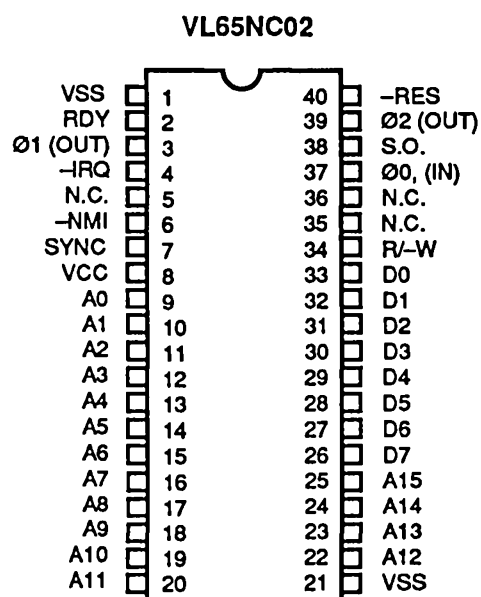
TIMING CONTROL

The timing control unit keeps track of the instruction cycle being monitored. The unit is set to zero each time an instruction fetch is executed and is advanced at the beginning of each phase-one clock pulse for as many cycles as are required to complete the instruction. Each data transfer that takes place between the registers depends upon decoding the contents of both the instruction register and the timing control unit.

PROGRAM COUNTER

The 16-bit program counter provides the addresses that step the microprocessor through sequential instructions in a program.

Each time the microprocessor fetches an instruction from program memory, the lower byte of the program counter (PCL) is placed on the low-order bits of the address bus and the higher byte of the program counter (PCH) is placed on the high-order 8 bits. The counter is incremented each time an instruction or data is fetched from program memory.

PIN DIAGRAM

ORDER INFORMATION

Part Number	Clock Frequency	Package
VL65NC02-01PC	1 MHz	Plastic DIP
VL65NC02-01CC		Ceramic DIP
VL65NC02-02PC	2 MHz	Plastic DIP
VL65NC02-02CC		Ceramic DIP
VL65NC02-03PC	3 MHz	Plastic DIP
VL65NC02-03CC		Ceramic DIP
VL65NC02-04PC	4 MHz	Plastic DIP
VL65NC02-04CC		Ceramic DIP

Note: Operating temperature range is 0°C to +70°C.



BLOCK DIAGRAM

INTERNAL ARCHITECTURE

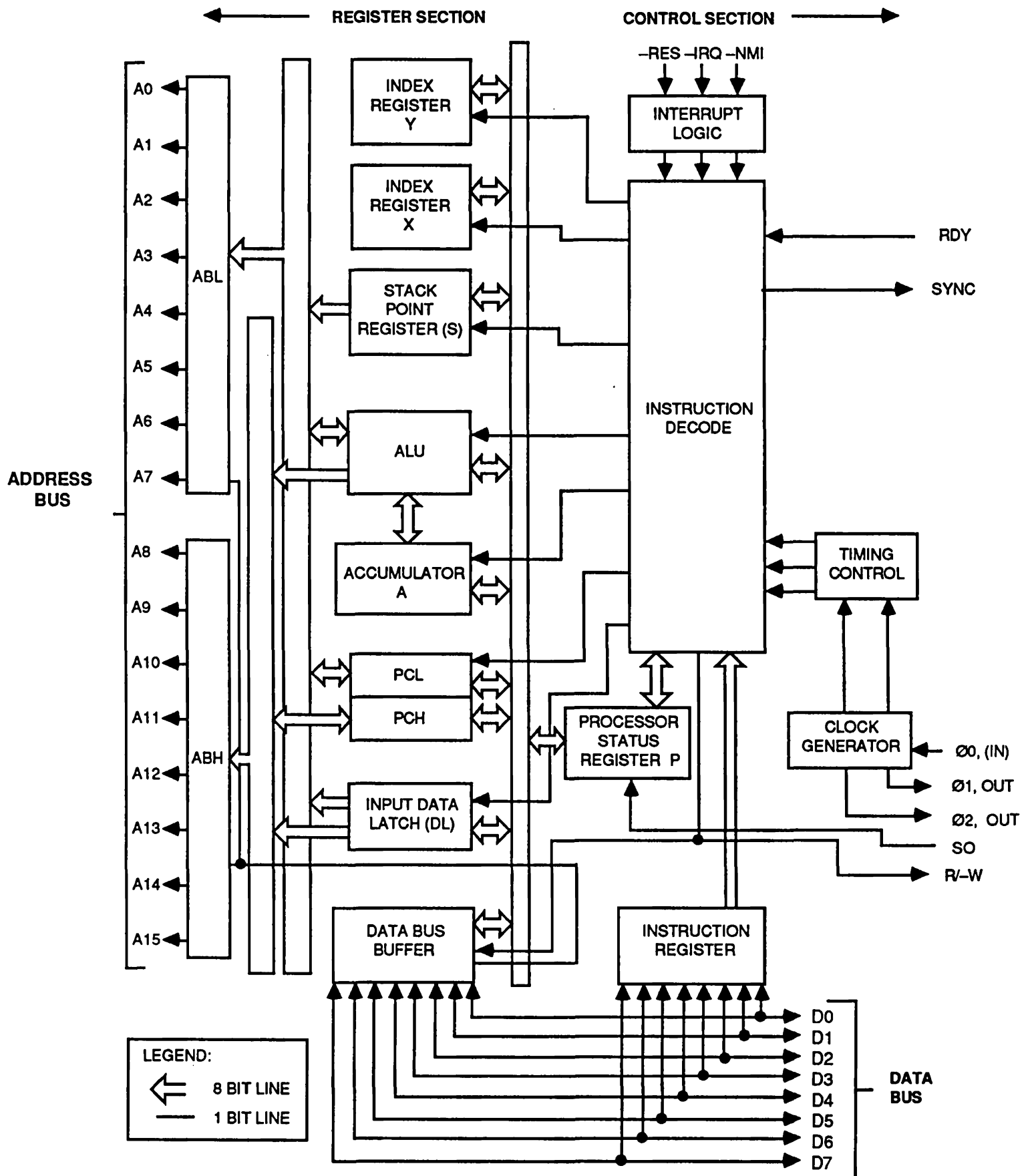


TABLE 1. HARDWARE ENHANCEMENTS

The VL65NC02 microprocessor has been designed with several hardware and software enhancements over the NMOS 6502 device, while maintaining software compatibility. In addition to the increased speed and lower power consumption inherent in CMOS technology, the VL65NC02 has the following characteristics:

- Two new addressing modes
- Seven software/operational enhancements
- Two hardware enhancements:
 - Eight new instructions, 64 total
 - 27 new opcodes, 178 total

VL65NC02 Enhancements

Pin compatible with NMOS 6502
64K addressable bytes of memory
–IRQ interrupt
TTL-level single phase clock input
RC time base clock input
Crystal time base clock input
Two-phase output clock
SYNC and RDY signals
–NMI interrupt signal

SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Description
Ø0 (IN), Ø1 (OUT), Ø2 (OUT)	37, 3, 39	Clock Signals - The VL65NC02 requires an external Ø0 clock. Ø0 is a TTL-level input that is used to generate the internal clocks of the VL65NC02. Two full-level output clocks are generated by the VL65NC02. The Ø2 clock is in phase with Ø0. The Ø1 clock output is 180° out of phase with Ø0. When Ø0 is stopped, the CPU is in the standby mode.
–IRQ	4	Interrupt Request - This TTL-compatible input requests that an interrupt sequence begin within the microprocessor. The –IRQ is sampled during Ø2 operation; if the interrupt flag in the processor status register is zero, the current instruction is completed and the interrupt sequence begins during Ø1. The program counter and processor status register are stored in the stack. The microprocessor then sets the interrupt mask flag high so that no further –IRQs may occur. At the end of this cycle, the program counter low byte is loaded from address FFFE, and program counter high byte from location FFFF, thus transferring program control to the memory vector located at these addresses. The RDY signal must be in the high state for any interrupt to be recognized. A 3 kΩ external resistor should be used for proper wire-OR operation.
–NMI	6	Non-Maskable Interrupt - A negative-going edge on this input requests that a non-maskable interrupt sequence be generated within the microprocessor. The –NMI is sampled during Ø2; the current instruction is completed and the interrupt sequence begins during Ø1. The program counter is loaded with the interrupt vector from locations FFFA (low byte) and FFFB (high byte), thereby transferring program control to the non-maskable interrupt routine. Since this interrupt is non-maskable, another –NMI can occur before the first is finished. Care should be taken when using –NMI to avoid this.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Description
RDY	2	Ready - This input allows the user to single-cycle the microprocessor on all cycles, including write cycles. A negative transition to the low state, during or coincident with ϕ_1 , halts the microprocessor with the output address lines reflecting the current address being fetched. This condition remains through a subsequent ϕ_2 in which the ready signal is low. This feature allows microprocessor interfacing with low-speed memory as well as direct memory access (DMA).
R/-W	34	Read/Write - This signal is normally in the high state, indicating that the microprocessor is reading data from memory or I/O bus. In the low state, the data bus has valid data from the microprocessor to be stored at the addressed memory location.
-SO	38	Set Overflow - A negative transition on this line sets the overflow bit (V) in the processor status register. The signal is sampled prior to the leading edge of ϕ_2 by the processor control time (tRWS).
-RES	40	Reset - This input resets the microprocessor. Reset must be held low for at least two clock cycles after VCC reaches operating voltage from a power-down. A positive transition on this pin causes an initialization sequence to begin. Likewise, after the system has been operating, a low on this line of at least two cycles ceases microprocessing activity, followed by initialization after the positive edge on -RES. When a positive edge is detected, there is an initialization sequence lasting six clock cycles. Then, the interrupt mask flag is set, the decimal mode is cleared, and the program counter is loaded with the restart vector from locations FFFC (low byte) and FFFD (high byte). This is the start location for program control. This input should be high in normal operation.
SYNC	7	Synchronize - This output line identifies those cycles during which the microprocessor is fetching the instruction operation code (op code). The SYNC line goes high during ϕ_1 of an opcode fetch and stays high for the remainder of that cycle. If the RDY line is pulled low during the ϕ_1 clock pulse in which SYNC went high, the processor stops in its current state and remains in the state until the RDY line goes high. In this manner, the SYNC signal can be used to control RDY to cause single instruction execution.
A0 - A15	9 - 25	Address Bus - A0-A15 forms a 16-bit address bus for memory and I/O exchanges on the data bus. The output of each address line is TTL-compatible, capable of driving one standard TTL load and 130 pF.
D0 - D7	33 - 26	Data Bus - The data lines constitute an 8-bit bidirectional data bus used for data exchanges to and from the device and peripherals. The outputs are three-state buffers capable of driving one TTL load and 130 pF.
VCC	8	5 V \pm 5% power supply
VSS	1,21	Digital ground

INSTRUCTION AND REGISTER DECODE

Instructions fetched from memory are gated onto the internal data bus. These instructions are latched into the instruction register, then decoded, along with timing and interrupt signals, to generate control signals for the various registers.

ARITHMETIC/LOGIC UNIT

All arithmetic and logic operations take place in the ALU, including incrementing and decrementing internal registers (except the program counter). The ALU has no internal memory and is used only to perform logical and transient numerical operations.

ACCUMULATOR

The accumulator is a general-purpose 8-bit register that stores the results of most arithmetic and logic operations. In addition, the accumulator usually contains one of the two data words used in these operations.

INDEX REGISTER

There are two 8-bit index registers (X and Y) that may be used to count program steps or to provide an index value to be used in generating an effective address.

When executing an instruction that specifies indexed addressing, the CPU fetches the op code and the base address, and modifies the address by adding the index register to it prior to performing the desired operation. Pre- or post-indexing of indirect addresses is possible (see addressing modes).

STACK POINTER

The stack pointer is an 8-bit register used to control the addressing of the variable-length stack on page one. The stack pointer is automatically incremented and decremented under control of the microprocessor to perform stack manipulations under direction of either the program or interrupts (–NMI and –IRQ). The stack allows simple implementation of nested sub-routines and multiple-level interrupts. The stack pointer should be initialized before any interrupts or stack operations occur.

PROCESSOR STATUS REGISTER

The 8-bit processor status register contains seven status flags. Some of the flags are controlled by the program, others may be controlled by the program and the CPU. The VL65NC02 instruc-

tion set contains a number of conditional branch instructions that are designed to allow testing of these flags.

HARDWARE ENHANCEMENTS

The VL65NC02 microprocessor incorporates several hardware enhancements over its NMOS counterpart, the 6502. These hardware enhancements are:

- The NMOS device would ignore the assertion of a Ready (RDY) during a write operation. The CMOS family stops the processor during Ø2 clock if RDY is asserted during a write operation.
- On the NMOS device, unused input-only pins (–IRQ, –NMI, RDY, –RES, and –SO) must be connected to a low impedance signal to avoid noise problems. These unused pins on the CMOS devices are internally connected by a high-impedance to VCC (approximately 250 kΩ).

OPERATIONAL ENHANCEMENTS

Tables 1 lists the operational enhancements that have been added to the VL65NC02 device.

TABLE 2. NO OPERATION (NOP) TIMING FOR UNDEFINED OPCODES

Opcode	Number of Bytes Expected (Total- Including Opcode):	Number of Cycles:
X2	2	2
X3	1	1
X7	1	1
XB	1	1
XF	1	1
44	2	3
54	2	4
D4	2	4
F4	2	4
5C	3	8
DC	3	4
FC	3	4

Note: "X" indicates a "Don't Care".

TABLE 3. INSTRUCTION SET SUMMARY

		IMME- DIATE		ABSO- LUTE		ZERO PAGE		(4) IMPLIED		(1) (IND. X)		(1) (IND. Y)		ZPG.X		(1) ABS.X		(1) ABS.Y		RELA- TIVE (2)		INDI- RECT		ZPG.Y		PROCESSOR STATUS CODE							
MNE- MONIC	OPERATION	OP	n #	OP	n #	OP	n #	OP	n #	OP	n #	OP	n #	OP	n #	OP	n #	OP	n #	OP	n #	OP	n #	OP	n #	7	6	4	3	2	1	0	MNE- MONIC
ADC	A + M + C - A (3)	69	2 2	6D	4 3	65	3 2			61	6 2	71	5 2	75	4 2	7D	4 3	79	4 3			72	5 2			N	V	Z	ADC
AND	A \wedge M - A	29	2 2	2D	4 3	25	3 2			21	6 2	31	5 2	35	4 2	3D	4 3	39	4 3			32	5 2			N	Z	AND	
ASL	C - [7] 0 - 0			0E	6 3	06	5 2	0A	2 1					16	6 2	1E	6 3									N	Z	ASL	
BCC	BRANCH IF C=0 (2)																			90	2 2					BCC
BCS	BRANCH IF C=1 (2)																			B0	2 2					BCS
BEQ	BRANCH IF Z=1 (2)																			F0	2 2					BEQ
BIT	A \wedge M (5)	89	2 2	2C	4 3	24	3 2							34	4 2	3C	4 3									M	Z	BIT	
BMI	BRANCH IF N=1 (2)																			30	2 2					BMI
BNE	BRANCH IF Z=0 (2)																			D0	2 2					BNE
BPL	BRANCH IF N=0 (2)																			10	2 2					BPL
BRA	BRANCH ALWAYS(2)																			80	2 2					BRA
BRK	BREAK							00	7 1																	.	.	1	0	1	.	.	BRK
BVC	BRANCH IF V=0 (2)																			50	2 2					BVC
BVS	BRANCH IF V=1 (2)																			70	2 2					BVS
CLC	0 - C							18	2 1																	0	CLC
CLD	0 - D							D8	2 1																	0	.	CLD
CLI	0 - I							58	2 1																	0	.	.	CLI
CLV	0 - V							B8	2 1																	.	0	CLV
CMP	A-M	C9	2 2	CD	4 3	C5	3 2			C1	6 2	D1	5 2	D5	4 2	DD	4 3	D9	4 3			D2	5 2			N	Z	CMP	
CPX	X-M	E0	2 2	EC	4 3	E4	3 2																			N	Z	CPX	
CPY	Y-M	C0	2 2	CC	4 3	C4	3 2																			N	Z	CPY	
DEC	DECREMENT			CE	6 3	C6	5 2	3A	2 1					D6	6 2	DE	6 3									N	Z	DEC	
DEX	X-1 - X							CA	2 1																		N	Z	DEX
DEY	Y-1 - Y							88	2 1																		N	Z	DEY
EOR	A \vee M - A	49	2 2	4D	4 3	45	3 2			41	6 2	51	5 2	55	4 2	5D	4 3	59	4 3			52	5 2			N	Z	EOR	
INC	INCREMENT			EE	6 3	E6	5 2	1A	2 1					F6	6 2	FE	6 3									N	Z	INC	
INX	X + 1 - X							E8	2 1																	N	Z	INX	
INY	Y + 1 - Y							C8	2 1																	N	Z	INY	
JMP	JUMP TO NEW LOC			4C	3 3					7C	6 3											6C	6 3			JMP
JSR	JUMP SUB			20	6 3																					JSR
LDA	M - A	A9	2 2	AD	4 3	A5	3 2			A1	6 2	B1	5 2	B5	4 2	BD	4 3	B9	4 3			B2	5 2			N	Z	LDA	
LDX	M - X	A2	2 2	AE	4 3	A6	3 2											BE	4 3					B6	4 2	N	Z	LDX	
LDY	M - Y	A0	2 2	AC	4 3	A4	3 2							B4	4 2	BC	4 3									N	Z	LDY	
LSR	0 - [7] 0 - C			4E	6 3	46	5 2	4A	2 1					56	6 2	5E	6 3									0	Z	LSR	
NOP	NO OPERATION							EA	2 1																	NOP
ORA	AVM - A	09	2 2	0D	4 3	05	3 2			01	6 2	11	5 2	15	4 2	1D	4 3	19	4 3			12	5 2			N	Z	ORA	
PHA	A - Ms S-1-S							48	3 1																	PHA
PHP	P - Ms S-1-S							08	3 1																	PHP
PHX	X - Ms S-1-S							DA	3 1																	PHX
PHY	Y - Ms S-1-S							5A	3 1																	PHY
PLA	S+1-S Ms-A							68	4 1																	N	Z	PLA	
PLP	S+1-S Ms-P							28	4 1																	N	V	1	D	I	Z	PLP	
PLX	S+1-S Ms-X							FA	4 1																	N	Z	PLX	
PLY	S+1-S Ms-Y							7A	4 1																	N	Z	PLY	
ROL	[7] 0 - C			2E	6 3	26	5 2	2A	2 1					36	6 2	3E	6 3									N	Z	ROL	
ROR	C - [7] 0			6E	6 3	66	5 2	6A	2 1					76	6 2	7E	6 3									N	Z	ROR	
RTI	RTRN INT							40	6 1																	N	V	1	D	I	Z	RTI	
RTS	RTRN SUB							60	6 1																	RTS
SBC	A-M-C-A (3)	E9	2 2	ED	4 3	E5	3 2			E1	6 2	F1	5 2	F5	4 2	FD	4 3	F9	4 3			F2	5 2			N	V	.	.	Z	SBC		
SEC	1 - C							38	2 1																	1	.	.	SEC
SED	1 - D							F8	2 1																	.	.	.	1	.	.	.	SED
SEI	1 - I							78	2 1																	1	.	.	SEI
STA	A - M			8D	4 3	85	3 2			81	6 2	91	6 2	95	4 2	9D	5 3	99	5 3			92	5 2			STA	
STP	STOP (1 - ϕ 2)							DB	3 1																	STP
STX	X - M			8E	4 3	86	3 2																			STX
STY	Y - M																																

TABLE 4. INSTRUCTION SET SUMMARY ABBREVIATIONS

X Index X	Λ And
Y Index Y	V Or
A Accumulator	⊕ Exclusive Or
M Memory per Effective Address	n Number of Cycles
Ms Memory per stack Pointer	# Number of Bytes
+ Add	M6 Memory Bit 6
- Subtract	M7 Memory Bit 7

Add 1 to "n" if decimal mode, if page boundary is crossed (except STA and STZ), or if branch on same page (add 2 if page different). Accumulator address is included in implied address. "N" and "V" flags are unchanged in immediate mode. "Z" flag includes A^M result (same as BIT instruction).

ADDRESSING MODES

The VL65NC02 CPU has 15 addressing modes (two more than the NMOS-equivalent family). In the following discussion of these addressing modes, a bracketed expression follows the title of the mode. This expression is the term used in the Instruction Set Opcode Matrix, Table 8, to make it easier to identify the actual addressing mode used by the instruction.

ACCUMULATOR ADDRESSING

[Accum]- This form of addressing is represented by a one-byte instruction, implying an operation on the accumulator.

IMMEDIATE ADDRESSING

[IMM] - In immediate addressing, the second byte of the instruction contains the operand, with no further memory addressing required.

ABSOLUTE ADDRESSING

[Absolute] - In absolute addressing, the second byte of the instruction specifies the eight low-order bits of the effective address, while the third byte specifies the eight high-order bits. Thus, the absolute addressing mode allows access to the entire 64K bytes of addressable memory.

ZERO PAGE ADDRESSING

[ZP] - The zero page instructions allow for shorter code and execution times by fetching only the second byte of the instruction and assuming a zero high address byte. Careful use of the zero-page can result in a significant increase in code efficiency.

INDEXED ZERO PAGED ADDRESSING

[ZP, X, or Y] - (X, Y Indexing) - This form of addressing is used with the index register and is referred to as "zero-page, X" or "zero-page, Y". The effective address is calculated by adding the second byte to the contents of the index register. Since this is a form of "zero-page" addressing, the content of

the second byte references a location in page zero. Additionally, due to the "zero-page" addressing nature of this mode, no carry is added to the high-order eight bits of memory and crossing of page boundaries does not occur.

INDEXED ABSOLUTE ADDRESSING

[ABS, X, or Y] - (X, Y Indexing) - This form of addressing is used in conjunction with X and Y index register and is referred to as "absolute, X" and "absolute, Y". The effective address is formed by adding the contents of X or Y to the address contained in the second and third bytes of the instruction. This mode allows the index register to contain the index or count value and the instruction to contain the base address. This type of indexing allows any location referencing and the index to modify multiple fields, resulting in reduced coding and execution time.

INDEXED ABSOLUTE INDIRECT

[(IND), X] - (JMP (IND), X) - The contents of the second and third instruction bytes are added to the X register. The 16-bit result is a memory address containing the effective address.

IMPLIED ADDRESSING

[Implied] - In the implied addressing mode, the address containing the operand is implicitly stated in the operation code of the instruction.

RELATIVE ADDRESSING

[Relative] - Relative addressing is used only with branch instructions and establishes a destination for the conditional branch.

The second byte of the instruction becomes the operand, which is an "offset" added to the contents of the lower eight bits of the program counter when the counter is set at the next instruction. The 8-bit offset provides a branching range of -128 to +127 bytes from the next instruction.

INDEXED INDIRECT ADDRESSING

[(IND, X)] - In indexed indirect addressing, referred to as indirect, X, the second byte of the instruction is added to the contents of the X index register, discarding the carry. The result of this addition points to a memory location on page zero whose contents are the low-order eight bits of the effective address. The next memory location in page zero contains the high-order eight bits of the effective address. Both memory locations specifying the high-and low-order bytes of the effective address must be in page zero.

INDIRECT INDEXED ADDRESSING

[(IND), Y] - In indirect indexed addressing, referred to as indirect, Y, the second byte of the instruction points to a memory location in page zero. The contents of this memory location are added to the contents of the Y index register, the result being the low-order eight bits of the effective address. The carry from this addition is added to the contents of the next page zero memory location, the result being the high-order eight bits of the effective address.

ABSOLUTE INDIRECT

[Indirect] - The second byte of the instruction contains the low-order eight bits of a memory location. The high-order eight bits of that memory location are contained in the third byte of the instruction. The contents of the fully specified memory location are the low-order byte of the effective address. The next memory location contains the high-order byte of the effective address, which is loaded into the 16 bits of the program counter, (JMP (IND) only).

INDIRECT

[(IND)] - The second byte of the instruction contains a zero page address serving as the indirect pointer. This is not available on the NMOS 6500 family.

INSTRUCTION SET

Table 5 lists the instruction set for the CMOS CPU family in alphabetic order according to mnemonic. Table 6 lists the hexadecimal codes for each of the instructions that are new to the CMOS family and were not available in the NMOS 6502 device family. Table 7 lists those instructions that were available on the NMOS family, but have been assigned new addressing modes in the CMOS CPU family.

TABLE 5. INSTRUCTION SET LISTING (ALPHABETIC)

Mnemonic	Function	Mnemonic	Function
(2) ADC	Add Memory to Accumulator with Carry	NOP	No Operation
(2) AND	"AND" Memory with Accumulator	(2) ORA	"OR" Memory with Accumulator
ASL	Shift Left One Bit (Memory or Accumulator)	PHA	Push Accumulator on Stack
(1)(3) BBR	Branch on Bit Reset	PHP	Push Processor Status on Stack
(1)(3) BBS	Branch on Bit Set	(1) PHX	Push X Register on Stack
BCC	Branch on Carry Clear	(1) PHY	Push Y Register on Stack
BCS	Branch on Carry Set	PLA	Pull Accumulator from Stack
BEQ	Branch on Result Zero	PLP	Pull Processor Status from Stack
(2) BIT	Test Bits in Memory with Accumulator	(1) PLX	Pull X Register from Stack
BMI	Branch on Result Minus	(1) PLY	Pull Y Register from Stack
BNE	Branch on Result not Zero	(1)(3) RMB	Reset Memory Bit
BPL	Branch on Result Plus	ROL	Rotate One Bit Left (Memory or Accumulator)
(1) BRA	Branch Always	ROR	Rotate One Bit Right (Memory or Accumulator)
BRK	Force Break	RTI	Return from Interrupt
BVC	Branch on Overflow Clear	RTS	Return from Subroutine
BVS	Branch on Overflow Set	(2) SBC	Subtract Memory from Accumulator with Borrow
CLC	Clear Carry Flag	SEC	Set Carry Flag
CLD	Clear Decimal Mode	SED	Set Decimal Mode
CLI	Clear Interrupt Disable Bit	SEI	Set Interrupt Disable Status
CLV	Clear Overflow Flag	(1)(3) SMB	Set Memory Bit
(2) CMP	Compare Memory and Accumulator	(2) STA	Store Accumulator in Memory
CPX	Compare Memory and Index X	STX	Store Index X in Memory
CPY	Compare Memory and Index Y	STY	Store Index Y in Memory
(2) DEC	Decrement Memory by One	(1) STZ	Store Zero
DEX	Decrement Index X by One	TAX	Transfer Accumulator to Index X
DEY	Decrement Index Y by One	TAY	Transfer Accumulator to Index Y
(2) EOR	"Exclusive-OR" Memory with Accumulator	(1) TRB	Test and Reset Bits
(2) INC	Increment Memory by One	(1) TSB	Test and Set Bits
INX	Increment Index X by One	TSX	Transfer Stack Pointer to Index X
INY	Increment Index Y by One	TXA	Transfer Index X to Accumulator
(2) JMP	Jump to New Location	TXS	Transfer Index X to Stack Register
JSR	Jump to New Location Saving Return Address	TYA	Transfer Index Y to Accumulator
(2) LDA	Load Accumulator with Memory		
LDX	Load Index X with Memory		
LDY	Load Index Y with Memory		
LSR	Shift One Bit Right (Memory or Accumulator)		

Notes:

1. CMOS instruction not available on NMOS Family.
2. Previous NMOS instruction with additional addressing mode(s) added to the CMOS family.
3. 65C02 instruction not available on VL65NC02.

TABLE 6. HEXADECIMAL CODES (NEW CMOS FAMILY INSTRUCTIONS)

Hex	Mnemonic	Description
80	BRA	Branch Relative Always (Relative)
3A	DEC	Decrement Accumulator (Accum)
1A	INC	Increment Accumulator (Accum)
DA	PHX	Push X on Stack (Implied)
5A	PHY	Push Y on Stack (Implied)
FA	PLX	Pull X from Stack (Implied)
7A	PLY	Pull Y from Stack (Implied)
9C	STZ	Store Zero (Absolute)
9E	STZ	Store Zero (ABS, X)
64	STZ	Store Zero (ZP)
74	STZ	Store Zero (ZP, X)
1C	TRB	Test and Reset Memory Bits with Accumulator (Absolute)
14	TRB	Test and Reset Memory Bits with Accumulator (ZP)
0C	TSB	Test and Set Memory Bits with Accumulator (Absolute)
04	TSB	Test and Set Memory Bits with Accumulator (ZP)
89	BIT	Test Immediate with Accumulator (IMM)
0F-7F(1)	BBR	Branch on Bit Reset (Bit Manipulation, ZP)
8F-FF(1)	BBS	Branch on Bit Set (Bit Manipulation, ZP)
07-77(1)	RMB	Reset Memory Bit (Bit Manipulation, ZP)
87-F7(1)	SMB	Set Memory Bit (Bit Manipulation, ZP)

Note:

1. Most significant digit change only. Instruction not available on 65C02.

**TABLE 7. HEXADECIMAL CODES
(INSTRUCTIONS WITH NEW CMOS ADDRESSING MODES)**

Hex	Mnemonic	Description
72	ADC	Add Memory to Accumulator with Carry [(ZP)]
32	AND	AND Memory with Accumulator [(ZP)]
3C	BIT	Test Memory Bits with Accumulator [ABS, X]
34	BIT	Test Memory Bits with Accumulator [ZP, X]
D2	CMP	Compare Memory and Accumulator [(ZP)]
52	EOR	Exclusive-OR Memory with Accumulator [(ZP)]
7C	JMP	Jump (New addressing mode) [(IND), X]
B2	LDA	Load Accumulator with Memory [(ZP)]
12	ORA	OR Memory with Accumulator [(ZP)]
F2	SBC	Subtract Memory from Accumulator with Borrow [(ZP)]
92	STA	Store Accumulator in Memory [(ZP)]

TABLE 8. INSTRUCTION SET OPCODE MATRIX

The following matrix shows the 210 op codes associated with the VL65NC02 microprocessor. The matrix identifies the hexadecimal code, the addressing mode, and the number of machine cycles associated with each op code.

MSD	LSD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
0		BRK Implied 1 7	ORA (IND, X) 2 6			TSB ZP 2 5	ORA ZP 2 3	ASL ZP 2 5	RMB0 ZP 2 5	PHP Implied 1 3	ORA IMM 2 2	ASL Accum 1 2		TSB ABS 3 6	ORA ABS 3 4	ASL ABS 3 6	BBR0 ZP 3 5**	0
1		BPL Relative 2 2**	ORA (IND), Y 2 5*	ORA (IND) 2 5		TRB ZP 2 5	ORA ZP, X 2 4	ASL ZP, X 2 6	RMB1 ZP 2 5	CLC Implied 1 2	ORA ABS, Y 3 4*	INC Accum 1 2		TRB ABS 3 6	ORA ABS, X 3 4*	ASL ABS, X 3 7	BBR1 ZP 3 5**	1
2		JSR ABS 3 6	AND (IND, X) 2 6			BIT ZP 2 3	AND ZP 2 3	ROL ZP 2 5	RMB2 ZP 2 5	PLP Implied 1 4	AND IMM 2 2	ROL Accum 1 2		BIT ABS 3 4	AND ABS 3 4	ROL ABS 3 6	BBR2 ZP 3 5**	2
3		BMI Relative 2 2**	AND (IND), Y 2 5*	AND (IND) 2 5		BIT ZP, X 2 4	AND ZP, X 2 4	ROL ZP, X 2 6	RMB3 ZP 2 5	SEC Implied 1 2	AND ABS, Y 3 4*	DEC Accum 1 2		BIT ABS, X 3 4*	AND ABS, X 3 4*	ROL ABS, X 3 7	BBR3 ZP 3 5**	3
4		RTI Implied 1 6	EOR (IND, X) 2 6				EOR ZP 2 3	LSR ZP 2 5	RMB4 ZP 2 5	PHA Implied 1 3	EOR IMM 2 2	LSR Accum 1 2		JMP ABS 3 3	EOR ABS 3 4	LSR ABS 3 6	BBR4 ZP 3 5**	4
5		BVC Relative 2 2**	EOR (IND), Y 2 5*	EOR (IND) 2 5			EOR ZP, X 2 4	LSR ZP, X 2 6	RMB5 ZP 2 5	CLI Implied 1 2	EOR ABS, Y 3 4*	PHY Implied 1 3			EOR ABS, X 3 4*	LSR ABS, X 3 7	BBR5 ZP 3 5**	5
6		RTS Implied 1 6	ADC (IND, X) 2 6†			STZ ZP 2 3	ADC ZP 2 3†	ROR ZP 2 5	RMB6 ZP 2 5	PLA Implied 1 4	ADC IMM 2 2†	ROR Accum 1 2		JMP (ABS) 3 6	ADC ABS 3 4†	ROR ABS 3 6	BBR6 ZP 3 5**	6
7		BVS Relative 2 2**	ADC (IND), Y 2 5†	ADC (IND) 2 5†		STZ ZP, X 2 4	ADC ZP, X 2 4†	ROR ZP, X 2 6	RMB7 ZP 2 5	SEI Implied 1 2	ADC ABS, Y 3 4†	PLY Implied 1 4		JMP (ABS, X) 3 6	ADC ABS, X 3 4†	ROR ABS, X 3 7	BBR7 ZP 3 5**	7
8		BRA Relative 2 3*	STA (IND, X) 2 6			STY ZP 2 3	STA ZP 2 3	STX ZP 2 3	SMB0 ZP 2 5	DEY Implied 1 2	BIT IMM 2 2	TXA Implied 1 2		STY ABS 3 4	STA ABS 3 4	STX ABS 3 4	BBS0 ZP 3 5**	8
9		BCC Relative 2 2**	STA (IND), Y 2 6	STA (IND) 2 5		STY ZP, X 2 4	STA ZP, X 2 4	STX ZP, Y 2 4	SMB1 ZP 2 5	TYA Implied 1 2	STA ABS, Y 3 5	TXS Implied 1 2		STZ ABS 3 4	STA ABS, X 3 5	STZ ABS, X 3 5	BBS1 ZP 3 5**	9
A		LDY IMM 2 2	LDA (IND, X) 2 6	LDX IMM 2 2		LDY ZP 2 3	LDA ZP 2 3	LDX ZP 2 3	SMB2 ZP 2 5	TAY Implied 1 2	LDA IMM 2 2	TAX Implied 1 2		LDY ABS 3 4	LDA ABS 3 4	LDX ABS 3 4	BBS2 ZP 3 5**	A
B		BCS Relative 2 2**	LDA (IND), Y 2 5*	LDA (IND) 2 5		LDY ZP, X 2 4	LDA ZP, X 2 4	LDX ZP, Y 2 4	SMB3 ZP 2 5	CLV Implied 1 2	LDA ABS, Y 3 4*	TSX Implied 1 2		LDY ABS, X 3 4*	LDA ABS, X 3 4*	LDX ABS, Y 3 4*	BBS3 ZP 3 5**	B
C		CPY IMM 2 2	CMP (IND, X) 2 6			CPY ZP 2 3	CMP ZP 2 3	DEC ZP 2 5	SMB4 ZP 2 5	INY Implied 1 2	CMP IMM 2 2	DEX Implied 1 2		CPY ABS 3 4	CMP ABS 3 4	DEC ABS 3 6	BBS4 ZP 3 5**	C
D		BNE Relative 2 2**	CMP (IND), Y 2 5*	CMP (IND) 2 5			CMP ZP, X 2 4	DEC ZP, X 2 6	SMB5 ZP 2 5	CLD Implied 1 2	CMP ABS, Y 3 4*	PHX Implied 1 3			CMP ABS, X 3 4*	DEC ABS, X 3 7	BBS5 ZP 3 5**	D
E		CPX IMM 2 2	SBC (IND, X) 2 6†			CPX ZP 2 3	SBC ZP 2 3†	INC ZP 2 5	SMB6 ZP 2 5	INX Implied 1 2	SBC IMM 2 2†	NOP Implied 1 2		CPX ABS 3 4	SBC ABS 3 4†	INC ABS 3 6	BBS6 ZP 3 5**	E
F		BEQ Relative 2 2**	SBC (IND), Y 2 5†	SBC (IND) 2 5†			SBC ZP, X 2 4†	INC ZP, X 2 6	SMB7 ZP 2 5	SED Implied 1 2	SBC ABS, Y 3 4†	PLX Implied 1 4			SBC ABS, X 3 4†	INC ABS, X 3 7	BBS7 ZP 3 5**	F



— New Opcode

0	BRK Implied 1 7
---	-----------------------

—OP Code
—Addressing Mode
—Instruction Bytes; Machine Cycles

†Add 1 to N if in decimal mode.
*Add 1 to N if page boundary is crossed.
**Add 1 to N if branch occurs to same page;
Add 2 to N if branch occurs to different page.

Note: All of the op codes in column 7 and column F are interpreted as a NOP in the 65NC02.

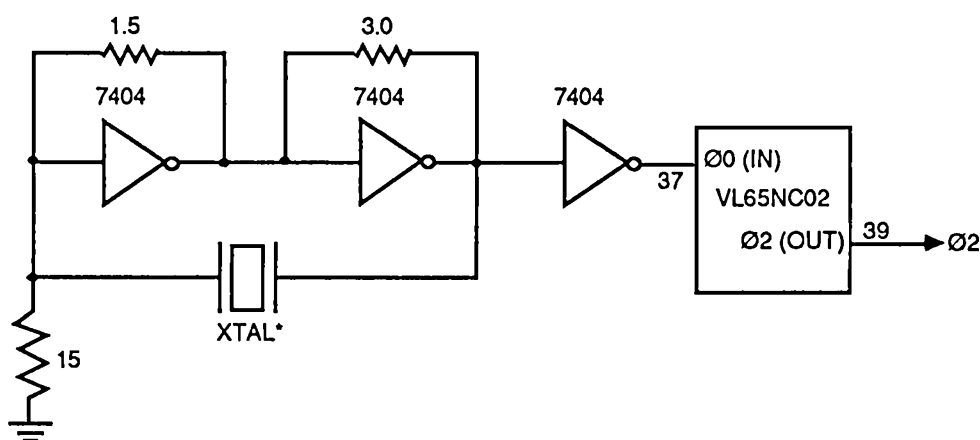
CRYSTAL/CLOCK CONSIDERATIONS

Figure 1 shows a time base generation scheme for 4 MHz operation of the VL65NC02 that has been tested and proven reliable for normal environments. As with any clock oscillator circuit, stray capacitance due to board layout can cause unpredictable results requiring "fine tuning" of the circuit. Figure 2 shows a possible external clock scheme for standby mode. Table 9 identifies nominal crystal parameters for five crystal frequencies.

Parameter	Frequency (MHz)					Units
	3.58	4.0	6.0	8.0	10.0	
RS	60	50	30-50	20-40	10-30	Ω
C0	3.5	6.5	4-6	4-6	3-5	pF
C1	0.15	0.025	0.01-0.02	0.01-0.02	0.01-0.02	pF
Q	740K	730K	720K	720K	720K	

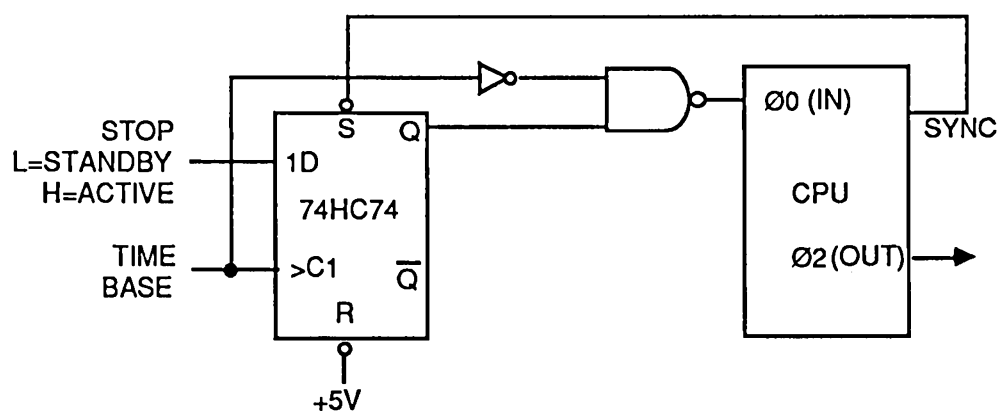
Note: AT-cut crystal parameters only. Others may be used.

FIGURE 1. TIME BASE GENERATOR



Note: CTS Knights MP Series or equivalent.

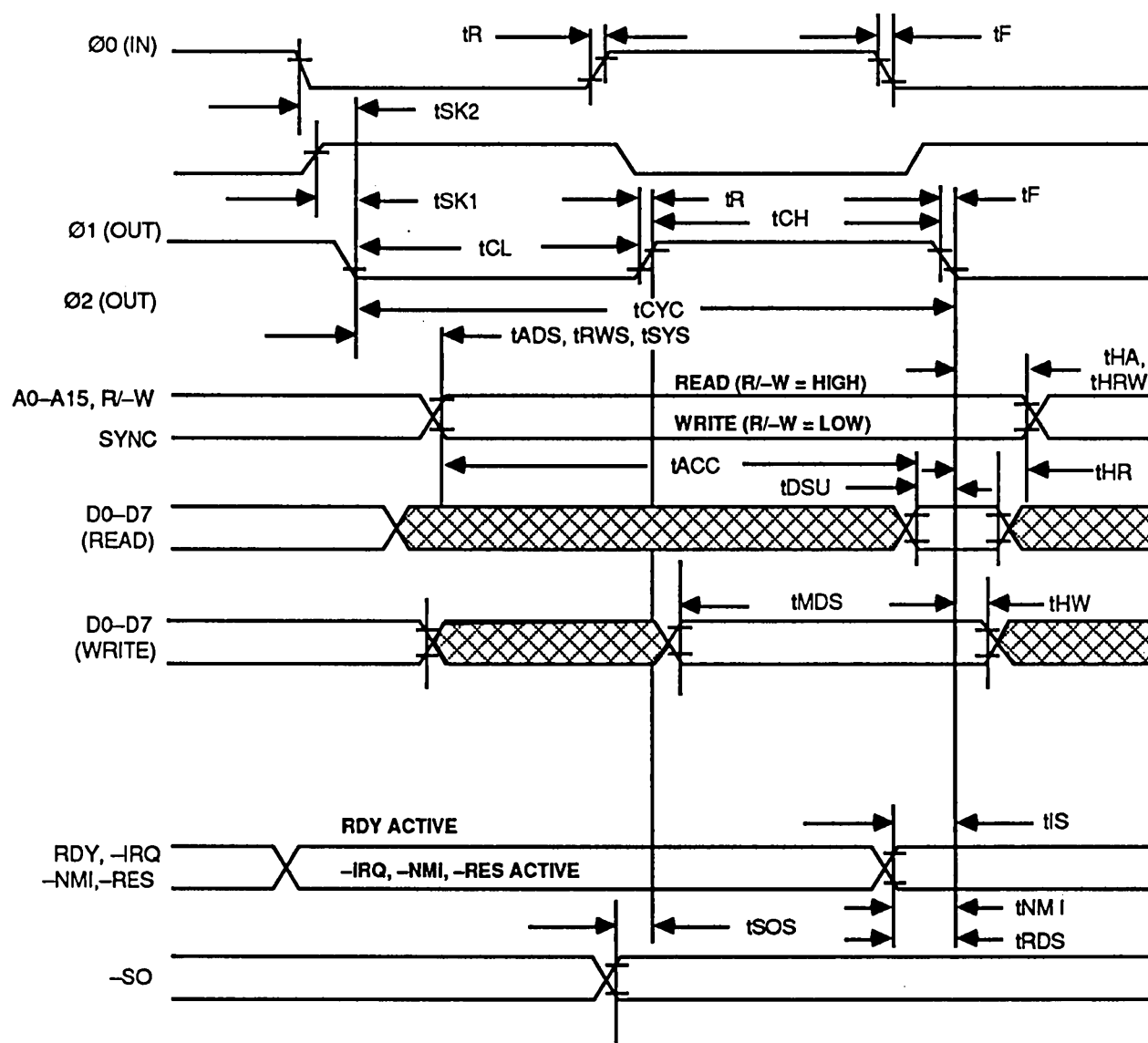
FIGURE 2. STANDBY MODE



STOPPING THE CLOCK-STANDBY MODE

Caution must be exercised when configuring the VL65NC02 in the standby mode (i.e., Ø0 (IN) clock stopped). The input clock can be held in the high state indefinitely; however, if the input clock is held in the low state longer than five μ s, internal register and data status can be lost. Figure 2 shows a circuit that stops the Ø0 (IN) clock in the high state during standby mode.

FIGURE 3. TIMING DIAGRAM



Note: All timing is referenced from a high level of 2.4 volts and a low level of 0.5 volts.

AC CHARACTERISTICS: TA = 0°C to +70°C, VCC = 5 V ±5%
CLOCK TIMING

Symbol	Parameter	1 MHz		2 MHz		3 MHz		4 MHz		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
tCYC	Ø2 Cycle Time	1000	Note(1)	500	Note(1)	333	Note(1)	250	Note(1)	ns
tCL	Ø2 Low Pulse Width	430	5000	210	5000	150	5000	100	5000	ns
tCH	Ø2 High Pulse Width	450	-	220	-	160	-	110	-	ns
tSK2	Ø0 to Ø2 Low Skew	-	50	-	50	-	40	-	30	ns
tSK1	Ø2 LOW to Ø1 High Skew	- 20	20	- 20	20	- 20	20	- 20	20	ns
tR, tF	Clock Rise and Fall Times	-	25	-	20	-	15	-	12	ns

READ/WRITE TIMING

Symbol	Parameter	1 MHz		2 MHz		3 MHz		4 MHz		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
tRWS	R/-W Setup Time	-	125	-	100	-	75	-	60	ns
tHRW	R/-W Hold Time	15	-	15	-	15	-	15	-	ns
tADS	Address Setup Time	-	125	-	100	-	75	-	60	ns
tHA	Address Hold Time	15	-	15	-	15	-	15	-	ns
tACC	Read Access Time	775	-	340	-	215	-	160	-	ns
tDSU	Read Data Setup Time	100	-	60	-	40	-	30	-	ns
tHR	Read Data Hold Time	10	-	10	-	10	-	10	-	ns
tMDS	Write Data Delay Time	-	200	-	110	-	85	-	55	ns
tHW	Write Data Hold Time	30	-	30	-	30	-	30	-	ns

CONTROL SIGNAL TIMING

Symbol	Parameter	1 MHz		2 MHz		3 MHz		4 MHz		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
tSYS	SYNC Delay	-	125	-	100	-	75	-	60	ns
tRDS	RDY Setup Time	200	-	110	-	80	-	60	-	ns
tSOS	-SO Setup Time	75	-	50	-	40	-	30	-	ns
tIS	-IRQ,-RES Setup Time	200	-	110	-	80	-	60	-	ns
tNMI	-NMI Setup Time	200	-	150	-	100	-	70	-	ns

Notes:

1. VL65NC02 minimum operating frequency is limited by Ø2 low pulse width. The processor can be stopped with Ø2 held high.

ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature:

– Commercial 0°C to +70°C

– Industrial -40°C to +85°C

Storage Temperature -65°C to +150°C

Supply Voltage to
Ground Potential -0.3 to +7.0 V

Applied Output
Voltage -0.3 to VCC + 0.3 V

Applied Input
Voltage -0.3 to VCC + 0.3 V

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or other conditions above those indicated in the

operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS: TA = 0°C to +70°C, VCC = +5.0 V ± 5% (Notes 1, 2, 3)

Symbol	Parameter		Min	Typ	Max	Units	Test Conditions
VIH	Input High Voltage	Ø0 (IN)	2.4	-	VCC + 0.3	V	
		All Other Inputs	2.0	-	VCC + 0.3	V	
VIL	Input Low Voltage	Ø0 (IN)	-0.3	-	+ 0.4	V	
		All Other Inputs	-0.3	-	+ 0.8	V	
IIN	Input Leakage Current	Ø0 (IN)	-	-	1.0	µA	VIN = 0 V to +5.25 V VCC = 0 V
		-NMI, -IRQ, RDY, -RES, -SO	-	-	-50	µA	
ITSI	Three-State (Off-State) Input Current D7 - D0		-	-	10	µA	VIN = 0.4 V to +2.4 V VCC = +5.25 V
VOH	Output High Voltage SYNC, D7-D0, A15-A0, R/-W, Ø1, Ø2		2.4	-	-	V	VCC = +4.75 V ILOAD = -100 µA
VOL	Output Low Voltage SYNC, D7-D0, A15-A0, R/-W, Ø1, Ø2		-	-	+0.4	V	VCC = +4.75 V ILOAD = 1.6 µA
ICC	Supply Current	Standby (4)	-	2.0	10	µA	VCC = +5.0 V
		Active (5)	-	2.6	-	mA/MHz	
		Active (6)	-	-	10	mA	
		Low Power	-	1.1	-	mA/MHz	RDY = 0 V
CIN	Input Capacitance	-NMI, -IRQ, -SO, RDY	-	-	7	pF	VCC = +5.0 V, VIN = 0 V, f = 1 MHz, TA = 25°C
		Ø0 (IN)	-	-	30	pF	
CIO	I/O Capacitance - D7-D0, Ø1, Ø2		-	-	10	pF	
COUT	Output Capacitance - A15-A0, R/-W, SYNC		-	-	10	pF	

Notes:

(1) All units are direct current (DC).

(2) A negative sign indicates outward current flow, positive indicates inward flow.

(3) -IRQ and -NMI require an external pull-up resistor.

(4) Typical values are shown for VCC = +5.0 V and TA = +25°C.

(5) Typical value for power estimation only; dependent on frequency of operation.

(6) Maximum value for power consumption; independent of frequency of operation.

PARALLEL INTERFACE/TIMER

FEATURES

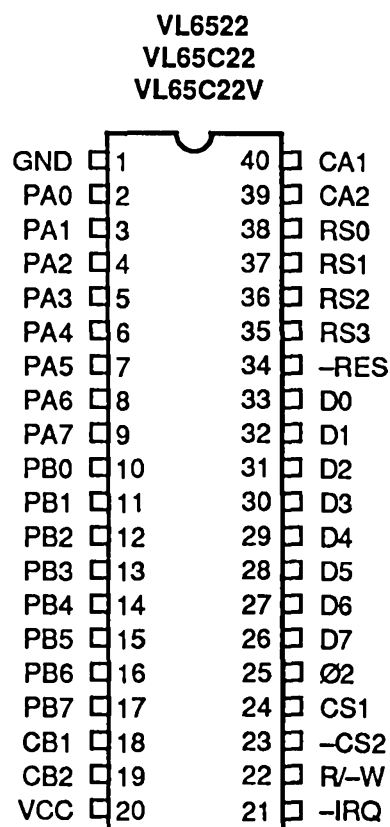
- Low power consuming CMOS parallel interface/timer
 - VL65C22 has active pull-ups on Port "B"
 - VL65C22V has resistive pull-ups on Port "B"
- Low cost HMOS parallel interface/timer (VL6522)
- Two 8-bit bidirectional I/O ports
- Two 16-bit timer/counters
- Serial bidirectional peripheral I/O port
- Programmable Data Direction Registers

DESCRIPTION

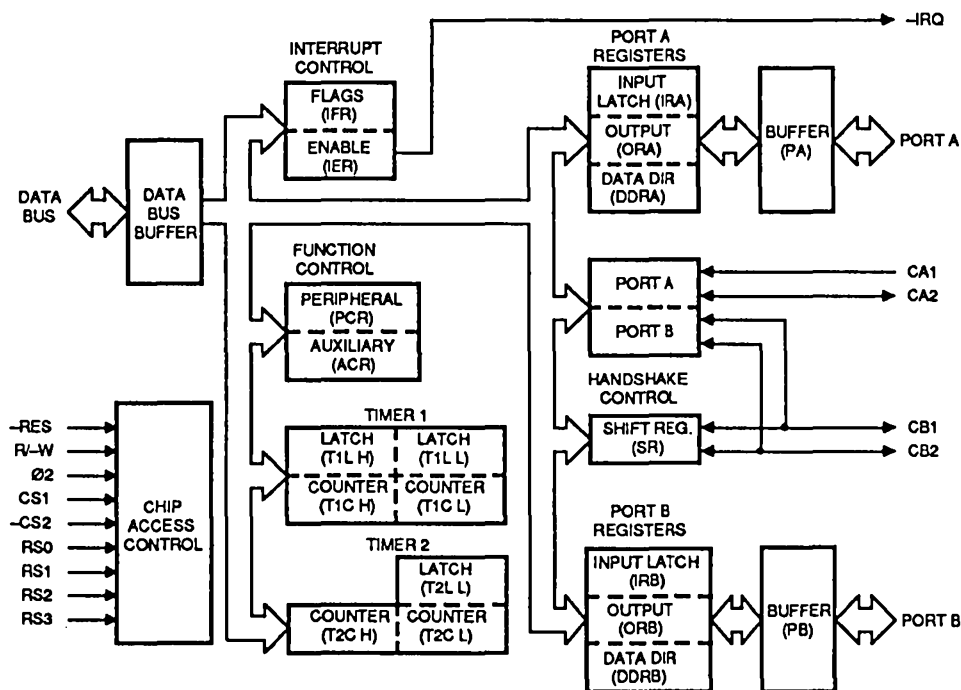
The VL6522/VL65C22/VL65C22V are flexible I/O devices for use with the 65XX family of processors. The VL65C22/VL65C22V are CMOS implementations of the VL6522 device. All include functions for programmed control of up to two peripheral devices (Ports A and B). Two program-controlled 8-bit bidirectional peripheral I/O ports allow direct interfacing between the microprocessor and selected peripheral devices. Two programmable Data Direction Registers (A and B) allow selection of data direction (input versus output) on an individual line-by-

line basis. Also provided are two programmable 16-bit counter/timers with latches. Timer 1 may be operated in a one-shot interrupt mode with interrupts on each count-to-zero, or in a free-running mode with a series of evenly spaced interrupts. Timer 2 functions both as an interval and pulse counter. Serial data transfers are provided by a shift register. Application versatility is further increased by various control registers, including an interrupt flag register, an interrupt enable register, and two function control registers.

PIN DIAGRAM



BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Technology	Clock Frequency	Package
VL6522-01PC	HMOS	1 MHz	Plastic DIP
VL6522-01QC	HMOS		Plastic Leaded Chip Carrier (PLCC)
VL6522-02PC	HMOS	2 MHz	Plastic DIP
VL65C22-02PC	CMOS		Plastic DIP
VL65C22V-02PC	CMOS		Plastic DIP
VL6522-02QC	HMOS		Plastic Leaded Chip Carrier (PLCC)
VL65C22-02QC	CMOS		Plastic Leaded Chip Carrier (PLCC)
VL65C22V-02QC	CMOS		Plastic Leaded Chip Carrier (PLCC)
VL65C22-04PC	CMOS	4 MHz	Plastic DIP
VL65C22V-04PC	CMOS		Plastic DIP
VL65C22-04QC	CMOS		Plastic Leaded Chip Carrier (PLCC)
VL65C22V-04QC	CMOS		Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range is 0°C to +70°C

PIN DIAGRAM

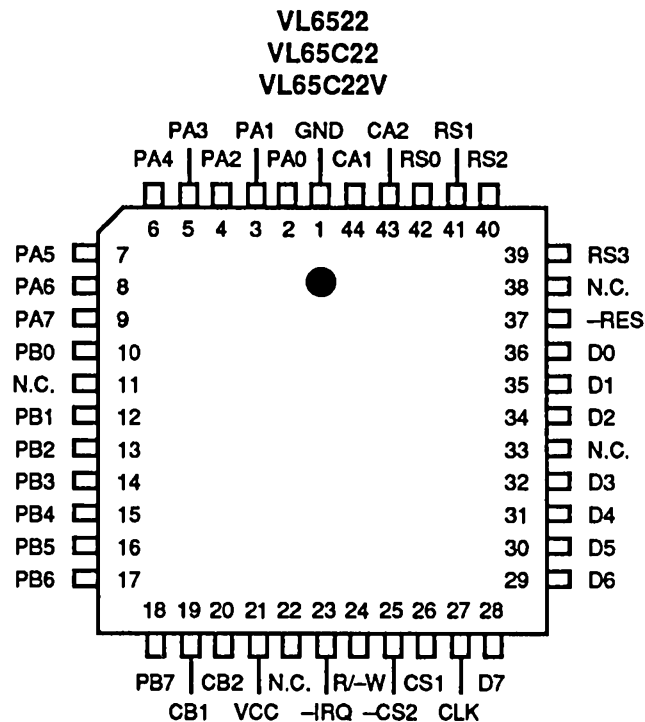
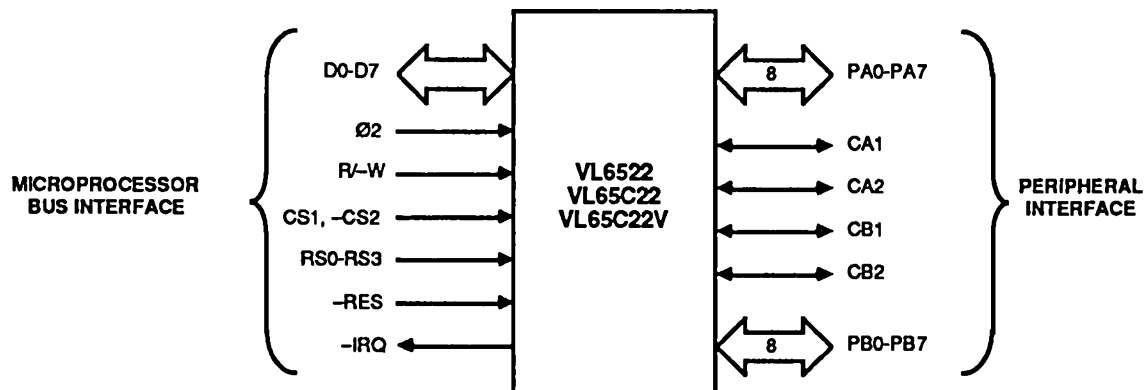


FIGURE 1. MICROPROCESSOR AND PERIPHERAL INTERFACE



FUNCTIONAL DIFFERENCES AMONG VL6522, VL65C22, AND VL65C22V

Function	VL6522	VL65C22	VL65C22V
Register Select Lines	Are Decoded During -Ø2	Are Decoded During -Ø2 Only if -CS2 is an Active Low	Are Decoded During -Ø2 Only if -CS2 is an Active Low
CB1	Must Not Change During Last 100 ns of -Ø2	Must Not Change During Last 100 ns of -Ø2	Can Change Anytime, But is Sampled Only During -Ø2
Port B (PB0 - PB7, CB1, CB2)	Has Active (Transistor) Internal Pull-ups	Has Active (Transistor) Internal Pull-ups	Has Passive (Resistor, Approx. 6 kohms) Internal Pull-ups
Port B (PB0 - PB7, CB1, CB2)	Each pin represents one Standard TTL load either as an input or as an output	Each pin represents two Standard TTL loads either as an input or as an output	Each pin represents one Standard TTL load either as an input or as an output

**SIGNAL
DESCRIPTIONS**

Signal Name	Pin Number	Signal Description
-RES	34	AA low reset (-RES) input clears all VL65(C)22(V) internal registers to logic 0 (except T1 and T2 latches and counters and the Shift Register). This places all peripheral interface lines in the input state; disables the timers, shift register, and interrupting from the chip.
Ø2	25	The input clock is the system Ø2 clock and triggers all data transfers between processor bus and the VL65(C)22(V).
R/-W	22	The direction of the data transfers between the VL65(C)22(V) and the system processor is controlled by the R/-W line and the CS1 and -CS2 inputs. When R/-W is low, (write operation) and the VL65(C)22(V) is selected, data is transferred from the processor bus into the selected VL65(C)22(V) register. When R/-W is high, (read) and the chip is selected, and data is transferred from the selected VL65(C)22(V) register to the CPU.
D0-D7	33-26	The eight bidirectional data bus lines transfer data between the VL65(C)22(V) and the system processor bus. During ready cycles, the contents of the selected VL65(C)22(V) register are placed on the data bus lines. During write cycles, these lines are high-impedance inputs and data is transferred from the processor bus into the selected register. When the VL65(C)22(V) is not selected, the data bus lines are high-impedance.
CS1, -CS2	24, 23	The two chip select inputs are normally connected to processor address lines either directly or through decoding. The selected VL65(C)22(V) register is accessed when CS1 is high and -CS2 is low.
RS0, RS1, RS2, RS3	38 - 35	The coding of the four Register Select inputs selects one of the 16 internal registers of the VL65(C)22(V), as shown in Table 2.
-IRQ	21	The Interrupt Request output goes low whenever an internal interrupt flag is set and the corresponding interrupt enable bit is a logic 1. This output is open-drain to allow the interrupt request signal to be wire-or'd with other equivalent signals in the system.
PA0 - PA7	2 - 9	Port A consists of eight lines which can be individually programmed to act as inputs or outputs under control of Data Direction Register A. The polarity of output pins is controlled by an Output Register and input data may be latched into an internal register under control of CA1 line. All modes of operation are controlled by the system processor through the internal control registers. These lines, as inputs represent one standard TTL load in the input mode and will drive one standard TTL load in the output mode.
PB0 - PB7	10 - 17	Peripheral Data Port B is an 8-line, bidirectional bus, controlled by an Output Register, Input Register and Data Direction Register similar to Data Port A. The output signal on line PB7 may be controlled by Timer 1 while Timer 2 may be programmed to count pulses on PB6 line. VL6522 and VL65C22 Port B lines are also capable of sourcing 3.0 mA at 1.5 VDC in the output mode. This allows the outputs to directly drive Darlington transistor circuits. VL65C22V Port B lines have internal pull-up resistors (3 kΩ) to VCC.
CA1, CA2	40, 39	Control Lines CA1 and CA2 serve as interrupt inputs or handshake outputs for Peripheral Data Port A. Each line controls an internal Interrupt Flag with a corresponding Interrupt Enable bit. CA1 also controls the latching of Input Data on Port A. CA1 is a high impedance input, while CA2 represents one standard TTL load in the input mode. In the output mode, CA2 will drive one standard TTL load.
CB1, CB2	18, 19	Control lines CB1 and CB2 are interrupt inputs or handshake outputs for Peripheral Data Port B. Like Port A, these two lines control an internal Interrupt Flag with a corresponding Interrupt Enable bit. These lines are also a serial data port under control of the Shift Register (SR). Each control line represents two standard TTL loads in the input mode (one TTL load on the VL65C22V) and can drive two TTL loads in the output mode (one TTL load for the VL65C22V). CB1 and CB2 cannot drive Darlington transistor circuits.
VCC	20	+5 Volts
GND	1	Ground

FUNCTIONAL DESCRIPTION

PERIPHERAL DATA PORTS (PORT A, PORT B)

Each Peripheral Data Port operates in conjunction with a Data Direction Register (DDRA or DDRB). Under program control, the Data Direction Registers specify which lines within the port bus are to be designated as inputs or outputs. A Logic 0 in any bit position of the register will cause the corresponding line to serve as an input, while a Logic 1 will cause the line to serve as an output.

When a line is programmed as an output, it is controlled by a corresponding bit in the Output Register (ORA or ORB). A Logic 1 in the Output Register will cause the corresponding output line to go high, while a Logic 0 will cause the line to go low. Under program control, data is written into the Output Register bit positions corresponding to the output lines which have been programmed as outputs. Should data be written into bit positions corresponding to lines which have been programmed as inputs, the output lines will be unaffected.

When reading a Peripheral Data Port, the contents of the corresponding Input Register (IRA or IRB) are transferred onto the Data Bus. When the input latching feature is disabled, Input Register A (IRA) will reflect the logic levels present on the Port A bus lines. However, with input latching enabled and the selected active transition on CA1 having occurred, Input Register A will contain the data present on the Port A bus lines at the time of the transition. In this case, once Input Register A has been read, it will appear transparent, reflecting the current state of the Port A bus lines until the next CA1 latching transition.

With respect to Input Register B, it operates similar to Input Register A except that for those Port B bus lines which have been programmed as outputs, there is a difference. When reading Input Register A, the logic level on the bus line determines whether a Logic 1 or 0 is sensed. However, when reading the Input Register B, the logic level stored in Output Register B (ORB) is the logic level sensed. For this reason, those outputs which have large loading effects may cause the reading of

Input Register A to result in the reading of Logic 0 when a 1 was actually programmed, and reading a Logic 1 when a 0 was programmed. However, when reading Input Register B, the logic level read will be correct, regardless of loading on the particular bus line.

For information on formats and operation of the Peripheral Data Port registers, refer to Figures 14, 15, 16, and 17. It should be noted that the input latching modes are controlled by the Auxiliary Control Register.

DATA TRANSFER - HANDSHAKE CONTROL

A powerful feature of the VL65(C)22(V) is its ability to provide absolute control over data transfers between the microprocessor and peripheral devices. This control is accomplished by way of "handshake" lines. Port A lines (CA1, CA2) handshake data transfers on both Read and Write operations, while Port B lines (CB1, CB2) handshake data on Write operations only.

READ HANDSHAKE CONTROL

Read Handshaking provides effective control of data transfers from a peripheral device to the microprocessor. To accomplish the Read Handshake, the peripheral device generates a Data Ready signal to the VL65(C)22(V) which indicates valid data is present on the Peripheral Data Port bus. In most cases, this Data Ready signal will interrupt the microprocessor, which will then read the data and generate a Data Taken signal. Once the peripheral senses the Data Taken signal, new data will be placed on the bus. This process continues until the data transfer is complete.

Automatic Read Handshaking applies to Peripheral Data Port A only. The Data Ready signal is transmitted by the peripheral device over the CA1 interrupt line, while the Data Taken signal is generated and transmitted to the peripheral device over the CA2 line. When the Data Ready signal is received, it sets an internal flag in the Interrupt Flag Register (IFR). This flag may interrupt the microprocessor or it may be polled under program control. As an option, the Data Taken signal may be either a pulse or a level. In

either case, it is set low (Logic 0) by the microprocessor and is cleared by the next Data Ready signal. Refer to Figures 2 and 3 for Read Handshake timing and operating sequence.

WRITE HANDSHAKE CONTROL

The Write Handshake operation is similar to Read Handshaking. For Write Handshaking, however, the VL65(C)22(V) generates the Data Ready signal and the peripheral device must generate the Data Taken return signal. Note that Write Handshaking may occur on both Data Ports (A and B). For a Write Handshake, CA2 or CB2 serve as the Data Ready output and can operate in either the Handshake Mode or the Pulse Mode. The Data Taken signal is received by CA1 or CB1. The Data Taken signal sets a flag in the Interrupt Flag Register and clears the Data Ready output signal. Note that the selection of Read or Write Handshake operating modes (CA1, CA2, CB1, and CB2) is accomplished by the Peripheral Control Register (PCR).

INTERRUPT OPERATION

There are three basic operations, including: setting the flag within the Interrupt Flag Register (IFR), enabling the interrupt by way of a corresponding bit in the Interrupt Enable Register (IER), and signaling the microprocessor with an Interrupt Request (IRQ). An Interrupt Flag can be set by conditions internal to the chip or by inputs to the chip from external sources. Normally, an Interrupt Flag remains set until the interrupt is serviced. To determine the source of an interrupt, the microprocessor must examine each flag in order, from highest to lowest priority. This is accomplished by reading the contents of the Interrupt Flag Register into the microprocessor accumulator, shifting the contents either left or right and then using conditional branch instructions to detect an active interrupt. Each Interrupt Flag has a corresponding Interrupt Enable bit in the Interrupt Enable Register. The enable bits are controlled by the microprocessor (set or reset). If an Interrupt Flag is high (Logic 1), and the corresponding Interrupt Enable bit is high (Logic 1), the Interrupt Request (IRQ) will go low (Logic 0).



FUNCTIONAL DESCRIPTION (Cont.)

IRQ is an open-collector output which can be wire-or'd with other devices within the system.

All Interrupt Flags are contained within a single Interrupt Flag Register. Bit 7 of this register will be high (Logic 1) whenever an Interrupt Flag is set, thus allowing convenient polling of several devices within a system to determine the source of the interrupt.

The Interrupt Flag Register (IFR) and Interrupt Enable Register (IER) format and operation is shown in Figures 28 and 29 respectively. The Interrupt Flag Register may be read directly by the microprocessor, and individual flag bits may be cleared by Writing a "1" into the appropriate bit of the IFR. Bit 7 of the IFR indicates the status of the Interrupt Request (IRQ) output. Bit 7 corresponds to the following logic function:

$$\text{IRQ} = \text{IFR6} \times \text{IER6} + \text{IFR5} \times \text{IER5} + \text{IFR4} \times \text{IER4} + \text{IFR3} \times \text{IER3} + \text{IFR2} \times \text{IER2} + \text{IFR1} \times \text{IER1} + \text{IFR0} \times \text{IER0}.$$
 Note \times = LogicAND, $+$ = LogicOR.

Bit 7 is not a flag. For this reason, bit 7 is not directly cleared by writing a "1" into its bit position. It can be cleared, however, by clearing all the flags within the register, or by disabling all active interrupts in the next section.

TIMER OPERATION

Timer 1 Operation - Interval Timer T1 consists of two 8-bit latches and a 16-bit counter. The latches serve to store data which is to be loaded into the counter. Once the counter is loaded under program control, it decrements at a Phase 2 ($\emptyset 2$) clock rate. Upon reaching zero, an Interrupt Flag is set, causing Interrupt Request (IRQ) to go low (Logic 0) if the corresponding Interrupt Enable bit is set. Once the Timer reaches a count of zero, it will either disable any further interrupts (provided it has been programmed to do so), or it will automatically transfer the contents of the latches into the counter and proceed to decrement again. The counter may be programmed to invert the output signal on PB7 each time it reaches a count of zero. Additional control bits are provided in the Auxiliary Control Register (bits 6 and 7) to allow selection of Timer 1 operating modes.

It should be noted that the microprocessor does not write directly into the low-order counter (T1C-L). Instead, this half of the counter is loaded automatically from the low-order register when the microprocessor writes into the high-order register and counter. In fact, it may not be necessary to write to the low-order register in some applications since the timing operation is triggered by writing to the high-order register and counter.

Timer 1 One-Shot Mode - Interval Timer T1 may operate in the One-Shot Mode which allows the generation of a single Interrupt Flag each time the Timer is loaded. The Timer can also be programmed to produce a single negative pulse on Data Port Line PB7.

To generate a single interrupt, it is required that bits 6 and 7 of the Auxiliary Control Register be low (Logic 0). The low-order T1 counter (T1C-L) or the low-order T1 latch (T1L-L) must then be loaded with the low-order count value. Note that a load to T1C-L is effectively a load to T1L-L. Next, the high-order count value must be loaded into the high-order T1 counter (T1C-H), at which time the value is simultaneously loaded into high-order T1 latch (T1L-H). During this load sequence, the contents of T1L-L is transferred to T1C-L. The counter will start counting down on the next $\emptyset 2$ clock following the load sequence into T1C-H, and will decrement at the $\emptyset 2$ clock rate. Once the T1 counter reaches a zero count, the Interrupt Flag is set. To generate a negative pulse on Data Port line PB7, the sequence is identical to the above except bit 7 of the Auxiliary Control Register must be high (Logic 1). Data Port line PB7 will then go low (Logic 0) following the load to T1C-H, and will go high (Logic 1) again when the counter reaches a zero count. Once set, the T1 Interrupt Flag is reset by either loading T1C-H, which starts a new count, or by reading T1C-L.

Timer 1 Free-Run Mode - An important advantage within the VL65C22 is the ability of the latches associated with the T1 counter to provide a continuous series of evenly spaced interrupts or a square wave on Data Port line PB7. It

should also be noted that the continuous series of interrupts and square waves are not affected by variations in the microprocessor interrupt response time. These advantages are all produced in the Free-Run Mode. When operating in the Free-Run Mode, the Interrupt Flag is set and the signal on PB7 is inverted each time the counter reaches a count of zero. In the Free-Run Mode, however, the counter does not continue to decrement after reaching a zero count. Instead, the counter automatically transfers the contents of the latch into the counter (16 bits) and then decrements from the new count value. As can be seen, it is not necessary to reload the timer in order to set the Interrupt Flag on the next count of zero. When set, the Interrupt Flag can be cleared by either reading T1C-L, by writing directly into the Interrupt Flag Register (IFR) as will be discussed later, or by a load into T1C-H when a new count value is desired.

Since the interval timers are all retriggerable, reloading the counter will always reinitialize the time-out period. Should the microprocessor continue to reload the counter before it reaches zero, counter time-out can be prevented. Timer 1 is able to operate in this manner provided the microprocessor writes into the high-order counter (T1C-H). By loading the latches only, the microprocessor can access the timer during each count-down operation without affecting the time-out in progress. In this way, data loaded into the latches will determine the length of the next subsequent time-out period. This capability is of value in the Free-Run Mode with the output enabled. In the Free-Run Mode, the signal on Data Port line PB7 is inverted and the Interrupt Flag is set with each counter time-out. When the microprocessor responds to the interrupts with new data for the latches, it can determine the period of the next half-cycle during each half-cycle of the output signal on line PB7. In this way, complex waveforms can be generated.

Timer 2 Operation - Timer 2 operates in the One-Shot Mode only (as an interval timer), or as a pulse counter for



FUNCTIONAL DESCRIPTION (Cont.)

counting negative pulses on Data Port line PB6. A single control bit within the Auxiliary Control Register is used to select between these two modes. Timer 2 is made up of a write-only low-order latch (T2L-L), a read-only low-order counter (T2C-L), and a read/write high-order counter (T2C-H). This 16-bit counter decrements at a $\emptyset 2$ clock rate.

Timer 2 One-Shot Mode - Operation of Timer 2 in the One-Shot Mode is similar to Timer 1. That is, for each load T2C-H operation, Timer 2 sets the Interrupt Flag for each countdown to zero. However, after a time-out, the T2 counters roll over to all 1's (FFF16) and continue to decrement. This two's complement decrement allows the user to determine how long the T2 Interrupt Flag has been set. Since the Interrupt Flag logic is disabled after the initial interrupt set (zero count), further interrupts cannot be set by a subsequent count to zero. To enable the Interrupt Flag logic, the microprocessor must reload T2C-H. The Interrupt Flag is cleared by either reading T2C-L or by loading T2C-H.

Timer 2 Pulse Counting Mode-In the Pulse Counting Mode, Timer 2 counts a predetermined number of negative-going pulses on Data Port line PB6. To accomplish this, a count number is loaded into T2C-H, which clears the Interrupt Flag logic and starts the counter to decrement each time a negative pulse is applied to Data Port line PB6. When the T2 counter reaches a count of zero, the Interrupt Flag is set and the counter continues to decrement with each pulse on PB6. To enable the Interrupt Flag for subsequent count-downs, it is necessary to reload T2C-H. The decrement pulse on line PB6 must be low (Logic 0) during the leading edge of the $\emptyset 2$ clock.

SHIFT REGISTER OPERATION AND MODES

Shift Register Operation - The Shift Register performs bidirectional serial data transfers on line CB2. These transfers are controlled by an internal modulo-8 counter. Shift pulses can be applied to the CB1 line for controlling external devices. Each Shift Register

operating mode is controlled by control bits within the Auxiliary Control Register.

Shift Register Input Modes - Shift Register Disabled (000) - In the 000 mode, the Shift Register is disabled from all operation. the microprocessor can read or write the Shift Register, but shifting is disabled and both CB1 and CB2 are controlled by bits in the Peripheral Control Register (PCR). The Shift Register Interrupt Flag is held low (disabled).

Shift In - Counter T2 Control (001) - In this mode, the shifting rate is controlled by the low order eight bits of counter T2. Shift pulses are generated on the CB1 line to control shifting in external devices. The time between transitions of the CB1 output clock is determined by the $\emptyset 2$ clock period and the contents of the low-order T2 latch (N). Shifting occurs by writing or reading the Shift Register. Data is shifted into the low-order bit first, and is then shifted into the next higher order bit on the negative-going edge of each clock pulse. Input data should change before the positive-going edge of the CB1 clock pulse. This data is then shifted into the Shift Register during the $\emptyset 2$ clock cycle following the positive-going edge of the CB1 clock pulse. After eight CB1 clock pulses, the Shift Register Interrupt Flag will set the IRQ will go low (Logic 0).

Shift In - $\emptyset 2$ Clock Control (010) - In this mode, the shift rate is controlled by the $\emptyset 2$ clock frequency. Shift pulses are generated on the CB1 line to control shifting in external devices. Timer 2 operates as an independent interval timer and has no influence on the Shift Register. Shifting occurs by reading or writing the Shift Register. Data is shifted into the low order bit first, and is then shifted into the next higher order bit on the trailing edge of the $\emptyset 2$ clock pulse. After eight clock pulses, the Shift Register Interrupt Flag will be set and output clock pulses on the CB1 line will stop.

Shift In - External CB1 Clock Control (011) - In this mode, CB1 serves as an input to the Shift Register. In this way, an external device can load the Shift Register at its own pace. The Shift Register counter will interrupt the

microprocessor after each eight bits have been shifted in. The Shift Register counter does not stop the shifting operation. Its function is simply that of a pulse counter. Reading or writing the Shift Register resets the Interrupt Flag and initializes the counter to count another eight pulses. Note that data is shifted during the first $\emptyset 2$ clock cycle following the positive-going edge of the CB1 shift pulse. For this reason, data must be held stable during the first full cycle following CB1 going high.

Shift Out - Free Running at T2 Rate (100) -This mode is similar to mode 101 in which the shifting rate is determined by T2. However, in mode 100 the Shift Register Counter does not stop the shifting operation. Since Shift Register bit 7 (SR7) is recirculated back into bit 0, the eight bits loaded into the Shift Register will be clocked onto the CR2 line repetitively. In this mode, the Shift Register Counter is disabled and IRQ is never set.

Shift Out - T2 Control (101) - In this mode, the shift rate is controlled by T2 (as in mode 100). However, with each read or write of the Shift Register, the Shift Register Counter is reset and eight bits are shifted onto the CB2 line. At the same time, eight shift pulses are placed on the CB1 line to control shifting in external devices. After the eight shift pulses, the shifting is disabled, the Interrupt Flag is set, and CB2 will remain at the last data level.

Shift Out - $\emptyset 2$ Clock Control (110) - In this mode, the shift rate is controlled by the system $\emptyset 2$ Clock.

Shift Out - External CB1 Clock Control (111) - In this mode, shifting is controlled by external pulses applied to the CB1 line. The Shift Register Counter sets the Interrupt Flag for each eight-pulse count, but does not disable the shifting function. Each time the microprocessor reads or writes to the Shift Register, the Interrupt Flag is reset and the counter is initialized to begin counting the next eight pulses on the CB1 line. After eight shift pulses, the Interrupt Flag is set. The microprocessor can then load the Shift Register with the next eight bits of data.

TABLE 1. PERIPHERAL INTERFACE CHARACTERISTICS $T_A = 0^\circ\text{C to } 70^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 5\%$

Symbol	Parameter	Min	Typ	Max	Unit
tR, tF	Rise and Fall Time for CA1, CB1, CA2 and CB2 Input Signals			1.0	μs
tCA2	Delay Time, Clock Negative Transition to CA2 Negative Transition (Read Handshake or Pulse Mode)			1.0	μs
tRS1	Delay Time, Clock Negative Transition to CA2 Positive Transition (Pulse Mode)			1.0	μs
tRS2	Delay Time, CA1 Active Transition to CA2 Positive Transition (Handshake Mode)			2.0	μs
tWHS	Delay Time, Clock Positive Transition to CA2 or CB2 Negative Transition (Write Handshake)	0.05		1.0	μs
tDS	Delay Time, Peripheral Data Valid to CB2 Negative Transition	0.20		1.5	μs
tRS3	Delay Time, Clock Positive Transition to CA2 or CB2 Positive Transition (Pulse Mode)			1.0	μs
tRS4	Delay Time, CA1 or CB1 Active Transition to CA2 or CB2 Positive Transition (Handshake Mode)			2.0	μs
t21	Delay Time Required from CA2 Output to CA1 Active Transition (Handshake Mode)	400			ns
tIL	Set-up Time, Peripheral Data Valid to CA1 or CB1 Active Transition (Input Latching)	300			ns
tSR1	Shift-Out Delay Time - Time from Ø2 Falling Edge to CB2 Data Out			300	ns
tSR2	Shift-In Set-up Time - Time from CB2 Data In to Ø2 Rising Edge	300*			ns
tSR3	External Shift Clock (CB1) Set-up Time Relative to Ø2 Trailing Edge	100		tCYC	ns
tIPW	Pulse Width - PB6 Input Pulse	2 x tCYC			
tICW	Pulse Width - CB1 Input Clock	2 x tCYC			
tIPS	Pulse Spacing - PB6 Input Pulse	2 x tCYC			
tICS	Pulse Spacing - CB1 Input Pulse	2 x tCYC			
tAL	CA1, CB1 Set Up Prior to Transition to Arm Latch	300			ns
tPDH	Peripheral Data Hold After CA1, CB1 Transition	150			ns

*Note: This specification is "0" (zero) on the VL65C22V.

FIGURE 2. TIMING FOR READ HANDSHAKE, PULSE MODE

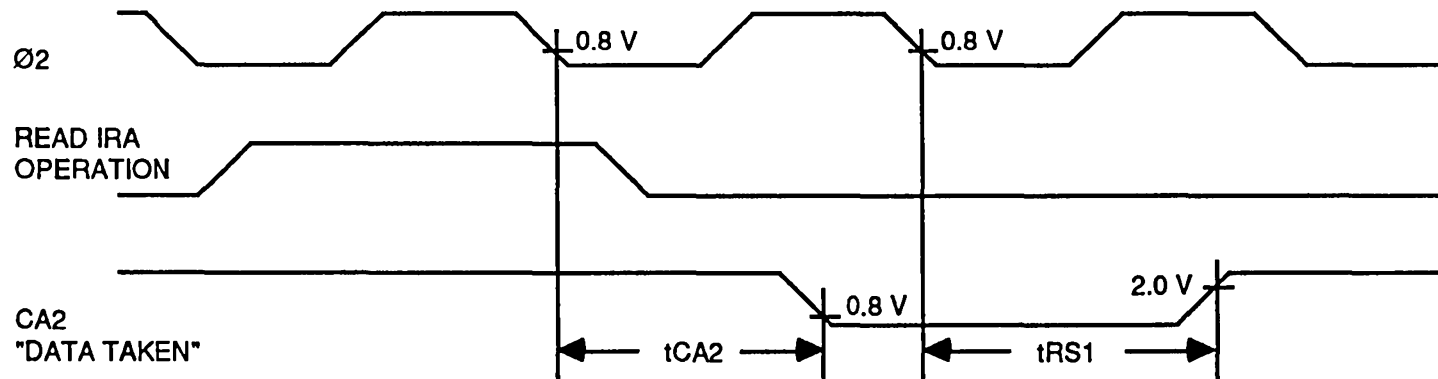


FIGURE 3. TIMING FOR READ HANDSHAKE, HANDSHAKE MODE

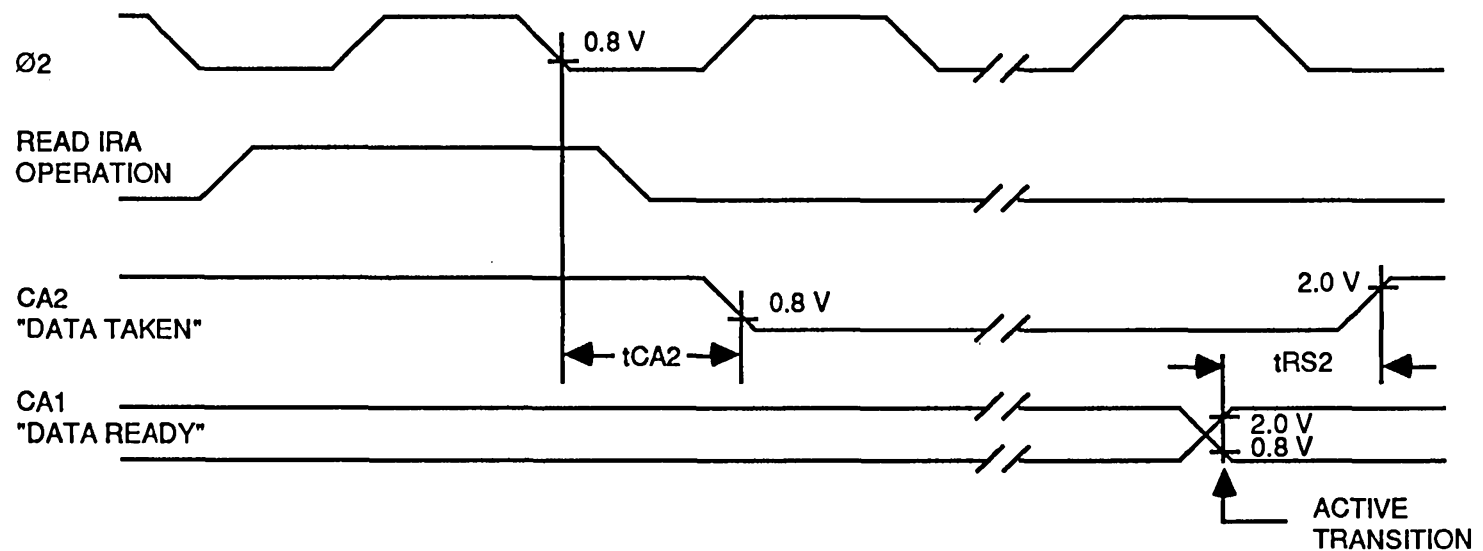


FIGURE 4. TIMING FOR WRITE HANDSHAKE, PULSE MODE

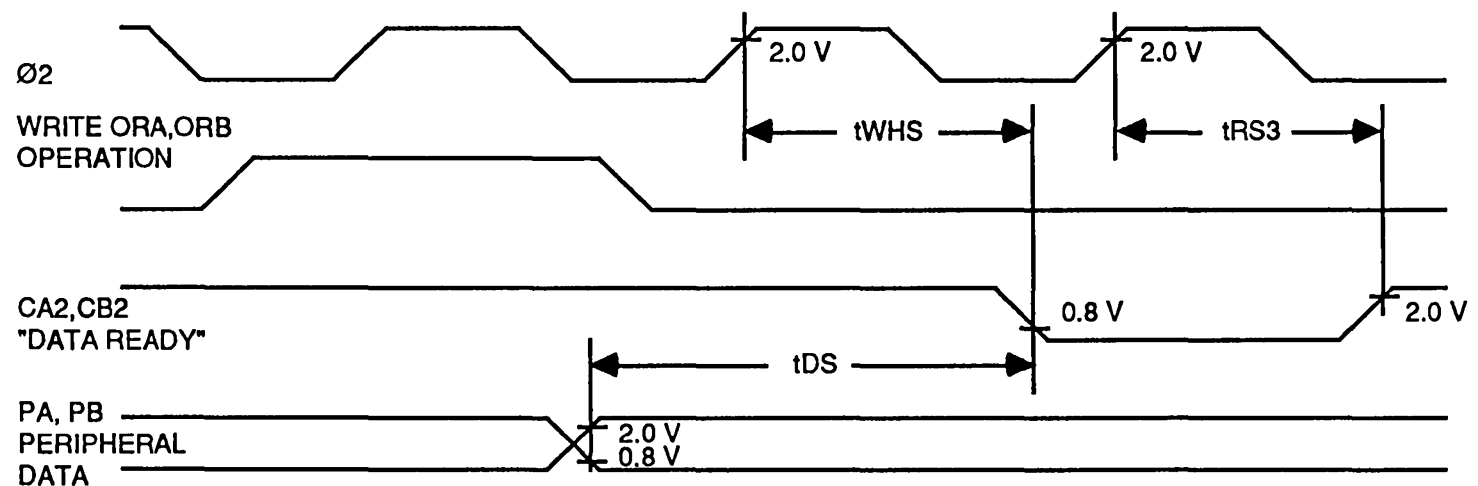


FIGURE 5. TIMING FOR WRITE HANDSHAKE, HANDSHAKE MODE

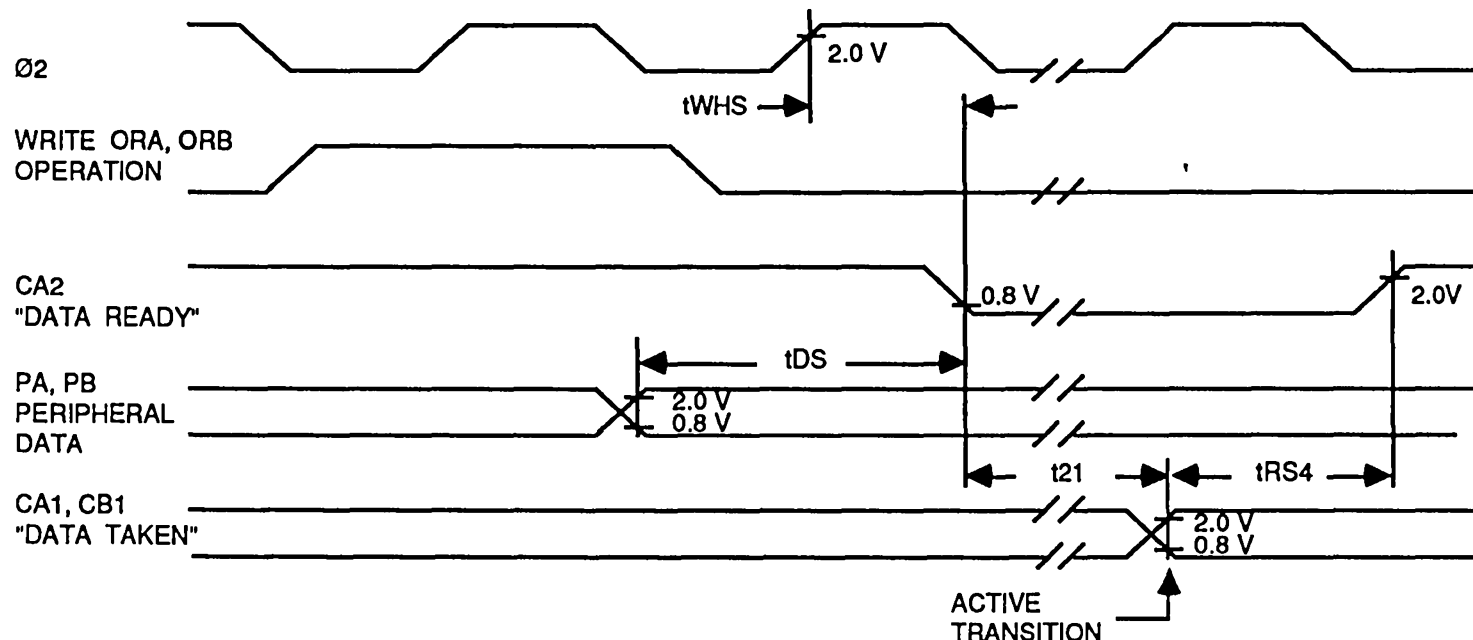


FIGURE 6. PERIPHERAL DATA INPUT LATCHING TIMING

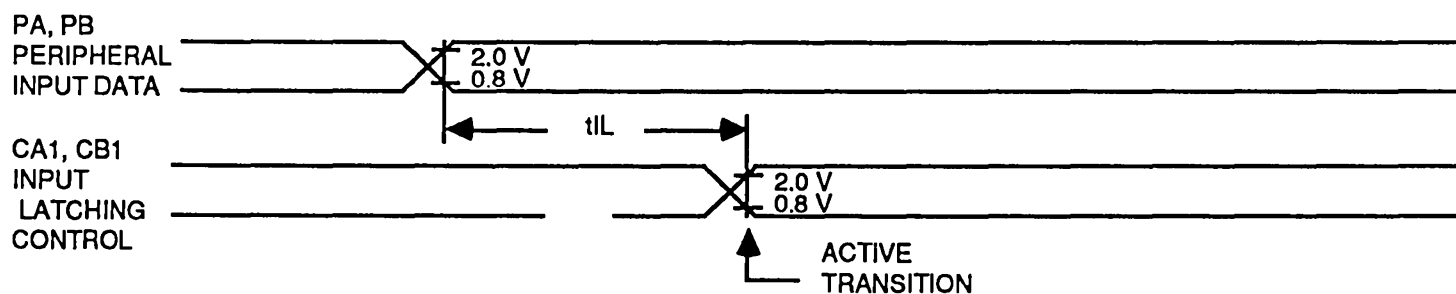


FIGURE 7. TIMING FOR SHIFT OUT WITH INTERNAL OR EXTERNAL SHIFT CLOCKING

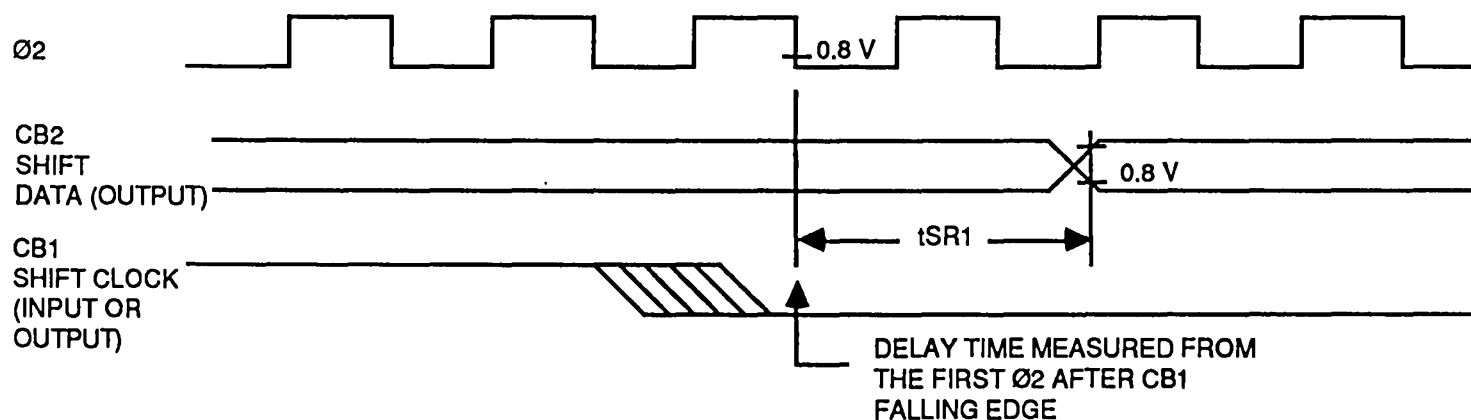




FIGURE 8. TIMING FOR SHIFT IN WITH INTERNAL OR EXTERNAL SHIFT CLOCKING (VL6522 AND VL65C22)

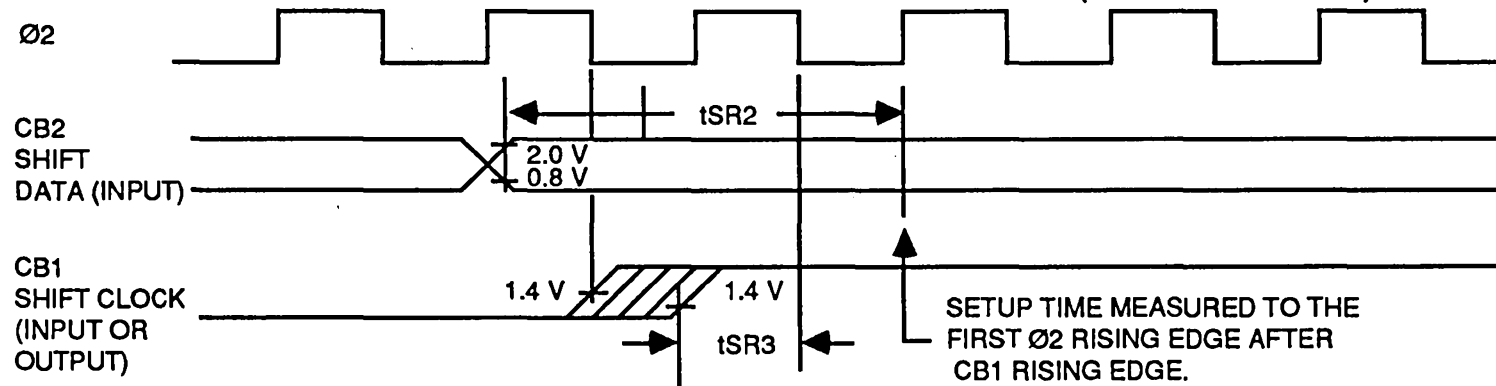


FIGURE 8A. TIMING FOR SHIFT IN WITH INTERNAL OR EXTERNAL SHIFT CLOCKING (VL65C22V)

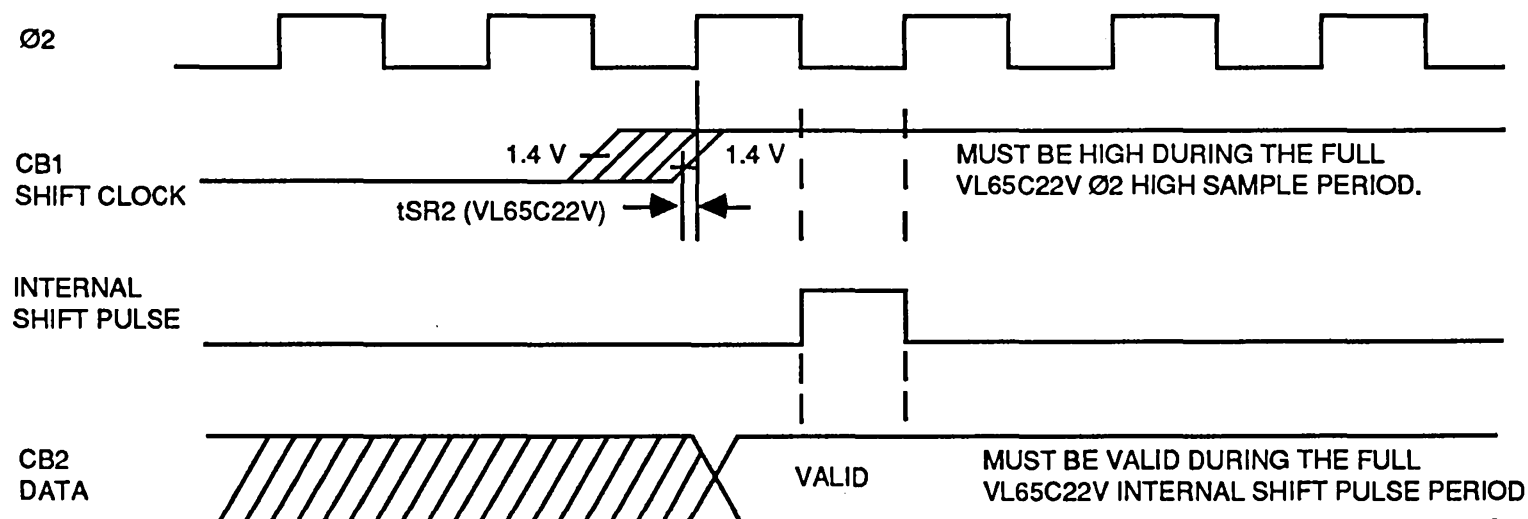


FIGURE 9. EXTERNAL SHIFT CLOCK TIMING

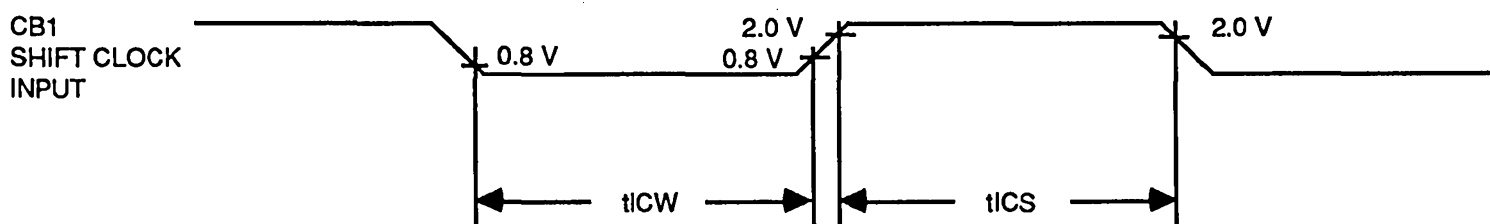


FIGURE 10. PULSE COUNT INPUT TIMING

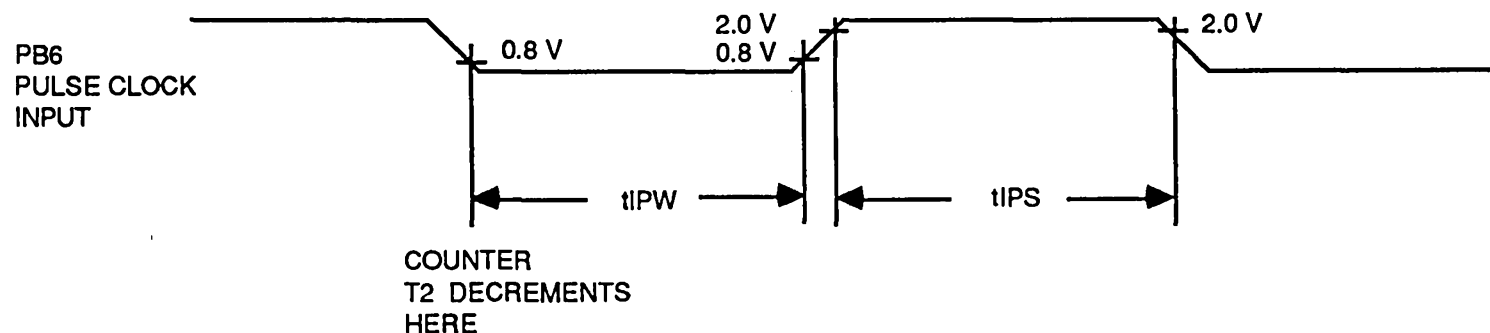


TABLE 2. REGISTER SELECT

Register Number	RS Coding				Register Designation	Register/Description	
	RS3	RS2	RS1	RS0		Write (R/-W=0)	Read (R/-W=1)
0	0	0	0	0	ORB / IRB	Output Register B	Input Register B
1	0	0	0	1	ORA / IRA	Output Register A	Input Register A
2	0	0	1	0	DDRB	Data Direction Register B	
3	0	0	1	1	DDRA	Data Direction Register A	
4	0	1	0	0	T1C - L	T1 Low-Order Latches	T1 Low-Order Counter
5	0	1	0	1	T1C - H	T1 High-Order Counter	
6	0	1	1	0	T1L - L	T1 Low-Order Latches	
7	0	1	1	1	T1L - H	T1 High-Order Latches	
8	1	0	0	0	T2C - L	T2 Low-Order Latches	T2 Low-Order Counter
9	1	0	0	1	T2C - H	T2 High-Order Counter	
10	1	0	1	0	SR	Shift Register	
11	1	0	1	1	ACR	Auxiliary Control Register	
12	1	1	0	0	PCR	Peripheral Control Register	
13	1	1	0	1	IFR	Interrupt Flag Register	
14	1	1	1	0	IER	InterruptEnable Register	
15	1	1	1	1	ORA / IRA	Output Register A *	Input Register A *

Notes: 1. * - Same as Register 1, except no handshake

2. On the VL65C22V and VL65C22, the Register Select may be decoded only while -CS2 is low.

TABLE 3. READ TIMING

Symbol	Parameter	VL6522-01		VL6522-02		VL65C22(V)-02		VL65C22(V)-04		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
tCYC	Cycle Time	1	10	0.5	10	0.5	10	0.25	10	μs
tACR	Address Setup Time	180	-	90	-	90	-	45	-	ns
tCAR	Address Hold Time	0	-	0	-	0	-	0	-	ns
tPCR	Peripheral Data Setup Time	300	-	150	-	150	-	75	-	ns
tCDR	Data Bus Delay Time	-	365	-	190	-	190	-	90	ns
tHR	Data Bus Hold Time	10	-	10	-	10	-	10	-	ns

TABLE 4. WRITE TIMING

Symbol	Parameter	VL6522-01		VL6522-02		VL65C22(V)-02		VL65C22(V)-04		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
tCYC	Cycle Time	1	10	0.5	10	0.5	10	0.25	10	μs
tC	Ø2 Pulse Width	470	-	240	-	240	-	120	-	ns
tACW	Address Setup Time	180	-	90	-	90	-	45	-	ns
tCAW	Address Hold Time	0	-	0	-	0	-	0	-	ns
tWCW	R/-W Setup Time	180	-	90	-	90	-	45	-	ns
tCWW	R/-W Hold Time	0	-	0	-	0	-	0	-	ns
tDCW	Data Bus Setup Time	200	-	90	-	90	-	45	-	ns
tHW	Data Bus Hold Time	10	-	10	-	10	-	10	-	ns
tCPW	Peripheral Data Delay Time	-	1.0	-	0.5	-	0.5	-	0.25	μs
tCMOS	Peripheral Data Delay Time to CMOS Levels	-	2.0	-	1.0	-	1.0	-	0.5	μs

Note: tRISE, tFALL = 10 to 30 ns.

FIGURE 11. READ TIMING

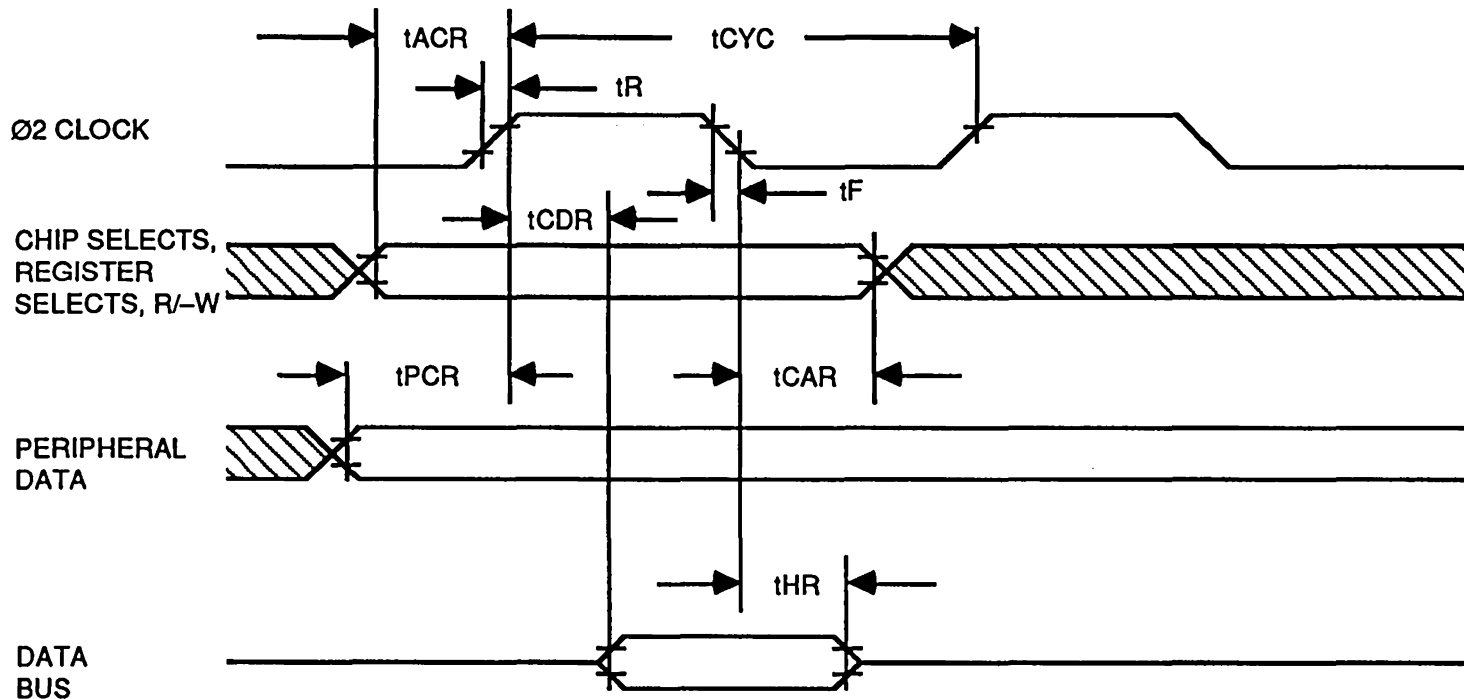


FIGURE 12. WRITE TIMING

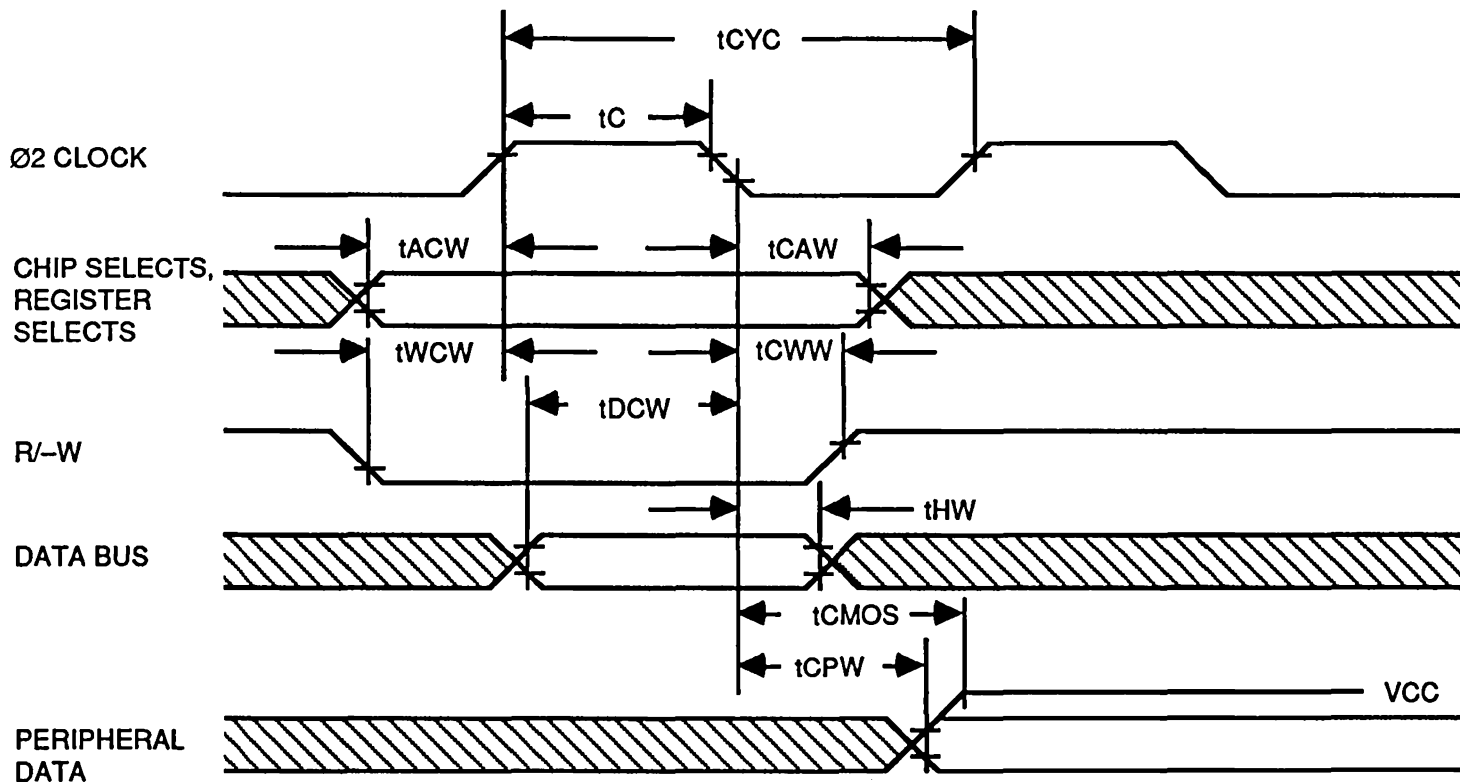
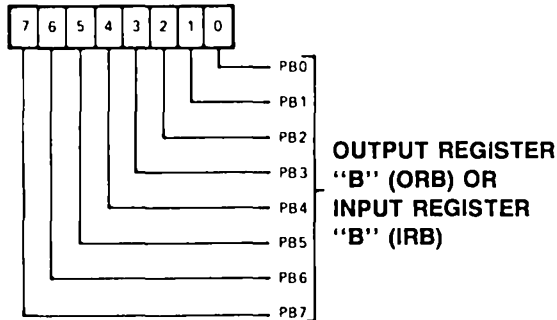
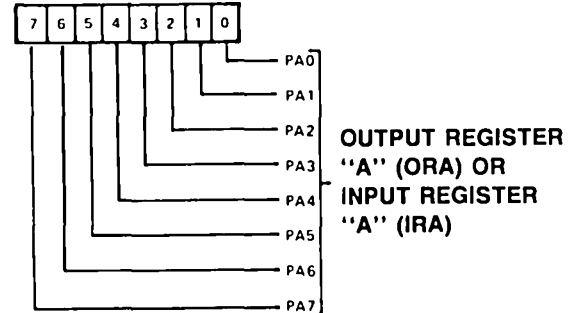


FIGURE 13. REGISTER 0, ORB/IRB



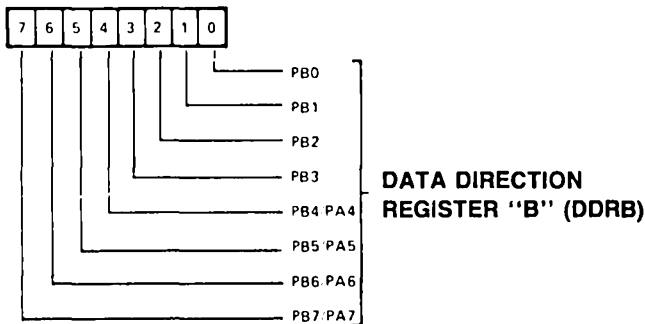
PIN DATA DIRECTION SELECTION	WRITE	READ
DDRB = "1" (OUTPUT)	MPU WRITES OUTPUT LEVEL (ORB)	MPU READS OUTPUT REGISTER BIT IN ORB. PIN LEVEL HAS NO AFFECT
DDRB = "0" (INPUT) (INPUT LATCHING DISABLED)	MPU WRITES INTO ORB, BUT NO EFFECT ON PIN LEVEL, UNTIL DDRB CHANGED	MPU READS INPUT LEVEL ON PB PIN
DDRB = "0" (INPUT) (INPUT LATCHING ENABLED)		MPU READS IRB BIT, WHICH IS THE LEVEL OF THE PB PIN AT THE TIME OF THE LAST CB1 ACTIVE TRANSITION

FIGURE 14. REGISTER 1, ORA/IRA



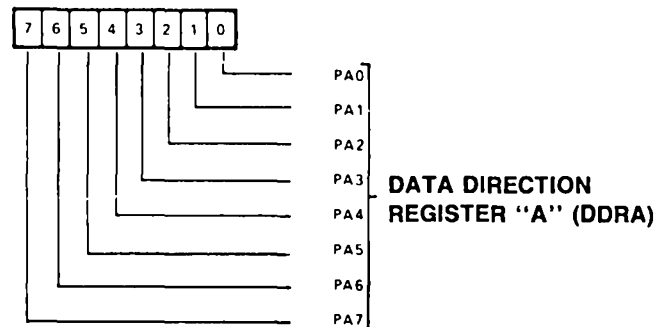
PIN DATA DIRECTION SELECTION	WRITE	READ
DDRA = "1" (OUTPUT) (INPUT LATCHING DISABLED)	MPU WRITES OUTPUT LEVEL (ORA)	MPU READS LEVEL ON PA PIN
DDRA = "1" (OUTPUT) (INPUT LATCHING ENABLED)		MPU READS IRA BIT WHICH IS THE LEVEL OF THE PA PIN AT THE TIME OF THE LAST CA1 ACTIVE TRANSITION
DDRA = "0" (INPUT) (INPUT LATCHING DISABLED)	MPU WRITES INTO ORA, BUT NO EFFECT ON PIN LEVEL, UNTIL DDRA CHANGED	MPU READS LEVEL ON PA PIN
DDRA = "0" (INPUT) (INPUT LATCHING ENABLED)		MPU READS IRA BIT, WHICH IS THE LEVEL OF THE PA PIN AT THE TIME OF THE LAST CA1 ACTIVE TRANSITION

FIGURE 15. REGISTER 2, DDRB



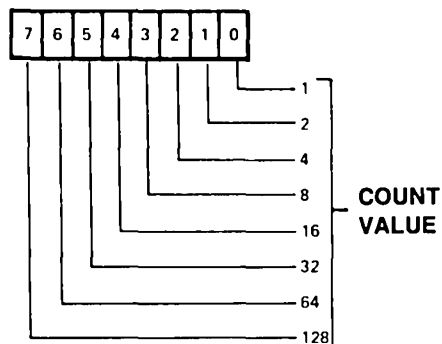
"0" ASSOCIATED PB PIN IS AN INPUT (HIGH IMPEDANCE)
 "1" ASSOCIATED PB PIN IS AN OUTPUT WHOSE LEVEL IS DETERMINED BY ORB REGISTER BIT

FIGURE 16. REGISTER 3, DDRA



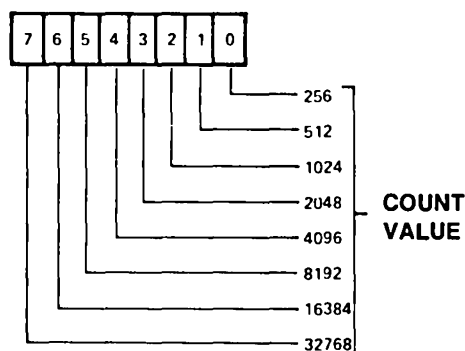
"0" ASSOCIATED PA PIN IS AN INPUT (HIGH IMPEDANCE)
 "1" ASSOCIATED PA PIN IS AN OUTPUT WHOSE LEVEL IS DETERMINED BY ORA REGISTER BIT

FIGURE 17. REGISTER 4, TIMER 1 LOW-ORDER COUNTER



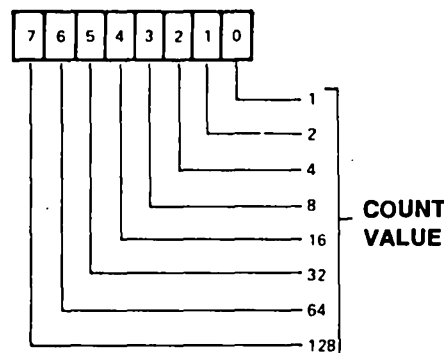
WRITE - 8 BITS LOADED INTO T1 LOW-ORDER LATCHES. LATCH CONTENTS ARE TRANSFERRED INTO LOW-ORDER COUNTER AT THE TIME THE HIGH-ORDER COUNTER IS LOADED (REG 5).
 READ - 8 BITS FROM T1 LOW-ORDER COUNTER TRANSFERRED TO MPU. IN ADDITION, T1 INTERRUPT FLAG IS RESET (BIT 6 IN INTERRUPT FLAG REGISTER).

FIGURE 18. REGISTER 5, TIMER 1 HIGH-ORDER COUNTER



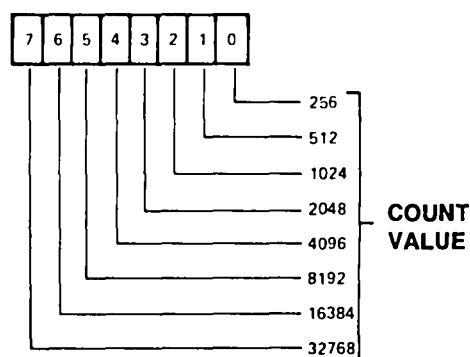
WRITE - 8 BITS LOADED INTO T1 HIGH-ORDER LATCHES. ALSO, AT THIS TIME BOTH HIGH- AND LOW-ORDER LATCHES TRANSFERRED INTO T1 COUNTER. T1 INTERRUPT FLAG ALSO IS RESET.
READ - 8 BITS FROM T1 HIGH-ORDER COUNTER TRANSFERRED TO MPU.

FIGURE 19. REGISTER 6, TIMER 1 LOW-ORDER LATCH



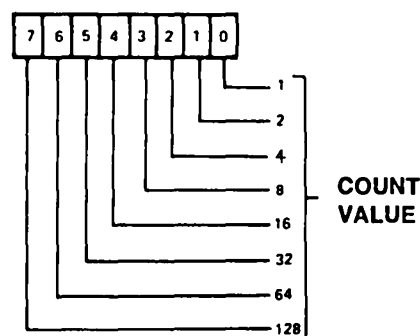
WRITE - 8 BITS LOADED INTO T1 LOW-ORDER LATCHES. THIS OPERATION IS NO DIFFERENT THAN A WRITE INTO REG 4.
READ - 8 BITS FROM T1 LOW-ORDER LATCHES TRANSFERRED TO MPU. UNLIKE REG 4 OPERATION, THIS DOES NOT CAUSE RESET OF T1 INTERRUPT FLAG

FIGURE 20. REGISTER 7, TIMER 1 HIGH-ORDER LATCH



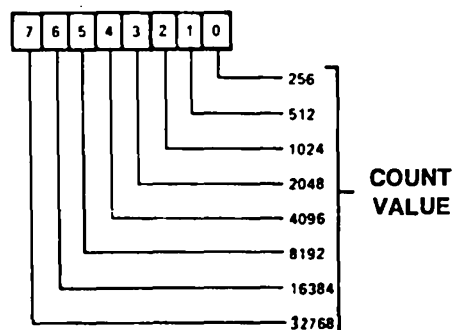
WRITE - 8 BITS LOADED INTO T1 HIGH-ORDER LATCHES. UNLIKE REG 4 OPERATION NO LATCH-TO-COUNTER TRANSFERS TAKE PLACE.
READ - 8 BITS FROM T1 HIGH-ORDER LATCHES TRANSFERRED TO MPU.

FIGURE 21. REGISTER 8, TIMER 2 LOW-ORDER LATCH/COUNTER



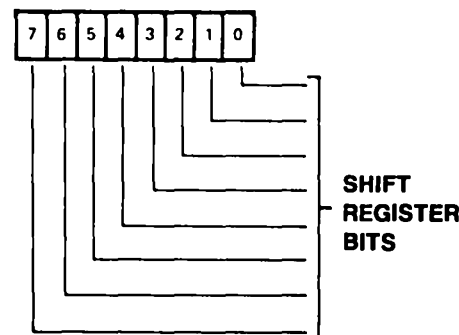
WRITE - 8 BITS LOADED INTO T2 LOW-ORDER LATCH
READ - 8 BITS FROM T2 LOW-ORDER COUNTER TRANSFERRED TO MPU. T2 INTERRUPT FLAG IS RESET.

FIGURE 22. REGISTER 9, TIMER 2 HIGH-ORDER LATCH/COUNTER



WRITE - 8 BITS LOADED INTO T2 HIGH ORDER COUNTER. ALSO, LOW ORDER LATCH TRANSFERRED TO LOW ORDER COUNTER. IN ADDITION, T2 INTERRUPT FLAG IS RESET
READ - 8 BITS FROM T2 HIGH ORDER COUNTER TRANSFERRED TO MPU

FIGURE 23. REGISTER 10, SHIFT REGISTER



NOTES:
1. WHEN SHIFTING OUT, BIT 7 IS THE FIRST BIT OUT AND SIMULTANEOUSLY IS ROTATED BACK INTO BIT 0.
2. WHEN SHIFTING IN, BITS INITIALLY ENTER BIT 0 AND ARE SHIFTED TOWARDS BIT 7.

FIGURE 24. REGISTER 11A, AUXILIARY CONTROL REGISTER

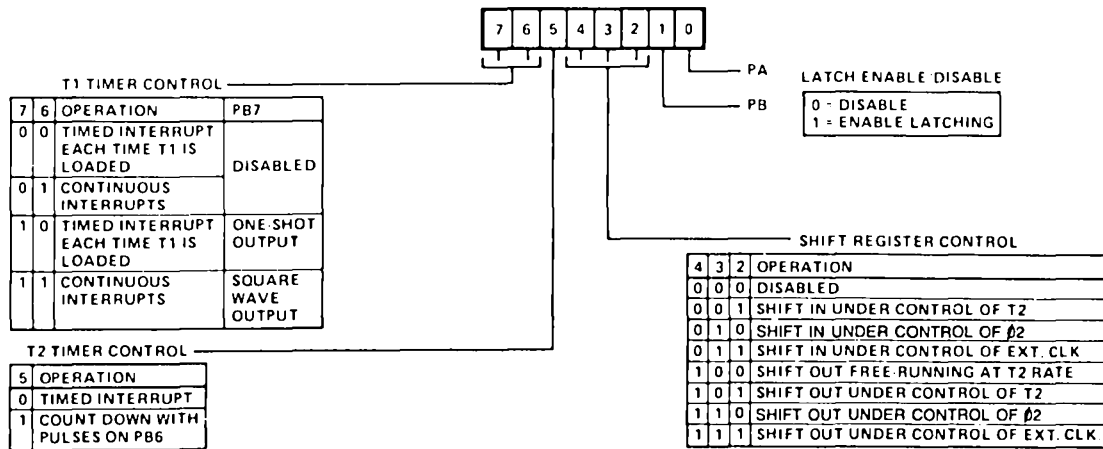


FIGURE 25. REGISTER 11B, AUXILIARY CONTROL REGISTER

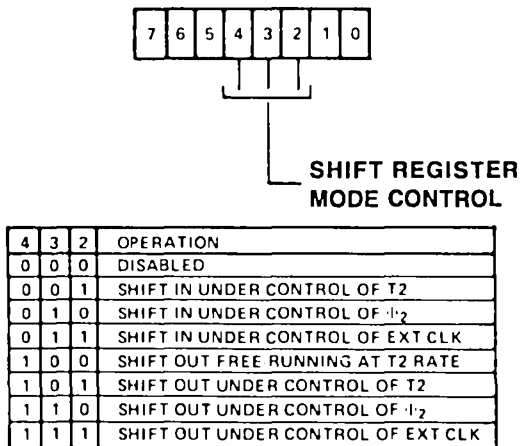
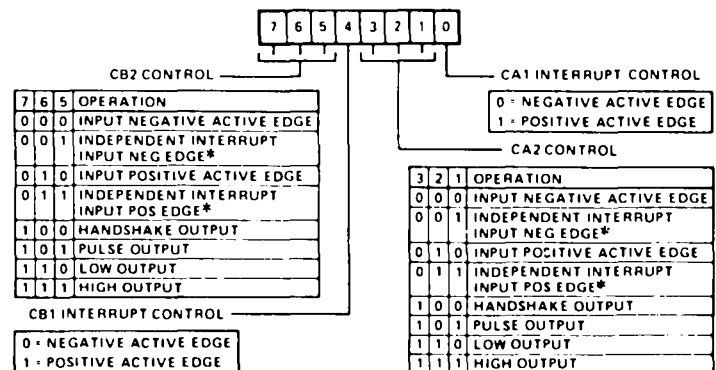
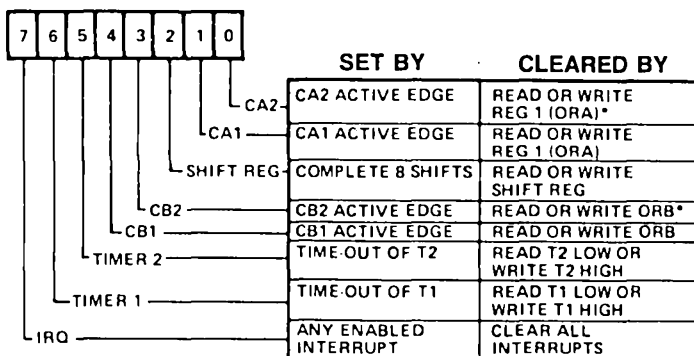
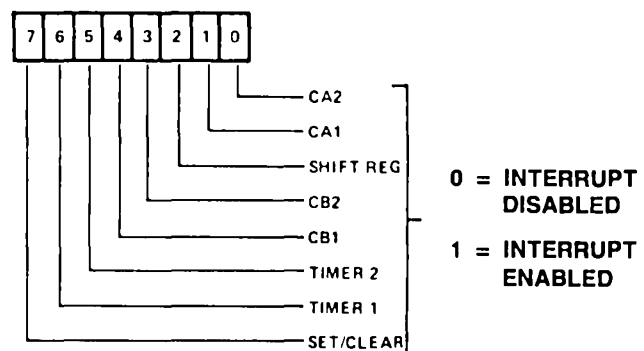


FIGURE 26. REGISTER 12, PERIPHERAL CONTROL REGISTER

**FIGURE 27. REGISTER 13, INTERRUPT FLAG REGISTER**

- IF THE CA2/CB2 CONTROL IN THE PCR IS SELECTED AS "INDEPENDENT" INTERRUPT INPUT, THEN READING OR WRITING THE OUTPUT REGISTER ORA/ORB WILL NOT CLEAR THE FLAG BIT. INSTEAD, THE BIT MUST BE CLEARED BY WRITING INTO THE IFR, AS DESCRIBED PREVIOUSLY.

FIGURE 28. REGISTER 14, INTERRUPT ENABLE REGISTER



NOTES:

- NOTES:
- 1 IF BIT 7 IS A "0", THEN EACH "1" IN BITS 0 - 6 DISABLES THE CORRESPONDING INTERRUPT.
 - 2 IF BIT 7 IS A "1", THEN EACH "1" IN BITS 0 - 6 ENABLES THE CORRESPONDING INTERRUPT.
 - 3 IF A READ OF THIS REGISTER IS DONE, BIT 7 WILL BE "1" AND ALL OTHER BITS WILL REFLECT THEIR ENABLE/DISABLE STATE.

ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	–10 to +80°C
Storage Temperature	–65 to +150°C
Supply Voltage to Ground Potential	–0.5 to +7.0 V
Applied Voltage	–0.5 to +7.0 V
Power Dissipation	750 mW

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or

any other conditions above those indicated on the operational sections of this specification is not implied and exposure to conditions for extended periods may affect device reliability.

DC CHARACTERISTICS (VL6522): VCC = 5 V ±5%, TA = 0°C to 70°C

Symbol	Parameter		Min.	Typ	Max.	Unit	Conditions
VIH	Input High Voltage		2.4		VCC	V	
VIL	Input Low Voltage		–0.3		0.4	V	
IIN	Input Leakage Current R/–W, –RES, RS3 – RS0, –CS2, CS1, CA1, Ø2		-		±2.5	µA	VIN = 0 V to 5.0 V VCC = 0 V
ITSI	Input Leakage Current for Three-State Off D7 – D0		-		±10	µA	VIN = 0.4 V to 2.4 V VCC = 5.25 V
IIH	Input High Current PA7-PA0, CA2, PB7-PB0, CB1, CB2		–100		-	µA	VIN = 2.4 V
IIL	Input Low Current PA7-PA0, CA2, PB7-PB0, CB1, CB2		-		–1.8	mA	VIL = 0.4 V
VOH	Output High Voltage PA7-PA0, CA2, PB7-PB0, CB1, CB2		2.4		-	V	VCC = 4.75 V ILOAD = –100 µA
VOL	Output Low Voltage		-		0.4	V	VCC = 4.75 V ILOAD = 3.2 mA
IOH	Output High Current (Sourcing)	PA7-PA0, PB7-PB0 (TTL drive), D7-D0	–100		-	µA	VOH = 2.4 V
		PB7-PB0 (other drive, e.g., Darlington)	–1.0		-	mA	VOH = 1.5 V
IOL	Output Low Current (Sinking)		1.6		-	mA	VOL = 0.4 V
IOFF	Output Leakage Current (Off State) –IRQ		-		10	µA	
PD	Power Dissipation		-		700	mW	

**DC CHARACTERISTICS (VL65C22 AND VL65C22V): VCC = 5 V \pm 5%, TA = 0°C to 70°C**

Symbol	Parameter		Min.	Typ	Max.	Unit	Conditions
VIH	Input High Voltage		2.4		VCC	V	
VIL	Input Low Voltage		-0.3		0.4	V	
IIN	Input Leakage Current R/-W, -RES, RS3 - RS0, -CS2, CS1, CA1, Ø2		-		± 1.0	μ A	VIN = 0 V to 5.0 V VCC = 0 V
ITSI	Input Leakage Current for Three-State Off D7 - D0		-		± 10	μ A	VIN = 0.4 V to 2.4 V VCC = 5.25 V
IiH	Input High Current PA7-PA0, CA2, PB7-PB0, CB1, CB2		-200		-	μ A	VIN = 2.4 V
IiL	Input Low Current PA7-PA0, CA2, PB7-PB0, CB1, CB2		-		-1.6	mA	VIL = 0.4 V
VOH	Output High Voltage PA7-PA0, CA2, PB7-PB0, CB1, CB2		2.4		-	V	VCC = 4.75 V ILOAD = -100 μ A
VOL	Output Low Voltage		-		0.4	V	VCC = 4.75 V ILOAD = 3.2 mA
IOH	Output High Current (Sourcing)	PA7-PA0, PB7-PB0 (TTL drive), D7-D0	-200		-	μ A	VOH = 2.4 V
		PB7-PB0 (other drive, e.g., Darlington)	-3.0		-	mA	VOH = 1.5 V
IOL	Output Low Current (Sinking)		1.6		-	mA	VOL = 0.4 V
IOFF	Output Leakage Current (Off State) -IRQ		-		10	μ A	
ICC	Power Supply Current		-		2.5	mA/MHz	

CAPACITANCE: TA = 25°C, f = 1 MHz

Symbol	Parameter		Min.	Typ	Max.	Unit	Conditions
CI	Input Capacitance	R/-W, -RES, RS3-RS0, CS2,-CS1, D7-D0, CA1, CA2, PA7-PA0, PB7-PB0	-		7.0	pF	VCC = 5.0 V VIN = 0 V
		CB1, CB2	-		10	pF	
		Ø2 Input	-		20	pF	
COUT	Output Capacitance		-		10	pF	

CMOS 16-BIT MICROPROCESSOR
FEATURES

- Advanced CMOS design for low power consumption and increased noise immunity
- Single 5 V power supply
- Emulation mode allows complete hardware and software compatibility with 6502 designs
- 24-bit address bus allows access to 16M bytes of memory space
- Full 16-bit ALU, Accumulator, Stack Pointer, and Index Registers
- Valid data address (VDA) and valid program address (VPA) output allows dual cache and cycle steal DMA implementation
- Vector pull (VP) output indicates when interrupt vectors are being addressed
- VP may be used to implement vectored interrupt design
- ABORT input and associated vector supports interrupting any instruction without modifying internal registers
- Separate program and data bank

registers allow program segmentation

- New Direct Register allows "zero page" addressing anywhere in first 64k bytes of memory
- 24 addressing modes: 13 original 6502 modes plus 11 new addressing modes, with 91 instructions using 255 opcodes
- New Wait for Interrupt (WAI) and Stop the Clock (STP) instructions further reduce power consumption, decrease interrupt latency and allow synchronization with external events
- New Coprocessor (COP) instruction with associated vector supports coprocessor configurations (e.g., floating point processors)

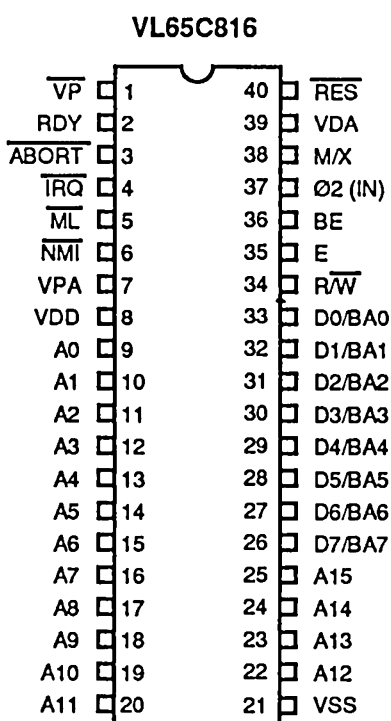
advantages of CMOS technology, including increased noise immunity, higher reliability, and greatly reduced power requirements. A software switch determines whether the processor is in the 8-bit "emulation" mode or in the "native" mode, thus allowing existing systems to use the expanded features.

The Accumulator, ALU, X and Y Index registers, and Stack Pointer Register have all been extended to 16 bits. A new 16-bit Direct Page Register augments the direct page addressing mode (formerly zero page addressing). Separate Program Bank and Data Bank Registers allow 24-bit memory addressing.

Four new signals provide the system designer with many options. The ABORT input can interrupt the currently executing instruction without modifying internal registers. Valid data address (VDA) and Valid program address (VPA) outputs facilitate dual cache memory by indicating whether a data segment or program segment is accessed. Modifying a vector is made easy by monitoring the vector pull (VP) output.

DESCRIPTION

The VL65C816 is a CMOS 16-bit microprocessor featuring total software compatibility with its 8-bit NMOS and CMOS 6500-series predecessors. The VL65C816 extends addressing to a full 16 megabytes. The device offers many

PIN DIAGRAMS

ORDER INFORMATION

Part Number	Clock Frequency	Package
VL65C816-02PC	2 MHz	Plastic DIP
VL65C816-02CC		Ceramic DIP
VL65C816-04PC	4 MHz	Plastic DIP
VL65C816-04CC		Ceramic DIP
VL65C816-06PC	6 MHz	Plastic DIP
VL65C816-06CC		Ceramic DIP
VL65C816-08PC	8 MHz	Plastic DIP
VL65C816-08CC		Ceramic DIP

Note: Operating temperature range is 0°C to +70°C.



BLOCK DIAGRAM

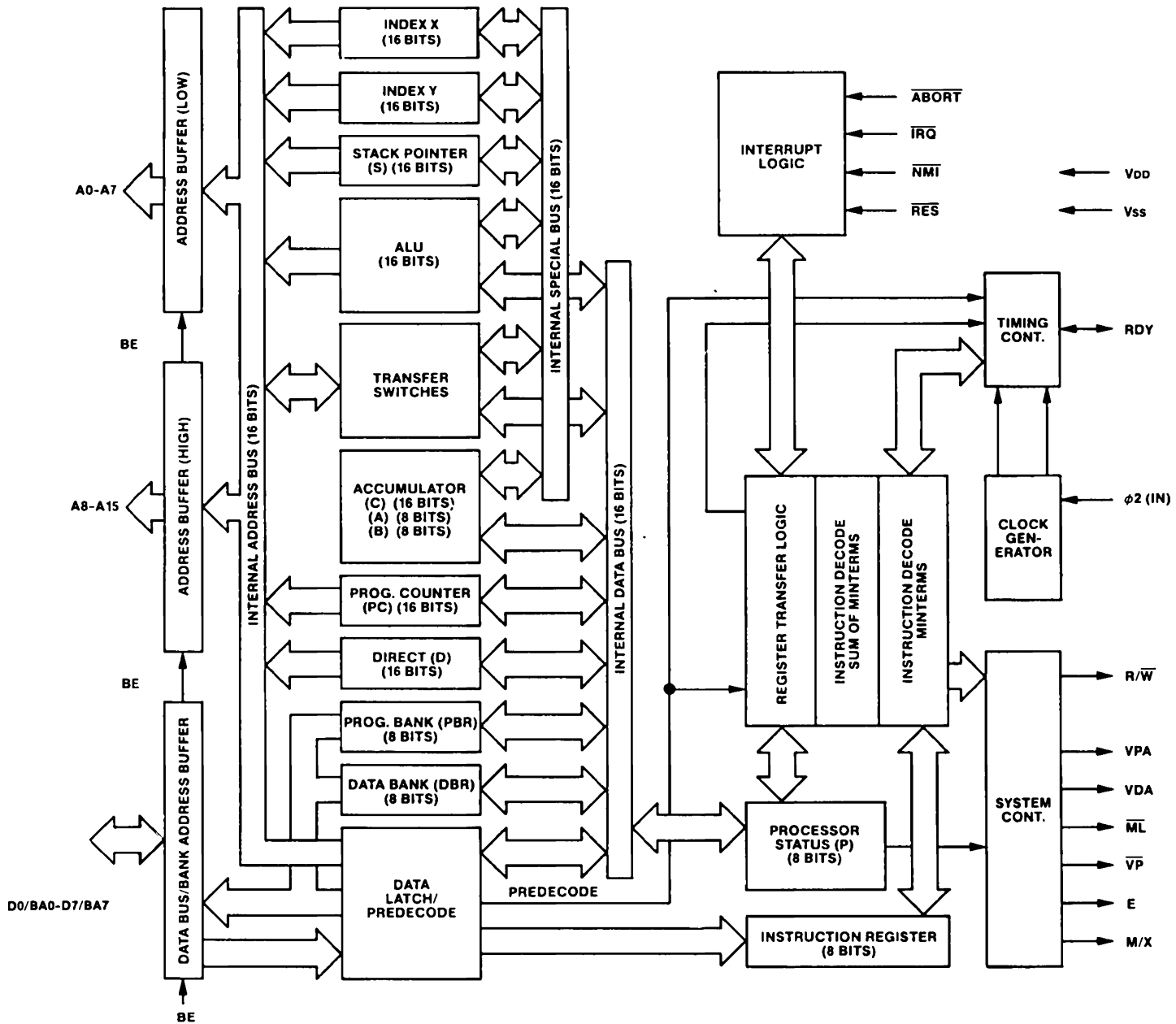


FIGURE 1. STATUS REGISTER

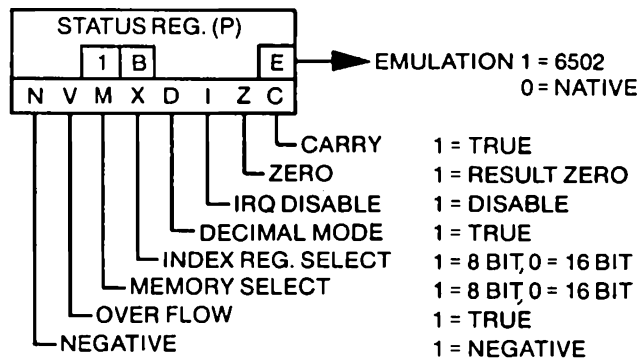


FIGURE 2. PROGRAMMING MODEL

8 BITS	8 BITS	8 BITS
Data Bank Reg. (DBR)	X Register Hi (XH)	X Register Low (XL)
Data Bank Reg. (DBR)	Y Register Hi (YH)	Y Register Low (YL)
00	Stack Register Hi (SH)	Stack Reg. Low (SL)
6502 Registers	Accumulator (B)	Accumulator (A)
Program Bank Reg. (PBR)	Program (PCH)	Counter (PCL)
00	Direct Reg. Hi (DH)	Direct Reg. Low (DL)

SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Description
$\overline{\text{ABORT}}$	3	Abort – The $\overline{\text{ABORT}}$ input is used to abort instructions (usually due to an Address Bus condition). A negative transition will inhibit modification of any internal register during the current instruction. Upon completion of this instruction, an interrupt sequence is initiated. The location of the aborted opcode is stored as the return address in stack memory. The Abort vector address is 00FFF8, 9 (Emulation Mode) or 00FFE8, 9 (Native mode). Since $\overline{\text{ABORT}}$ is an edge-sensitive input, an Abort occurs whenever there is a negative pulse (or level) on the $\overline{\text{ABORT}}$ line during a phase 2 clock.
A0-A15	9-12, 22-25	Address Bus – These 16 output lines form the Address Bus for memory and I/O exchange on the Data Bus. The address lines may be set to the high-impedance state by the Bus Enable (BE) signal.
BE	36	Bus Enable – The Bus Enable input signal allows external control of the Address and Data Buffers, as well as the R/W signal. With Bus Enable high, the R/W and Address Buffers are active. The Data/Address Buffers are active during the first half of every cycle and the second half of a write cycle. When BE is low, these buffers are disabled. Bus Enable is an asynchronous signal.
D0/BA0-D7/BA7	33-26	Data/Address Bus – These eight lines multiplex address bits BA0-BA7 with the data value. The address is present during the first half of a memory cycle, and the data value is read or written during the second half of the memory cycle. Two memory cycles are required to transfer 16-bit values. These lines may be set to the high impedance state by the BE signal.
E	35	Emulation Status – The Emulation Status output reflects the state of the Emulation (E) Mode flag in the Processor Status (P) Register. This signal may be thought of as an op code extension and used for memory and system management.
$\overline{\text{IRQ}}$	4	Interrupt Request – The Interrupt Request input signal is used to request that an interrupt sequence be initiated. When the IRQ Disable (I) Flag is cleared, a low input logic level initiates an interrupt sequence after the current instruction is completed. The Wait for Interrupt (WAI) instruction may be executed to ensure the interrupt is recognized immediately. The Interrupt Request vector address is 00FFFE,F (Emulation Mode) or 00FFEE,F (Native mode). Since $\overline{\text{IRQ}}$ is a level-sensitive input, an interrupt occurs if the interrupt source was not cleared since the last interrupt. Also, no interrupt occurs if the interrupt source is cleared prior to interrupt recognition.
$\overline{\text{ML}}$	5	Memory Lock – The Memory Lock output may be used to ensure the integrity of Read-Modify-Write instructions in a multiprocessor system. Memory Lock indicates the need to defer arbitration of the next bus cycle. Memory Lock is low during the last three or five cycles of ASL, DEC, INC, LSR, ROL, ROR, TRB, and TSB memory referencing instructions, depending on the state of the M flag.
M/X	38	Memory/Index Select Status – This multiplexed output reflects the state of the Accumulator (M) and Index (X) Select Flags (bits 5 and 4 of the Processor Status (P) Register). Flag M is valid during the Phase 2 clock negative transition and Flag X is valid during the Phase 2 clock positive transition. These bits may be thought of as opcode extensions and may be used for memory and system management.
$\overline{\text{NMI}}$	6	Non-Maskable Interrupt – A negative transition on the $\overline{\text{NMI}}$ input initiates an interrupt sequence. A high-to-low transition initiates an interrupt sequence after the current instruction is completed. The Wait for Interrupt (WAI) instruction may be executed to ensure that the interrupt will be recognized immediately. The Non-Maskable Interrupt vector address is 00FFFA,B (Emulation Mode) or 00FFEA,B (Native Mode). Since $\overline{\text{NMI}}$ is an edge-sensitive input, an interrupt occurs if there is a negative transition while servicing a previous interrupt. Also, no interrupt occurs if $\overline{\text{NMI}}$ remains low.
$\phi 2$ (IN)	37	Phase 2 In – This is the system clock input to the microprocessor internal clock generator [equivalent to $\phi 0$ (IN) on the 6502]. During the low power Standby Mode, $\phi 2$ (IN) should be held in the high state to preserve the contents of internal registers.

SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Description
$\overline{R/W}$	34	Read/Write – When the $\overline{R/W}$ output signal is in the high state, the microprocessor is reading data from memory or I/O. When in the low state, the Data Bus contains valid data from the microprocessor that is to be stored at the addressed memory location. The $\overline{R/W}$ signal may be set to the high impedance state by Bus Enable (BE).
RDY	2	Ready – This bidirectional signal indicates that a Wait for Interrupt (WAI) instruction has been executed allowing the user to halt operation of the microprocessor. A low input logic level will halt the microprocessor in its current state. Returning RDY to the active high state allows the microprocessor to continue following the next Phase 2 In clock negative transition. The RDY signal is internally pulled low following the execution of a Wait for Interrupt (WAI) instruction, and then returned to the high state when a RES, ABORT, NMI, or IRQ external interrupt is provided. This feature may be used to eliminate interrupt latency by placing the WAI instruction at the beginning of the IRQ servicing routine. If the IRQ Disable Flag has been set, the next instruction is executed when the IRQ occurs. The processor does not stop after a WAI instruction if RDY has been forced to a high state. The Stop (STP) instruction has no effect on RDY.
\overline{RES}	40	Reset –The Reset input is used to initialize the microprocessor and start program execution. The Reset input buffer has hysteresis such that a simple R-C timing circuit may be used with the internal pull-up device. The \overline{RES} signal must be held low for a least two clock cycles after VDD reaches operating voltage. Ready (RDY) has no effect while \overline{RES} is being held low. During this Reset conditioning period, the following processor initialization takes place:

Registers

D = 0000	SH = 01
DBR = 00	XH = 00
PBR = 00	YH = 00

	N	V	M	X	D	I	Z	C/E
P =	*	*	1	1	0	1	*	*/1

* = Not Initialized

STP and WAI instructions are cleared.

Signals

E = 1	VDA = 0
M/X = 1	VP = 1
$\overline{R/W}$ = 1	VPA = 0
SYNC = 0	

When Reset is brought high, an interrupt sequence is initiated $\overline{R/W}$ remains in the high state during the stack address cycles and the Reset vector address is 00FFFC,D.

VDA, VPA	39,7	Valid Data Address and Valid Program Address – These two output signals indicate the type of memory being accessed by the address bus. The following coding applies:
----------	------	--

VDA	VPA	
0	0	Internal operation - Address and Data Bus available.
0	1	Valid program address - May be used for program cache control.
1	0	Valid data address - May be used for data cache control.
1	1	Op code fetch - May be used for program cache control and single step control.

\overline{VP}	1	Vector Pull – The Vector Pull output indicates that a vector location is being addressed during an interrupt sequence. \overline{VP} is low during the last two interrupt sequence cycles, during which time the processor reads the interrupt vector. The \overline{VP} signal may be used to select and prioritize interrupts from several sources by modifying the vector addresses.
VDD	8	VDD is the 5 V supply voltage.
VSS	21	VSS is system logic ground.

FUNCTIONAL DESCRIPTION

The VL65C816 provides the design engineer with upward mobility and software compatibility in applications in which a 16-bit system configuration is desired. The VL65C816 16-bit hardware configuration, coupled with current software, allows a wide selection of system applications. In the Emulation Mode, the VL65C816 offers many advantages, including full software compatibility with 6502 coding. In addition, the powerful VL65C816 instruction set and addressing modes make it an excellent choice for new 16-bit designs.

The internal organization of the VL65C816 can be divided into two parts: 1) the Register Section, and 2) the Control Section. Instructions (or opcodes) obtained from program memory are executed by implementing a series of data transfers within the Register Section. Signals that cause data transfers to be executed are generated within the Control Section. The VL65C816 has a 16-bit internal architecture with an 8-bit external data bus.

INSTRUCTION REGISTER

An opcode enters the processor on the Data Bus and is latched into the Instruction Register during the instruction fetch cycle. This instruction is then decoded, along with timing and interrupt signals, to generate the various Instruction Register control signals.

TIMING CONTROL UNIT (TCU)

The Timing Control Unit keeps track of each instruction cycle as it is executed. The TCU is set to zero each time an instruction fetch is executed, and is advanced at the beginning of each cycle for as many cycles as is required to complete the instruction. Each data transfer between registers depends upon decoding the contents of both the Instruction Register and the Timing Control Unit.

ARITHMETIC LOGIC UNIT (ALU)

All arithmetic and logic operations take place within the 16-bit ALU. In addition to data operations, the ALU also calculates the effective address for relative and indexed addressing modes. The result of a data operation is stored in either memory or an internal register.

Carry, Negative, Overflow and Zero Flags may be updated following the ALU data operation.

INTERNAL REGISTERS (Refer to Figure 2, Programming Model.)

ACCUMULATORS (A, B, C)

The Accumulator is a general purpose register that stores one of the operands, or the result of most arithmetic and logical operations. In the Native Mode ($E=0$), when the Accumulator Select Bit (M) equals zero, the Accumulator is established as 16 bits wide ($A+B=C$). When the Accumulator Select Bit (M) equals one, the Accumulator is eight bits wide (A). In this case, the upper eight bits (B) may be used for temporary storage in conjunction with the Exchange B and A Accumulator (XBA) instruction.

DATA BANK REGISTER (DBR)

During modes of operation, the 8-bit Data Bank Register holds the default bank address for memory transfers. The 24-bit address is composed of the 16-bit instruction effective address and the 8-bit Data Bank address. The register value is multiplexed with the data value and is present on the Data/Address lines during the first half of a data transfer memory cycle for the VL65C816. The Data Bank Register is initialized to zero during Reset.

DIRECT (D)

The 16-bit Direct Register provides an address offset for all instructions using direct addressing. The effective bank zero address is formed by adding the 8-bit instruction operand address to the Direct Register contents. The Direct Register is initialized to zero during Reset.

INDEX (X AND Y)

There are two Index Registers (X and Y), which may be used as general purpose registers or to provide an index value for calculation of the effective address. When executing an instruction with indexed addressing, the microprocessor fetches the opcode and the base address, and then modifies the address by adding the Index Register contents to the address prior to performing the desired operation. Pre- or post-indexing of indirect addresses may be selected.

In the Native Mode ($E=0$), both Index Registers are 16 bits wide if the Index Select Bit (X) equals zero. If the Index Select Bit (X) equals one, both registers are 8 bits wide, and the high byte is forced to zero.

PROCESSOR STATUS (P)

The 8-bit Processor Status Register contains status flags and mode select bits. The Carry (C), Negative (N), Overflow (V), and Zero (Z) status flags serve to report the status of most ALU operations. These status flags are tested by use of Conditional Branch instructions. The Decimal (D), IRQ Disable (I), Memory/Accumulator (M), and Index (X) bits are used as mode select flags. These flags are set by the program to change microprocessor operations.

The Emulation (E) Select and the Break (B) flags are accessible only through the processor Status Register. The Emulation mode select flag is selected by the Exchange Carry and Emulation Bits (XCE) instruction. Table 1, Compatibility Issues, illustrates the features of the Native ($E=0$) and Emulation ($E=1$) Modes. The M and X flags are always equal to one in the Emulation Mode. When an interrupt occurs during the Emulation Mode, the Break Flag is written to stack memory as bit 4 of the Processor Status Register.

PROGRAM BANK REGISTER (PBR)

The 8-bit Program Bank Register holds the bank address for all instruction fetches. The 24-bit address consists of the 16-bit instruction effective address and the 8-bit Program Bank address. The register value is multiplexed with the data value and presented on the Data/Address lines during the first half of a program memory read cycle. The Program Bank Register is initialized to zero during Reset. The PHK instruction pushes the PBR register onto the Stack.

PROGRAM COUNTER (PC)

The 16-bit Program Counter Register provides the addresses that are used to step the microprocessor through sequential program instructions. The register is incremented each time an instruction or operand is fetched from program memory.

STACK POINTER (S)

The Stack Pointer is a 16-bit register that is used to indicate the next available location in the stack memory area. It serves as the effective address in

stack addressing modes as well as subroutine and interrupt processing. The Stack Pointer allows simple implementation of nested subroutines

and multiple-level interrupts. During the Emulation Mode, the Stack Pointer high-order byte (SH) is always equal to one. The bank address for all stack operations is bank zero.

PIN DESCRIPTIONS

Pin	Description
A0-A15	Address Bus
$\overline{\text{ABORT}}$	Abort Input
BE	Bus Enable
$\phi 2$ (IN)	Phase 2 In Clock
$\phi 1$ (OUT)	Phase 1 Out Clock
$\phi 2$ (OUT)	Phase 2 Out Clock
D0-D7	Data Bus
D0/BA0-D7/BA7	Data Bus, Multiplexed
E	Emulation Select
IRQ	Interrupt Request
$\overline{\text{ML}}$	Memory Lock
M/X	Mode Select (Pm or Px)

Pin	Description
NC	No Connection
$\overline{\text{NMI}}$	Non-Maskable Interrupt
RDY	Ready
$\overline{\text{RES}}$	Reset
R/ $\overline{\text{W}}$	Read/Write
$\overline{\text{SO}}$	Set Overflow
SYNC	Synchronize
VDA	Valid Data Address
$\overline{\text{VP}}$	Vector Pull
VPA	Valid Program Address
VDD	Positive Power Supply (+5 Volts)
VSS	Internal Logic Ground

TABLE 1. COMPATIBILITY ISSUES

	65C816	65C02	NMOS 6502
1. S (Stack)	Always page 1 (E = 1), 8 bits 16 bits when (E = 0).	Always page 1, 8 bits	Always page 1, 8 bits
2. X (X Index Register)	Indexed page zero always in page 0 (E = 1), Cross page (E = 0).	Always page 0	Always page 0
3. Y (Y Index Register)	Indexed page zero always in page 0 (E = 1), Cross page (E = 0).	Always page 0	Always page 0
4. A (Accumulator)	8 bits (M = 1), 16 bits (M = 0)	8 bits	8 bits
5. P (Flag Register)	N, V, and Z flags valid in decimal mode. D = 0 after reset or interrupt.	N, V, and Z flags valid in decimal mode. D = 0 after reset and interrupt.	N, V, and Z flags invalid in decimal mode. D = unknown after reset. D not modified after interrupt.
6. Timing			
A. ABS, X ASL, LSR, ROL, ROR With No Page Crossing	7 cycles	6 cycles	7 cycles
B. Jump Indirect Operand = XXFF	5 cycles	6 cycles	5 cycles and invalid page crossing
C. Branch Across Page	4 cycles (E = 1) 3 cycles (E = 0)	4 cycles	4 cycles
D. Decimal Mode	No additional cycle	Add 1 cycle	No additional cycle
7. BRK Vector	00FFFE,F (E = 1) BRK bit = 0 on stack if IRQ, NMI, ABORT. 00FFE6, 7 (E = 0) X = X on Stack always.	FFFE,F BRK bit = 0 on stack if IRQ, NMI.	FFFE,F BRK bit = 0 on stack if IRQ, NMI.
8. Interrupt or Break Bank Address	PBR not pushed (E = 1) RTI PBR not pulled (E = 1) PBR pushed (E = 0) RTI PBR pulled (E = 0)	Not available	Not available
9. Memory Lock (\overline{ML})	\overline{ML} = 0 during Read, Modify and Write cycles.	\overline{ML} = 0 during Modify and Write.	Not available
10. Indexed Across Page Boundary (d),y; a,x; a,y	Extra read of invalid address.	Extra read of last instruction fetch.	Extra read of invalid address.
11. RDY Pulled During Write Cycle.	Processor stops	Processor stops	Ignored
12. WAI and STP Instructions.	Available	Available	Not available
13. Unused OP Codes	One reserved OP Code specified as WDM will be used in future systems. The 65C816 performs a no-operation.	No operation	Unknown and some "hang up" processor.
14. Bank Address Handling	PBR = 00 after reset or interrupts.	Not available	Not available
15. R/W During Read-Modify- Write Instructions	E = 1, R/W = 0 during Modify and Write cycles. E = 0, R/W = 0 only during Write cycle.	R/W = 0 only during Write cycle	R/W = 0 during Modify and Write cycles.
16. Pin 7	VPA	SYNC	SYNC
17. COP Instruction Signatures 00-7F user defined Signatures 80-FF reserved	Available	Not available	Not available

TABLE 2. INSTRUCTION SET – ALPHABETICAL SEQUENCE

ADC	Add Memory to Accumulator with Carry	PHA	Push Accumulator on Stack
AND	"AND" Memory with Accumulator	PHB	Push Data Bank Register on Stack
ASL	Shift One Bit Left, Memory or Accumulator	PHD	Push Direct Register on Stack
BCC	Branch on Carry Clear (Pc = 0)	PHK	Push Program Bank Register on Stack
BCS	Branch on Carry Set (Pc = 1)	PHP	Push Processor Status on Stack
BEQ	Branch if Equal (Pz = 1)	PHX	Push Index X on Stack
BIT	Bit Test	PHY	Push Index Y on Stack
BMI	Branch if Result Minus (Pn = 1)	PLA	Pull Accumulator from Stack
BNE	Branch if Not Equal (Pz = 0)	PLB	Pull Data Bank Register from Stack
BPL	Branch if Result Plus (Pn = 0)	PLD	Pull Direct Register from Stack
BRA	Branch Always	PLP	Pull Processor Status from Stack
BRK	Force Break	PLX	Pull Index X from Stack
BRL	Branch Always Long	PLY	Pull Index Y from Stack
BVC	Branch on Overflow Clear (Pv = 0)	REP	Reset Status Bits
BVS	Branch on Overflow Set (Pv = 1)	ROL	Rotate One Bit Left (Memory or Accumulator)
CLC	Clear Carry Flag	ROR	Rotate One Bit Right (Memory or Accumulator)
CLD	Clear Decimal Mode	RTI	Return from Interrupt
CLI	Clear Interrupt Disable Bit	RTL	Return from Subroutine Long
CLV	Clear Overflow Flag	RTS	Return from Subroutine
CMP	Compare Memory and Accumulator	SBC	Subtract Memory from Accumulator with Borrow
COP	Coprocessor	SEC	Set Carry Flag
CPX	Compare Memory and Index X	SED	Set Decimal Mode
CPY	Compare Memory and Index Y	SEI	Set Interrupt Disable Status
DEC	Decrement Memory or Accumulator by One	SEP	Set Processor Status Bite
DEX	Decrement Index X by One	STA	Store Accumulator in Memory
DEY	Decrement Index Y by One	STP	Stop the Clock
EOR	"Exclusive OR" Memory with Accumulator	STX	Store Index X in Memory
INC	Increment Memory or Accumulator by One	STY	Store Index Y in Memory
INX	Increment Index X by One	STZ	Store Zero in Memory
INY	Increment Index Y by One	TAX	Transfer Accumulator to Index X
JML	Jump Long	TAY	Transfer Accumulator to Index Y
JMP	Jump to New Location	TCD	Transfer C Accumulator to Direct Register
JSL	Jump Subroutine Long	TCS	Transfer C Accumulator to Stack Pointer Register
JSR	Jump to New Location Saving Return Address	TDC	Transfer Direct Register to C Accumulator
LDA	Load Accumulator with Memory	TRB	Test and Reset Bit
LDX	Load Index X with Memory	TSB	Test and Set Bit
LDY	Load Index Y with Memory	TSC	Transfer Stack Pointer Register to C Accumulator
LSR	Shift One Bit Right (Memory or Accumulator)	TSX	Transfer Stack Pointer Register to Index X
MVN	Block Move Negative	TXA	Transfer Index X to Accumulator
MVP	Block Move Positive	TXS	Transfer Index X to Stack Pointer Register
NOP	No Operation	TXY	Transfer Index X to Index Y
ORA	"OR" Memory with Accumulator	TYA	Transfer Index Y to Accumulator
PEA	Push Effective Absolute Address on Stack (or Push Immediate Data on Stack)	TYX	Transfer Index Y to Index X
PEI	Push Effective Indirect Address on Stack (or Push Direct Data on Stack)	WAI	Wait for Interrupt
PER	Push Effective Program Counter Relative Address on Stack	WDM	Reserved for Future Use
		XBA	Exchange B and A Accumulator
		XCE	Exchange Carry and Emulation Bits

For alternate mnemonics, see Table 7.

TABLE 3. VECTOR LOCATIONS

E = 1		E = 0	
00FFFE,F — <u>IRQ</u> /BRK	Hardware/Software	00FFEE,F — <u>IRQ</u>	Hardware
00FFFC,D — <u>RESET</u>	Hardware	00FFEC,D —(Reserved)	
00FFFA,B — <u>NMI</u>	Hardware	00FFEA,B — <u>NMI</u>	Hardware
00FFF8,9 — <u>ABORT</u>	Hardware	00FFE8,9 — <u>ABORT</u>	Hardware
00FFF6,7 —(Reserved)		00FFE6,7 — <u>BRK</u>	Software
00FFF4,5 — <u>COP</u>	Software	00FFE4,5 — <u>COP</u>	Software

The VP output is low during the two cycles used for vector location access.
When an interrupt is executed, D = 0 and I = 1 in Status Register P.

TABLE 4. OPCODE MATRIX

M S D	LSD																M S D
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
0	BRK s 2 8	ORA (d,x) 2 6	COP s 2 * 8	ORA d,s 2 * 4	TSB d 2 * 5	ORA d 2 3	ASL d 2 5	ORA [d] 2 * 6	PHP s 1 3	ORA # 2 2	ASL A 1 2	PHD s 1 * 4	TSB a 3 * 6	ORA a 3 4	ASL a 3 6	ORA al 4 * 5	0
1	BPL r 2 2	ORA (d),y 2 5	ORA (d) 2 * 5	ORA (d,s),y 2 * 7	TRB d 2 * 5	ORA d,x 2 4	ASL d,x 2 6	ORA [d],y 2 * 6	CLC i 1 2	ORA a,y 3 4	INC A 1 * 2	TCS i 1 * 2	TRB a 3 * 6	ORA a,x 3 4	ASL a,x 3 7	ORA al,x 4 * 5	1
2	JSR a 3 6	AND (d,x) 2 6	JSL al 4 * 8	AND d,s 2 * 4	BIT d 2 3	AND d 2 3	ROL d 2 5	AND [d] 2 * 6	PLP s 1 4	AND # 2 2	ROL A 1 2	PLD s 1 * 5	BIT a 3 4	AND a 3 4	ROL a 3 6	AND al 4 * 5	2
3	BMI r 2 2	AND (d),y 2 5	AND (d) 2 * 5	AND (d,s),y 2 * 7	BIT d,x 2 * 4	AND d,x 2 4	ROL d,x 2 6	AND [d],y 2 * 6	SEC i 1 2	AND a,y 3 4	DEC A 1 * 2	TSC i 1 * 2	BIT a,x 3 * 4	AND a,x 3 4	ROL a,x 3 7	AND al,x 4 * 5	3
4	RTI s 1 7	EOR (d,x) 2 6	WDM 2 * 2	EOR d,s 2 * 4	MVP xyc 3 * 7	EOR d 2 3	LSR d 2 5	EOR [d] 2 * 6	PHA s 1 3	EOR # 2 2	LSR A 1 2	PHK s 1 * 3	JMP a 3 3	EOR a 3 4	LSR a 3 6	EOR al 4 * 5	4
5	BVC r 2 2	EOR (d),y 2 5	EOR (d) 2 * 5	EOR (d,s),y 2 * 7	MVN xyc 3 * 7	EOR d,x 2 4	LSR d,x 2 6	EOR [d],y 2 * 6	CLI i 1 2	EOR a,y 3 4	PHY s 1 * 3	TCD i 1 * 2	JMP al 4 * 4	EOR a,x 3 4	LSR a,x 3 7	EOR al,x 4 * 5	5
6	RTS s 1 6	ADC (d,x) 2 6	PER s 3 * 6	ADC d,s 2 * 4	STZ d 2 * 3	ADC d 2 3	ROR d 2 5	ADC [d] 2 * 6	PLA s 1 4	ADC # 2 2	ROR A 1 2	RTL s 1 * 6	JMP (a) 3 5	ADC a 3 4	ROR a 3 6	ADC al 4 * 5	6
7	BVS r 2 2	ADC (d),y 2 5	ADC (d) 2 * 5	ADC (d,s),y 2 * 7	STZ d,x 2 * 4	ADC d,x 2 4	ROR d,x 2 6	ADC [d],y 2 * 6	SEI i 1 2	ADC a,y 3 4	PLY s 1 * 4	TDC i 1 * 2	JMP (a,x) 3 * 6	ADC a,x 3 4	ROR a,x 3 7	ADC al,x 4 * 5	7
8	BRA r 2 * 2	STA (d,x) 2 6	BRL rl 3 * 3	STA d,s 2 * 4	STY d 2 3	STA d 2 3	STX d 2 3	STA [d] 2 * 6	DEY i 1 2	BIT # 2 * 2	TXA i 1 2	PHB s 1 * 3	STY a 3 4	STA a 3 4	STX a 3 4	STA al 4 * 5	8
9	BCC r 2 2	STA (d),y 2 6	STA (d) 2 * 5	STA (d,s),y 2 * 7	STY d,x 2 4	STA d,x 2 4	STX d,y 2 4	STA [d],y 2 * 6	TYA i 1 2	STA a,y 3 5	TXS i 1 2	TXY i 1 * 2	STZ a 3 * 4	STA a,x 3 5	STZ a,x 3 * 5	STA al,x 4 * 5	9
A	LDY # 2 2	LDA (d,x) 2 6	LDX # 2 2	LDA d,s 2 * 4	LDY d 2 3	LDA d 2 3	LDX d 2 3	LDA [d] 2 * 6	TAY i 1 2	LDA # 2 2	TAX i 1 2	PLB s 1 * 4	LDY a 3 4	LDA a 3 4	LDX a 3 4	LDA al 4 * 5	A
B	BCS r 2 2	LDA (d),y 2 5	LDA (d) 2 * 5	LDA (d,s),y 2 * 7	LDY d,x 2 4	LDA d,x 2 4	LDX d,y 2 4	LDA [d],y 2 * 6	CLV i 1 2	LDA a,y 3 4	TSX i 1 2	TYX i 1 * 2	LDY a,x 3 4	LDA a,x 3 4	LDX a,y 3 4	LDA al,x 4 * 5	B
C	CPY # 2 2	CMP (d,x) 2 6	REP # 2 * 3	CMP d,s 2 * 4	CPY d 2 3	CMP d 2 3	DEC d 2 5	CMP [d] 2 * 6	INY i 1 2	CMP # 2 2	DEX i 1 2	WAI i 1 * 3	CPY a 3 4	CMP a 3 4	DEC a 3 6	CMP al 4 * 5	C
D	BNE r 2 2	CMP (d),y 2 5	CMP (d) 2 * 5	CMP (d,s),y 2 * 7	PEI s 2 * 6	CMP d,x 2 4	DEC d,x 2 6	CMP [d],y 2 * 6	CLD i 1 2	CMP a,y 3 4	PHX s 1 * 3	STP i 1 * 3	JML (a) 3 * 6	CMP a,x 3 4	DEC a,x 3 7	CMP al,x 4 * 5	D
E	CPX # 2 2	SBC (d,x) 2 6	SEP # 2 * 3	SBC d,s 2 * 4	CPX d 2 3	SBC d 2 3	INC d 2 5	SBC [d] 2 * 6	INX i 1 2	SBC # 2 2	NOP i 1 2	XBA i 1 * 3	CPX a 3 4	SBC a 3 4	INC a 3 6	SBC al 4 * 5	E
F	BEQ r 2 2	SBC (d),y 2 5	SBC (d) 2 * 5	SBC (d,s),y 2 * 7	PEA s 3 * 5	SBC d,x 2 4	INC d,x 2 6	SBC [d],y 2 * 6	SED i 1 2	SBC a,y 3 4	PLX s 1 * 4	XCE i 1 * 2	JSR (a,x) 3 * 6	SBC a,x 3 4	INC a,x 3 7	SBC al,x 4 * 5	F
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	

symbol	addressing mode	symbol	addressing mode
#	immediate	[d]	direct indirect long
A	accumulator	[d],y	direct indirect long indexed
r	program counter relative	a	absolute
rl	program counter relative long	a,x	absolute indexed (with x)
i	implied	a,y	absolute indexed (with y)
s	stack	al	absolute long
d	direct	al,x	absolute long indexed
d,x	direct indexed (with x)	d,s	stack relative
d,y	direct indexed (with y)	(d,s),y	stack relative indirect indexed
(d)	direct indirect	(a)	absolute indirect
(d,x)	direct indexed indirect	(a,x)	absolute indexed indirect
(d),y	direct indirect indexed	xyz	block move

Op Code Matrix Legend

INSTRUCTION MNEMONIC		ADDRESSING MODE
BASE NO. BYTES	* = New 65C816 Opcodes ● = New 65C02 Opcodes Blank = NMOS 6502 Opcodes	BASE NO. CYCLES



TABLE 5.

OPERATION		#	a	al	d	A	I	(d),y	[d],y	(d,x)	d,x	d,y	a,x	al,x	a,y	r	rl	(a)	(d)	[d]	(a,x)	s	d,s	(d,s),y	xyc	PROCESSOR STATUS CODE								MNE-MONIC		
																										7 6 5 4 3 2 1 0										
																										N	V	M	X	D	I	Z	C			
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	N	V	1	B	D	I	Z	C	E= 0		
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	N	V	1	B	D	I	Z	C	E= 1		
ADC	A + M + C → A	69	6D	6F	65			71	77	61	75		7D	7F	79				72	67			63	73		N	V					Z	C	ADC		
AND	AAM → A	29	2D	2F	25	0A		31	37	21	35	16	3D	3F	39				32	27			23	33		N	V					Z	C	AND		
ASL	C ← [15/7] 0 → 0		0E		06											90										N	V					Z	C	ASL		
BCC	BRANCH IF C = 0															B0										N	V					Z	C	BCC		
BCS	BRANCH IF C = 1																									N	V					Z	C	BCS		
BEQ	BRANCH IF Z = 1	89	2C		24						34		3C			F0										M ₇ M ₆						Z		BEQ		
BIT	AAM (NOTE 1)															30																		BIT		
BMI	BRANCH IF N = 1															D0																		BMI		
BNE	BRANCH IF Z = 0															10																		BNE		
BPL	BRANCH IF N = 0																																		BPL	
BRA	BRANCH ALWAYS															80						00												BRA		
BRK	BREAK (NOTE 2)																																		BRK	
BRL	BRANCH LONG ALWAYS																82																	BRL		
BVC	BRANCH IF V = 0															50																		BVC		
BVS	BRANCH IF V = 1															70																		BVS		
CLC	0 → C						18																											CLC		
CLD	0 → D						D8																											CLD		
CLI	0 → I						58																											CLI		
CLV	0 → V						B8																											CLV		
CMP	A - M	C9	CD	CF	C5			D1	D7	C1	D5		DD	DF	D9				D2	C7				C3	D3	N	0					Z	C	CMP		
COP	CO-PROCESSOR	E0	EC		E4																	02				N								COP		
CPX	X - M	C0	CC		C4																					N								CPX		
CPY	Y - M		CE		C6	3A	CA				D6		DE													N								CPY		
DEC	DECREMENT																									N								DEC		
DEX	X - 1 → X																									N								DEX		
DEY	Y - 1 → Y						88																			N								DEY		
EOR	AYM → A	49	4D	4F	45	1A		51	57	41	55	F6	5D	5F	59				52	47				43	53	N						Z	EOR			
INC	INCREMENTS		EE		E6		E8																			N							Z	INC		
INX	X + 1 → X						C8																			N							Z	INX		
INY	Y + 1 → Y																									N							Z	INY		
JML	JUMP LONG TO NEW LOC.																	DC																JML		
JMP	JUMP TO NEW LOC.		4C	5C																														JMP		
JSL	JUMP LONG TO SUB.		20	22																														JSL		
JSR	JUMP TO SUB.		AD	AF				B1	B7	A1	B5		BD	BF	B9											N							Z	JSR		
LDA	M → A	A9	AD	AF	A5														B2	A7	FC				A3	B3							Z	LDA		
LDX	M → X	A2	AE		A6							B6			BE											N							Z	LDX		
LDY	M → Y	A0	AC		A4						B4	56	BC													N							Z	LDY		
LSR	0 ← [15/7] 0 → C		4E		4A																					N							Z	LSR		
MVN	M ← M BACKWARD																									54	0						Z	C	MVN	
MVP	M ← M FORWARD																									44								MVP		
NOP	NO OPERATION	09	0D	0F	05		EA	11	17	01	15		1D	1F	19											N							Z	NOP		
ORA	AVM → A																																		ORA	
PEA	Mpc + 1, Mpc + 2 → Ms - 1, Ms																										N							Z	PEA	
PEI	S - 2 → S																																		PEI	
PER	M(d), M(d + 1) → Ms - 1, Ms																																		PER	
	S - 2 → S																																			
	Mpc + rl, Mpc + rl + 1 → Ms - 1, Ms																																			
	S - 2 → S																																			
PHA	A → Ms, S - 1 → S																																			PHA
PHB	DBR → Ms, S - 1 → S																																			PHB
PHD	D → Ms, Ms - 1, S - 2 → S																																			PHD
PHK	PBR → Ms, S - 1 → S																																			PHK
PHP	P → Ms, S - 1 → S																																			PHP
PHX	X → Ms, S - 1 → S																																			PHX
PHY	Y → Ms, S - 1 → S																																			PHY
PLA	S + 1 → S, Ms → A																										N									



TABLE 6. DETAILED INSTRUCTION OPERATION

ADDRESS MODE	CYCLE	VP	ML	VDA	VPA	ADDRESS BUS	DATA BUS	R/W
1. Immediate # (LDY, CPY, CPX, LDY, ORA, AND, EOR, ADC, BIT, LDA, CMP, SBC, REP, SEP) (14 Op Codes) (2 and 3 bytes) (2 and 3 cycles)	1. 2. 2a.	1 1 1	1 1 1	1 0 0	1 1 1	PBR, PC PBR, PC+1 PBR, PC+2	Op Code IDL IDH	1 1 1
2a. Absolute # (BIT, STY, STZ, LDY, CPY, CPX, STX, LDY, ORA, AND, EOR, ADC, STA, LDA, CMP, SBC) (18 Op Codes) (3 bytes) (4 and 5 cycles)	1. 2. 3. 4. 4a.	1 1 1 1 1	1 1 1 1 1	1 0 0 0 0	1 1 1 0 0	PBR, PC PBR, PC+1 PBR, PC+2 DBR, AA DBR, AA+1	Op Code AAL AAH Data Low Data High	1 1 1 1/0 1/0
2b. Absolute (R-M-W) # (ASL, ROL, LSR, ROR, DEC, INC, TSB, TRB) (6 Op Codes) (3 bytes) (6 and 8 cycles)	1. 2. 3. 4. 4a. 5. 6a. 6.	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	1 0 0 0 0 0 0 0	1 1 1 0 0 0 0 0	PBR, PC PBR, PC+1 PBR, PC+2 DBR, AA DBR, AA+1 DBR, AA+1 DBR, AA	Op Code AAL AAH Data Low Data High Data High Data Low	1 1 1 1 1 0 0
2c. Absolute (JUMP) # (JMP) (4C) (1 Op Code) (3 bytes) (3 cycles)	1. 2. 3. 1.	1 1 1 1	1 1 1 1	1 0 0 1	1 1 1 1	PBR, PC PBR, PC+1 PBR, PC+2 PBR, NEW PC	Op Code NEW PCL NEW PCH Op Code	1 1 1 1
2d. Absolute (Jump to subroutine) # (JSR) (1 Op Code) (3 bytes) (6 cycles) (different order from N6502)	1. 2. 3. 4. 5. 6. 1.	1 1 1 1 1 1 1	1 1 1 1 1 1 1	1 0 0 0 0 0 1	1 1 1 0 0 0 1	PBR, PC PBR, PC+1 PBR, PC+2 PBR, PC+2 Q, S Q, S-1 PBR, NEW PC	Op Code NEW PCL NEW PCH IO PCH PCL Next Op Code	1 1 1 1 0 0 1
*3a. Absolute Long # (ORA, AND, EOR, ADC, STA, LDA, CMP, SBC) (8 Op Codes) (4 bytes) (5 and 6 cycles)	1. 2. 3. 4. 5. 5a.	1 1 1 1 1 1	1 1 1 1 1 1	1 0 0 0 0 0	1 1 1 0 0 0	PBR, PC PBR, PC+1 PBR, PC+2 PBR, PC+3 AAB, AA AAB, AA+1	Op Code AAL AAH AAB Data Low Data High	1 1 1 1 1/0 1/0
*3b. Absolute Long (JUMP) # (JMP) (1 Op Code) (4 bytes) (4 cycles)	1. 2. 3. 4. 1.	1 1 1 1 1	1 1 1 1 1	1 0 0 0 1	1 1 1 0 1	PBR, PC PBR, PC+1 PBR, PC+2 PBR, PC+3 NEW PBR, PC	Op Code NEW PCL NEW PCH NEW BR Op Code	1 1 1 1 1
*3c. Absolute Long (Jump to Subroutine Long) # (JSL) (1 Op Code) (4 bytes) (7 cycles)	1. 2. 3. 4. 5. 6. 7. 8. 1.	1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1	1 0 0 0 0 0 0 0 1	1 1 1 0 0 0 0 0 1	PBR, PC PBR, PC+1 PBR, PC+2 Q, S Q, S PBR, PC+3 Q, S-1 Q, S-2 NEW PBR, PC	Op Code NEW PCL NEW PCH PBR IO NEW PBR PCH PCL Next Op Code	1 1 1 0 0 1 0 0 1
4a. Direct # (BIT, STZ, STY, LDY, CPY, CPX, STX, LDY, ORA, AND, EOR, ADC, STA, LDA, CMP, SBC) (18 Op Codes) (2 bytes) (3, 4 and 5 cycles)	1. 2. 2a. 3. 3a.	1 1 1 1 1	1 1 1 1 1	1 0 0 0 0	1 1 0 1 0	PBR, PC PBR, PC+1 PBR, PC+1 Q, D+DO Q, D+DO+1	Op Code DO IO Data Low Data High	1 1 1 1/0 1/0
4b. Direct (R-M-W) # (ASL, ROL, LSR, ROR, DEC, INC, TSB, TRB) (6 Op Codes) (2 bytes) (5, 6, 7 and 8 cycles)	1. 2. 2a. 3. 3a. 4. 5. 5a.	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	1 0 0 0 0 0 0 0	1 1 0 0 0 0 0 0	PBR, PC PBR, PC+1 PBR, PC+1 Q, D+DO Q, D+DO+1 Q, D+DO+1 Q, D+DO+1	Op Code DO IO Data Low Data High Data High Data Low	1 1 1 1 1 0 0
5. Accumulator # (ASL, INC, ROL, DEC, LSR, ROR) (6 Op Codes) (1 byte) (2 cycles)	1. 2.	1 1	1 1	1 0	1 0	PBR, PC PBR, PC+1	Op Code IO	1 1
6a. Implied I (DEY, INY, INX, DEX, NOP, XCE, TYA, TAY, TXA, TXS, TAX, TSX, TCS, TSC, TCD, TDC, TXY, TYX, CLC, SEC, CLI, SEI, CLV, CLD, SED) (25 Op Codes) (1 byte) (2 cycles)	1. 2.	1 1	1 1	1 0	1 0	PBR, PC PBR, PC+1	Op Code IO	1 1
*6b. Implied I (XBA) (1 Op Code) (1 byte) (3 cycles)	1. 2. 3.	1 1 1	1 1 1	1 0 0	1 1 1	PBR, PC PBR, PC+1 PBR, PC+1	Op Code IO IO	1 1 1
6c. Wait For Interrupt (WAI) (1 Op Code) (1 byte) (3 cycles)	1. 2. 3. 1.	1 1 1 1	1 1 1 1	1 0 0 1	1 1 0 1	PBR, PC PBR, PC+1 PBR, PC+1 PBR, PC+1	Op Code IO IO IRQ(BRK)	1 1 1 1
6d. Stop-The-Clock (STP) (1 Op Code) (1 byte) (3 cycles)	1. 2. 3. 1c. 1b. 1a.	1 1 1 1 1 1	1 1 1 1 1 1	1 0 0 0 0 0	1 1 0 0 0 0	PBR, PC PBR, PC+1 PBR, PC+1 PBR, PC+1 PBR, PC+1 PBR, PC+1	Op Code IO IO RES(BRK) RES(BRK) RES(BRK) BEGIN	1 1 1 1 1 1
See 21a Stack (Hardware interrupt)								
7. Direct Indirect Indexed (d), y (ORA, AND, EOR, ADC, STA, LDA, CMP, SBC) (8 Op Codes) (2 bytes) (5, 6, 7 and 8 cycles)	1. 2. 2a. 3. 4. 4a. 5. 5a.	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	1 0 0 0 0 0 0 0	1 1 0 0 0 0 0 0	PBR, PC PBR, PC+1 PBR, PC+1 Q, D+DO Q, D+DO+1 DBR, AAH, AAL+Y DBR, AA+Y DBR, AA+Y+1	Op Code DO IO AAL AAL YL IO Data Low Data High	1 1 1 1 1 1/0 1/0
8. Direct Indirect Indexed Long (d), y (ORA, AND, EOR, ADC, STA, LDA, CMP, SBC) (8 Op Codes) (2 bytes) (6, 7 and 8 cycles)	1. 2. 2a. 3. 4. 5. 6. 6a.	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	1 0 0 0 0 0 0 0	1 1 0 0 0 0 0 0	PBR, PC PBR, PC+1 PBR, PC+1 Q, D+DO Q, D+DO+1 AAB, AA+Y AAB, AA+Y+1	Op Code DO IO AAL AAL Data Low Data High	1 1 1 1 1 1/0 1/0
9. Direct Indexed Indirect (d), x (ORA, AND, EOR, ADC, STA, LDA, CMP, SBC) (8 Op Codes) (2 bytes) (6, 7 and 8 cycles)	1. 2. 2a. 3. 4. 5. 6. 6a.	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	1 0 0 0 0 0 0 0	1 1 0 0 0 0 0 0	PBR, PC PBR, PC+1 PBR, PC+1 Q, D+DO Q, D+DO+1 DBR, AA DBR, AA+1	Op Code DO IO AAL AAL Data Low Data High	1 1 1 1 1 1/0 1/0
10a. Direct, X d, x (BIT, STZ, STY, LDY, ORA, AND, EOR, ADC, STA, LDA, CMP, SBC) (11 Op Codes) (2 bytes) (4, 5 and 6 cycles)	1. 2. 2a. 3. 4. 4a.	1 1 1 1 1 1	1 1 1 1 1 1	1 0 0 0 0 0	1 1 0 0 0 0	PBR, PC PBR, PC+1 PBR, PC+1 Q, D+DO Q, D+DO+1	Op Code DO IO IO Data Low Data High	1 1 1 1 1/0 1/0
10b. Direct, X(R-M-W) d, x (ASL, ROL, LSR, ROR, DEC, INC) (6 Op Codes) (2 bytes) (6, 7, 8 and 9 cycles)	1. 2. 2a. 3. 4. 4a. 5. 6a.	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	1 0 0 0 0 0 0 0	1 1 0 0 0 0 0 0	PBR, PC PBR, PC+1 PBR, PC+1 Q, D+DO Q, D+DO+1 Q, D+DO+1 Q, D+DO+1	Op Code DO IO Data Low Data High Data High Data Low	1 1 1 1 1 0 0
11. Direct, Y d, y (STX, LDY) (2 Op Codes) (2 bytes) (4, 5 and 6 cycles)	1. 2. 2a. 3. 4. 4a.	1 1 1 1 1 1	1 1 1 1 1 1	1 0 0 0 0 0	1 1 0 0 0 0	PBR, PC PBR, PC+1 PBR, PC+1 Q, D+DO Q, D+DO+1	Op Code DO IO Data Low Data High	1 1 1 1/0 1/0
12a. Absolute, X #, x (BIT, LDY, STZ, ORA, AND, EOR, ADC, STA, LDA, CMP, SBC) (11 Op Codes) (3 bytes) (4, 5 and 6 cycles)	1. 2. 3. 4. 3a. 4a.	1 1 1 1 1 1	1 1 1 1 1 1	1 0 0 0 0 0	1 1 0 0 0 0	PBR, PC PBR, PC+1 PBR, PC+2 DBR, AAH, AAL+XL DBR, AA+X DBR, AA+X+1	Op Code AAL AAH XL IO Data Low Data High	1 1 1 1 1/0 1/0
12b. Absolute, X(R-M-W) #, x (ASL, ROL, LSR, ROR, DEC, INC) (6 Op Codes) (3 bytes) (7 and 9 cycles)	1. 2. 3. 4. 5. 5a. 6. 7a.	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	1 0 0 0 0 0 0 0	1 1 0 0 0 0 0 0	PBR, PC PBR, PC+1 PBR, PC+2 DBR, AAH, AAL+XL DBR, AA+X DBR, AA+X+1 DBR, AA+X	Op Code AAL AAH XL IO Data Low Data High Data High Data Low	1 1 1 1 1 0 0
*13. Absolute Long, X #, x (ORA, AND, EOR, ADC, STA, LDA, CMP, SBC) (8 Op Codes) (4 bytes) (5 and 6 cycles)	1. 2. 3. 4. 5. 5a.	1 1 1 1 1 1	1 1 1 1 1 1	1 0 0 0 0 0	1 1 0 0 0 0	PBR, PC PBR, PC+1 PBR, PC+2 PBR, PC+3 AAB, AA+X AAB, AA+X+1	Op Code AAL AAH AAB Data Low Data High	1 1 1 1 1/0 1/0
14. Absolute, Y #, y (LDX, ORA, AND, EOR, ADC, STA, LDA, CMP, SBC) (9 Op Codes) (3 bytes) (4, 5 and 6 cycles)	1. 2. 3. 3a. 4. 4a.	1 1 1 1 1 1	1 1 1 1 1 1	1 0 0 0 0 0	1 1 0 0 0 0	PBR, PC PBR, PC+1 PBR, PC+2 DBR, AAH, AAL+YL DBR, AA+Y DBR, AA+Y+1	Op Code AAL AAH YL IO Data Low Data High	1 1 1 1/0 1/0 1/0
15. Relative r (BPL, BMI, BVC, BVS, BCC, BCS, BNE, BEQ, BRA) (9 Op Codes) (2 bytes) (2, 3 and 4 cycles)	1. 2. 2a. 2b. 1.	1 1 1 1 1	1 1 1 1 1	1 0 0 0 1	1 1 0 0 1	PBR, PC PBR, PC+1 PBR, PC+1 PBR, PC+1 PBR, PC+Offset	Op Code Offset IO IO Op Code	1 1 1 1 1

TABLE 6. DETAILED INSTRUCTION OPERATION (CONT.)

ADDRESS MODE	CYCLE	VP	ML	VDA,VPA	ADDRESS BUS	DATA BUS	R/W	ADDRESS MODE	CYCLE	VP	ML	VDA,VPA	ADDRESS BUS	DATA BUS	R/W		
*16. Relative Long r1 (BRL) (1 Op Code) (3 bytes) (4 cycles)	1.	1	1	1	1	PBR,PC	Op Code	1	21f. Stack (Push) # (PHP,PHA,PHY,PHX,PHD,PHK,PHB) (7 Op Codes) (1 byte) (3 and 4 cycles)	1.	1	1	1	1	PBR,PC'	Op Code	1
	2.	1	1	0	1	PBR,PC+1	Offset Low	1		2.	1	1	0	0	PBR,PC+1	IO	1
	3.	1	1	0	1	PBR,PC+2	Offset High	1		(1) 3a.	1	1	1	0	0,S	Register High	1
	4.	1	1	0	0	PBR,PC+2	IO	1		3.	1	1	1	0	0,S-1	Register Low	1
17a. Absolute Indirect (#) (JMP) (1 Op Code) (3 bytes) (5 cycles)	1.	1	1	1	1	PBR,PC	Op Code	1	21g. Stack (Pull) # (PLP,PLA,PLY,PLX,PLD,PLB) (Different than N6502) (6 Op Codes) (1 byte) (4 and 5 cycles)	1.	1	1	1	1	PBR,PC	Op Code	1
	2.	1	1	0	1	PBR,PC+1	AAL	1		2.	1	1	0	0	PBR,PC+1	IO	1
	3.	1	1	0	1	PBR,PC+2	AAH	1		3.	1	1	0	0	PBR,PC+1	IO	1
	4.	1	1	1	0	0,AA	NEW PCL	1		4.	1	1	1	0	0,S+1	Register Low	1
	5.	1	1	1	0	0,AA+1	NEW PCH	1		(1) 4a.	1	1	1	0	0,S+2	Register High	1
*17b. Absolute Indirect (#) (JML) (1 Op Code) (3 bytes) (6 cycles)	1.	1	1	1	1	PBR,NEW PC	Op Code	1	*21h. Stack (Push Effective Indirect Address) # (PEI) (1 Op Code) (2 bytes) (6 and 7 cycles)	1.	1	1	1	1	PBR,PC	Op Code	1
	2.	1	1	0	1	PBR,PC+1	AAL	1		2.	1	1	0	1	PBR,PC+1	DO	1
	3.	1	1	0	1	PBR,PC+2	AAH	1		(2) 2a.	1	1	0	0	PBR,PC+1	IO	1
	4.	1	1	1	0	0,AA	NEW PCL	1		3.	1	1	1	0	0,D+DO	AAL	1
	5.	1	1	1	0	0,AA+1	NEW PCH	1		4.	1	1	1	0	0,D+DO+1	AAH	1
	6.	1	1	1	0	0,AA+2	NEW PBR	1		5.	1	1	1	0	0,S	AAH	0
*18. Direct Indirect (d) (ORA,AND,EOR,ADC,STA,LDA,CMP,SBC) (8 Op Codes) (2 bytes) (5,6 and 7 cycles)	1.	1	1	1	1	PBR,PC	Op Code	1	*21i. Stack (Push Effective Absolute Address) # (PEA) (1 Op Code) (3 bytes) (5 cycles)	1.	1	1	1	1	PBR,PC	Op Code	1
	2.	1	1	0	1	PBR,PC+1	DO	1		2.	1	1	0	1	PBR,PC+1	AAL	1
	(2) 2a.	1	1	0	0	PBR,PC+1	IO	1		3.	1	1	0	1	PBR,PC+2	AAH	1
	3.	1	1	1	0	0,D+DO	AAL	1		4.	1	1	1	0	0,S	AAH	0
	4.	1	1	1	0	0,D+DO+1	AAH	1		5.	1	1	1	0	0,S-1	AAL	0
	5.	1	1	1	0	DBR,AA	Data Low	1/0		*21j. Stack (Push Effective Program Counter Relative Address) # (PER) (1 Op Code) (3 bytes) (6 cycles)	1.	1	1	1	1	PBR,PC	Op Code
(1) 5a.	1	1	1	0	DBR,AA+1	Data Low	1/0	2.	1		1	0	1	PBR,PC+1	Offset Low	1	
*19. Direct Indirect Long [d] (ORA,AND,EOR,ADC,STA,LDA,CMP,SBC) (8 Op Codes) (2 bytes) (6,7 and 8 cycles)	1.	1	1	1	1	PBR,PC	Op Code	1	3.		1	1	0	1	PBR,PC+2	Offset High	1
	2.	1	1	0	1	PBR,PC+1	DO	1	4.		1	1	0	0	PBR,PC+2	IO	1
	(2) 2a.	1	1	0	0	PBR,PC+1	IO	1	5.		1	1	1	0	0,S	PCH+OFF+CARRY	0
	3.	1	1	1	0	0,D+DO	AAL	1	6.		1	1	1	0	0,S-1	PCL+OFFSET	0
	4.	1	1	1	0	0,D+DO+1	AAH	1	*22. Stack Relative d,s (ORA,AND,EOR,ADL,STA,LDA,CMP,SDC) (8 Op Codes) (2 bytes) (4 and 5 cycles)	1.	1	1	1	1	PBR,PC	Op Code	1
	5.	1	1	1	0	0,D+DO+2	AAB	1		2.	1	1	0	1	PBR,PC+1	SO	1
6.	1	1	1	0	AAB,AA	Data Low	1/0	3.		1	1	0	0	PBR,PC+1	IO	1	
(1) 6a.	1	1	1	0	AAB,AA+1	Data High	1/0	4.		1	1	1	0	0,S+SO	Data Low	1/0	
1.	1	1	1	1	PBR,PC	Op Code	1	(1) 4a.		1	1	1	0	0,S+SO+1	Data High	1/0	
20a. Absolute Indexed Indirect (#,x) (JMP) (1 Op Code) (3 bytes) (6 cycles)	1.	1	1	1	1	PBR,PC	Op Code	1		*23. Stack Relative Indirect Indexed (d,s),y (ORA,AND,EOR,ADC,STA,LDA,CMP,SDC) (8 Op Codes) (2 bytes) (7 and 8 Cycles)	1.	1	1	1	1	PBR,PC	Op Code
2.	1	1	0	1	PBR,PC+1	AAL	1	2.	1		1	0	1	PBR,PC+1	SO	1	
3.	1	1	0	1	PBR,PC+2	AAH	1	3.	1		1	0	0	PBR,PC+1	IO	1	
4.	1	1	0	0	PBR,PC+2	IO	1	4.	1		1	1	0	0,S+SO	AAL	1	
5.	1	1	0	1	PBR,AA+X	NEW PCL	1	5.	1		1	1	0	0,S+SO+1	AAH	1	
6.	1	1	0	1	PBR,AA+X+1	NEW PCH	1	6.	1		1	0	0	0,S+SO+1	IO	1	
1.	1	1	1	1	PBR,NEW PC	Op Code	1	7.	1		1	1	0	DBR,AA+Y	Data Low	1/0	
*20b. Absolute Indexed Indirect (Jump to Subroutine Indexed Indirect) (#,x) (JSR) (1 Op Code) (3 bytes) (8 cycles)	1.	1	1	1	1	PBR,PC	Op Code	1	(1) 7a.		1	1	1	0	DBR,AA+Y+1	Data High	1/0
	2.	1	1	0	1	PBR,PC+1	AAL	1	1.	1	1	1	1	PBR,PC	Op Code	1	
	3.	1	1	1	0	0,S	PCH	0	2.	1	1	0	1	PBR,PC+1	DBA	1	
	4.	1	1	1	0	0,S-1	PCL	0	3.	1	1	0	1	PBR,PC+2	SBA	1	
	5.	1	1	0	1	PBR,PC+2	AAH	1	N-2 4.	1	1	1	0	SBA,X	Source Data	1	
	6.	1	1	0	0	PBR,PC+2	IO	1	Byte 5.	1	1	1	0	DBA,Y	Dest. Data	0	
	7.	1	1	0	1	PBR,AA+X	NEW PCL	1	C=2 6.	1	1	0	0	DBA,Y	IO	1	
	8.	1	1	0	1	PBR,AA+X+1	NEW PCH	1	7.	1	1	0	0	DBA,Y	IO	1	
21a. Stack (Hardware Interrupts) # (IRQ,NMI,ABORT,RES) (4 hardware interrupts) (0 bytes) (7 and 8 cycles)	1.	1	1	1	1	PBR,NEW PC	Next Op Code	1	*24a. Block Move Positive (forward) xyc (MVP) (1 Op Code) (3 bytes) (7 cycles) x = Source Address y = Destination c = Number of Bytes to Move -1 x,y Decrement MVP is used when the destination start address is higher (more positive) than the source start address.	1.	1	1	1	1	PBR,PC	Op Code	1
	(3) 2.	1	1	0	0	PBR,PC	IO	1		2.	1	1	0	1	PBR,PC+1	DBA	1
	(7) 3.	1	1	1	0	0,S	PBR	0		3.	1	1	0	1	PBR,PC+2	SBA	1
	4.	1	1	1	0	0,S-1	PCH	0		N-4 4.	1	1	1	0	SBA,X	Source Data	1
	5.	1	1	1	0	0,S-2	PCL	0		Byte 5.	1	1	1	0	DBA,Y	Dest. Data	0
	6.	1	1	1	0	0,S-3	P	0		C=2 6.	1	1	0	0	DBA,Y	IO	1
	7.	0	1	1	0	0,VA	AAVL	1		7.	1	1	0	0	DBA,Y	IO	1
	8.	0	1	1	0	0,VA+1	AAVH	1		1.	1	1	1	1	PBR,PC	Op Code	1
21b. Stack (Software Interrupts) # (BRK,COP) (2 Op Codes) (2 bytes) (7 and 8 cycles)	1.	1	1	1	1	0,AAV	Next Op Code	1	*24b. Block Move Negative (backward) xyc (MVN) (1 Op Code) (3 bytes) (7 cycles) x = Source Address y = Destination c = Number of Bytes to Move -1 x,y Increment	2.	1	1	0	1	PBR,PC+1	DBA	1
	(3) 2.	1	1	0	1	PBR,PC+1	Signature	1		3.	1	1	0	1	PBR,PC+2	SBA	1
	(7) 3.	1	1	1	0	0,S	PBR	0		4.	1	1	1	0	SBA,X	Source Data	1
	4.	1	1	1	0	0,S-1	PCH	0		Byte 5.	1	1	1	0	SBA,X	Source Data	1
	5.	1	1	1	0	0,S-2	PCL	0		C=2 6.	1	1	0	0	DBA,Y	Dest. Data	0
	6.	1	1	1	0	0,S-3	(COP Latches) P	0		7.	1	1	0	0	DBA,Y-2	IO	1
	7.	0	1	1	0	0,VA	AAVL	1		1.	1	1	1	1	PBR,PC	Op Code	1
	8.	0	1	1	0	0,VA+1	AAVH	1		2.	1	1	0	1	PBR,PC+1	DBA	1
21c. Stack (Return from Interrupt) # (RTI) (1 Op Code) (1 byte) (6 and 7 cycles) (different order from N6502)	1.	1	1	1	1	0,AAV	Next Op Code	1	*24c. Block Move Positive (backward) xyc (MVN) (1 Op Code) (3 bytes) (7 cycles) x = Source Address y = Destination c = Number of Bytes to Move -1 x,y Increment	3.	1	1	0	1	PBR,PC+2	SBA	1
	(3) 2.	1	1	0	0	PBR,PC+1	IO	1		4.	1	1	1	0	SBA,X-2	Source Data	1
	(7) 3.	1	1	1	0	0,S+1	P	1		Byte 5.	1	1	1	0	DBA,Y-2	Dest. Data	0
	4.	1	1	1	0	0,S+2	PCL	1		C=1 6.	1	1	0	0	DBA,Y-2	IO	1
	5.	1	1	1	0	0,S+3	PCH	1		7.	1	1	0	0	DBA,Y-2	IO	1
	6.	1	1	1	0	0,S+4	PBR	1		1.	1	1	1	1	PBR,PC	Op Code	1
	7.	1	1	1	0	PBR,PC	New Op Code	1		2.	1	1	0	1	PBR,PC+1	DBA	1
	1.	1	1	1	1	PBR,PC	Op Code	1		3.	1	1	0	1	PBR,PC+2	SBA	1
21d. Stack (Return from Subroutine) # (RTS) (1 Op Code) (1 byte) (6 cycles)	2.	1	1	0	0	PBR,PC+1	IO	1	*24d. Block Move Negative (backward) xyc (MVN) (1 Op Code) (3 bytes) (7 cycles) x = Source Address y = Destination c = Number of Bytes to Move -1 x,y Increment	4.	1	1	1	0	SBA,X+1	Source Data	1
	3.	1	1	0	0	PBR,PC+1	IO	1		Byte 5.	1	1	1	0	DBA,Y+1	Dest. Data	0
	4.	1	1	1	0	0,S+1	PCL	1		C=1 6.	1	1	0	0	DBA,Y+1	IO	1
	5.	1	1	1	0	0,S+2	PCH	1		7.	1	1	0	0	DBA,Y+1	IO	1
	6.	1	1	1	0	0,S+2	IO	1		1.	1	1	1	1	PBR,PC	Op Code	1
	1.	1	1	1	1	PBR,PC	Op Code	1		2.	1	1	0	1	PBR,PC+1	DBA	1
	2.	1	1	0	0	PBR,PC+1	IO	1		3.	1	1	0	1	PBR,PC+2	SBA	1
	3.	1	1	0	0	PBR,PC+1	IO	1		4.	1	1	1	0	SBA,X+2	Source Data	1
*21e. Stack (Return from Subroutine Long) # (RTL) (1 Op Code) (1 byte) (6 cycles)	4.	1	1	1	0	0,S+1	NEW PCL	1	*24e. Block Move Negative (backward) xyc (MVN) (1 Op Code) (3 bytes) (7 cycles) x = Source Address y = Destination c = Number of Bytes to Move -1 x,y Increment	5.	1	1	1	0	DBA,Y+2	Dest. Data	0
	5.	1	1	1	0	0,S+2	NEW PCH	1		6.	1	1	0	0	DBA,Y+2	IO	1
	6.	1	1	1	0	0,S+3	NEW PBR	1		7.	1	1	0	0	DBA,Y+2	IO	1
	1.	1	1	1	1	NEW PBR,PC	Next Op Code	1		1.	1	1	1	1	PBR,PC+3	Next Op Code	1
	2.	1	1	0	0	PBR,PC+1	IO	1		2.	1	1	0	1	PBR,PC+1	DBA	1
	3.	1	1	0	0	PBR,PC+1	IO	1		3.	1	1	0	1	PBR,PC+2	SBA	1

TABLE 5. NOTES
Notes:

1. Bit immediate N and V flags not affected. When M = 0, M₁₅ → N and M₁₄ → V.
2. Break Bit (B) in Status register indicates hardware or software break.

3. ★ = New 65C816 Instructions
● = New 65C02 Instructions
Blank = NMOS 6502

- + Add V OR
- Subtract ✕ Exclusive OR
Λ AND

TABLE 6. NOTES
Notes:

- (1) Add 1 byte (for immediate only) for M=0 or X=0 (i.e. 16 bit data), add 1 cycle for M=0 or X=0.
- (2) Add 1 cycle for direct register low (DL) not equal 0.
- (3) Special case for aborting instruction. This is the last cycle which may be aborted or the Status, PBR or DBR registers will be updated.
- (4) Add 1 cycle for indexing across page boundaries, or write, or X=0. When X=1 or in the emulation mode, this cycle contains invalid addresses.
- (5) Add 1 cycle if branch is taken.
- (6) Add 1 cycle if branch is taken across page boundaries in 6502 emulation mode (E=1).
- (7) Subtract 1 cycle for 6502 emulation mode (E=1).
- (8) Add 1 cycle for REP, SEP.
- (9) Wait at cycle 2 for 2 cycles after \overline{NMI} or \overline{IRQ} active input.

Abbreviations:

AAB Absolute Address Bank
AAH Absolute Address High
AAL Absolute Address Low
AAVH Absolute Address Vector High
AAVL Absolute Address Vector Low
C Accumulator
D Direct Register
DBA Destination Bank Address
DBR Data Bank Register
DO Direct Offset
IDH Immediate Data High
IDL Immediate Data Low
IO Internal Operation
P Status Register
PBR Program Bank Register
PC Program Counter
R-M-W Read-Modify-Write
S Stack Address
SBA Source Bank Address
SO Stack Offset
VA Vector Address
x,y Index Registers
★ = New 65C816 Addressing Modes
● = New 65C02 Addressing Modes
Blank = NMOS 6502 Addressing Modes

RECOMMENDED ASSEMBLER SYNTAX STANDARDS

DIRECTIVES

Assembler directives are those parts of the assembly language source program that give directions to the assembler; this includes the definition of data area and constants within a program. This standard excludes any definitions of assembler directives.

COMMENTS

An assembler should provide a way to use any line of the source program as a comment. The recommended way of doing this is to treat any blank line, or any line that starts with a semicolon or an asterisk, as a comment. Other special characters may be used as well.

THE SOURCE LINE

Any line that causes the generation of a single VL65C816 machine language instruction should be divided into four fields: a label field, the operation code, the operand, and the comment field.

The Label Field - The label field begins in column one of the line. A label must start with an alphabetic character, and may be followed by zero or more alphanumeric characters. An assembler may define an upper limit on the number

of characters that can be in a label, as long as that upper limit is greater than or equal to six characters. An assembler may limit the alphabetic characters to upper case characters if desired. If lower case characters are allowed, they should be treated as identical to their upper case equivalents. Other characters may be allowed in the label, as long as their use does not conflict with the coding of operand fields.

The Operation Code Field - The operation code consists of a three-character sequence (mnemonic) from Table 2. It starts no sooner than column two of the line, or one space after the label if a label is coded.

Many of the operation codes in Table 2 have duplicate mnemonics; when two or more machine language instructions have the same mnemonic, the assembler resolves the difference based on the operand.

If an assembler allows lower case letters in labels, it must also allow lower case letters in mnemonics. When lower case letters are used in the mnemonic, they

are treated as equivalent to the upper-case counterpart. Thus, the mnemonics LDA, lda, and LdA must all be recognized, and are equivalent.

In addition to the mnemonics in Table 2, an assembler may provide the alternative mnemonics shown in Table 7.

SJL should be recognized as equivalent to JSR when it is specified with a long absolute address. JML is equivalent to JMP with long addressing force.

The Operand Field - The operand field may start no sooner than one space after the operation code field. The assembler must be capable of at least 24-bit address calculations. The assembler should be capable of specifying addresses as labels, integer constants, and hexadecimal constants. The assembler must allow addition and subtraction in the operand field. Labels are recognized by the fact that they start with alphabetic characters. Decimal numbers are recognized as containing only the decimal digits 0 through 9. Hexadecimal constants shall be recognized by prefixing the constant

with a dollar sign (\$) character, followed by zero or more of either the decimal digits or the hexadecimal digits A through F. If lower case letters are allowed in the label field, then they are also allowed as hexadecimal digits.

All constants, no matter what their format, provide at least enough precision to specify all values that can be represented by a 24-bit signed or unsigned integer represented in two's complement notation.

Table 9 shows the operand formats that are recognized by the assembler. The symbol **d** is a label or value that the assembler can recognize as being less than #100. The symbol **a** is a label or value which the assembler can recognize as greater than \$FF but less than \$10000; the symbol **al** is a label or value that the assembler can recognize as being greater than \$FFFF. The symbol **EXT** is a label that cannot be located by the assembler at the time the instruction is assembled. Unless instructed otherwise, an assembler assumes that **EXT** labels are two bytes long. The symbols **r** and **rl** are 8- and 16-bit signed displacements calculated by the assembler.

Note that the operand does not determine whether or not immediate addressing loads one or two bytes; this is determined by the setting of the status register. This forces the requirement for a directive or directives that tell the assembler to generate one or two bytes of space for immediate loads. The directives provided must allow separate

settings for the accumulator and index registers.

The assembler shall use the **<**, **>**, and **^** characters after the **#** character in an immediate address to specify which byte or bytes are to be selected from the value of the operand. Any calculations in the operand must be performed before the byte selection takes place. Table 8 defines the action taken by each operand by showing the effect of the operator on an address. The column that shows a two-byte immediate value shows the bytes in the order in which they appear in memory. The coding of the operand is for an assembler that uses 32 bit address calculations, showing the way that the address should be reduced to a 24 bit value.

In any location in an operand in which an address, or expression resulting in an address, can be coded, the assembler recognizes the prefix characters **<**, **|**, and **>**, which force one-byte (direct page), two-byte (absolute) or three-byte (long absolute) addressing. In cases in which the addressing mode is not forced, the assembler shall assume that the address is two bytes unless the assembler is able to determine the type of addressing required by context, in which case that addressing mode is used. Addresses are truncated without error if an addressing mode is forced that does not require the entire value of the address. For example:

```
LDA    $0203
LDA    $010203
```

are completely equivalent. If the addressing mode is not forced, and the type of addressing cannot be determined from context, the assembler assumes that a two-byte address is to be used. If an instruction does not have a short addressing mode (as in **LDA**, which has no direct page indexed by **Y**) and a short address is used in the operand, the assembler automatically extends the address by padding the most significant bytes with zeros in order to extend the address to the length needed. As with immediate addressing, any expression evaluation takes place before the address is selected; thus, the address selection character is only used once, before the address of expression.

The exclamation point (!) character should be supported as an alternative to the vertical bar (|).

A long indirect address is indicated in the operand field of an instruction by surrounding the direct page address where the indirect address is found by square brackets; direct page addresses that contains 16-bit addresses are indicated by being surrounded by parentheses.

The operands of a block move instruction are specified as source bank, destination band (the opposite order of the object bytes generated).

Comment Field -The comment field may start no sooner than one space after the operation code field or operand code field or operand field, depending on instruction type.

TABLE 7. ALTERNATIVE MNEMONICS

Standard	Alias
BCC	BLT
BCS	BGE
CMP A	CMA
DEC A	DEA
INC A	INA
JSL	JSR
JML	JMP
TCD	TAD
TCS	TAS
TDC	TDA
TSC	TSA
XBA	SWA

TABLE 8. BYTE SELECTION OPERATOR

Operand	One Byte Result	Two Byte Result
#\$01020304	04	04 03
#<\$01020304	04	04 03
#>\$01020304	03	03 02
#^\$01020304	02	02 01

TABLE 9. ADDRESS MODE FORMATS

Addressing Mode	Format	Addressing Mode	Format			
Immediate	#d	Absolute Indexed by Y	!d,y	(the assembler calculates r and rl)		
	#a		d,y			
	#al		a,y			
	#EXT		!a,y			
	#<d		!al,y			
	#<a		!EXT,y			
	#<al		EXT,y			
	#<EXT		>d,x			
	#>d		>a,x			
	#>a		>al,x			
	#>al		al,x			
	#>EXT		>EXT,x			
	#^d		d			
	#^a		a			
	#^al		al			
Absolute	#^EXT	Relative and Program Counter	EXT			
	!d	Relative Long	(d)			
	!a	Absolute Indirect	(!d)			
	a		(a)			
	!al		(!a)			
	!EXT		(!al)			
	EXT		(EXT)			
	Absolute Long	>d	Direct Indirect	(d)		
		>a		(<a)		
		>al		(<al)		
		al		(<EXT)		
		>EXT		[d]		
	Direct Page	d	Direct Indirect Long	[<a]		
		<d		[<al]		
		<a		[<EXT]		
<al		(d,x)				
<EXT		(!d,x)				
Accumulator Implied Addressing Direct Indirect Indexed	A	Absolute Indexed	(a,x)			
	(no operand)		(!a,x)			
	(d),y		(!al,x)			
	(<d),y		(EXT,x)			
	(<a),y		(!EXT,x)			
	(<al),y		(no operand)			
	(<EXT),y		Stack Addressing	(d,s),y		
	Direct Indirect Indexed Long		[d],y	Stack Relative Indirect Indexed	(<d,s),y	
			[<d],y		(<a,s),y	
			[<a],y		(<al,s),y	
			[<al],y		(<EXT,s),y	
			[<EXT],y		d,d	
	Direct Indexed Indirect		(d,x)	Block Move	d,a	
			(<d,x)		d,al	
			(<a,x)		d,EXT	
(<al,x)		a,d				
(<EXT,x)		a,a				
Direct Indexed by X	d,x		a,al			
	<d,x		a,EXT			
	<a,x		al,d			
	<al,x		al,a			
	<EXT,x		al,al			
Direct Indexed by Y	d,y		al,EXT			
	<d,y		EXT,d			
	<a,y		EXT,a			
	<al,y		EXT,al			
	<EXT,y		EXT,EXT			
Absolute Indexed by X	d,x					
	!d,x					
	a,x					
	!a,x					
	!al,x					
	!EXT,x					
	EXT,x					

(the assembler calculates r and rl)

Note: The alternate ! (exclamation point) is used in place of the | (vertical bar).

TABLE 10. ADDRESSING MODE SUMMARY

Address Mode	Instruction Times In Memory Cycles		Memory Utilization In Number of Program Sequence Bytes	
	Original 8 Bit NMOS 6502	New 65C816	Original 8 Bit NMOS 6502	New 65C816
1. Immediate	2	2 ⁽³⁾	2	2 ⁽³⁾
2. Absolute	4 ⁽⁵⁾	4 ^(3,5)	3	3
3. Absolute Long	—	5 ⁽³⁾	—	4
4. Direct	3 ⁽⁵⁾	3 ^(3,4,5)	2	2
5. Accumulator	2	2	1	1
6. Implied	2	2	1	1
7. Direct Indirect Indexed (d),y	5 ⁽¹⁾	5 ^(1,3,4)	2	2
8. Direct Indirect Indexed Long [d], y	—	6 ^(3,4)	—	2
9. Direct Indexed Indirect (d,x)	6	6 ^(3,4)	2	2
10. Direct, X	4 ⁽⁵⁾	4 ^(3,4,5)	2	2
11. Direct, Y	4	4 ^(3,4)	2	2
12. Absolute, X	4 ^(1,5)	4 ^(1,3,5)	3	3
13. Absolute Long, X	—	5 ⁽³⁾	—	4
14. Absolute, Y	4 ⁽¹⁾	4 ^(1,3)	3	3
15. Relative	2 ^(1,2)	2 ⁽²⁾	2	2
16. Relative Long	—	3 ⁽²⁾	—	3
17. Absolute Indirect (Jump)	5	5	3	3
18. Direct Indirect	—	5 ^(3,4)	—	2
19. Direct Indirect Long	—	6 ^(3,4)	—	2
20. Absolute Indexed Indirect (Jump)	—	6	—	3
21. Stack	3-7	3-8	1-3	1-4
22. Stack Relative	—	4 ⁽³⁾	—	2
23. Stack Relative Indirect Indexed	—	7 ⁽³⁾	—	2
24. Block Move X, Y, C (Source, Destination, Block Length)	—	7	—	3

NOTES:

1. Page boundary, add 1 cycle if page boundary is crossed when forming address.
2. Branch taken, add 1 cycle if branch is taken.
3. M = 0 or X = 0, 16 bit operation, add 1 cycle, add 1 byte for immediate.
4. Direct register low (DL) not equal zero, add 1 cycle.
5. Read-Modify-Write, add 2 cycles for M = 1, add 3 cycles for M = 0.

ADDRESSING PREFACE

The VL65C816 is capable of directly addressing 16M Bytes of memory. This address space has special significance within certain addressing modes.

RESET AND INTERRUPT VECTORS

The Reset and Interrupt vectors use the majority of the fixed addresses between 00FFE0 and 00FFFF.

STACK

The stack may use memory from 000000 to 00FFFF. The effective address of Stack and Stack Relative addressing modes is always within this range.

DIRECT

The Direct addressing modes are usually used to store memory registers and pointers. The effective address generated by Direct, Direct X, and

Direct Y addressing modes is always in Bank 0 (000000-00FFFF).

PROGRAM ADDRESS SPACE

The Program Bank Register is not affected by the Relative, Relative Long, Absolute, Absolute Indirect, and Absolute Indexed Indirect addressing modes or by incrementing the Program Counter from FFFF. The only instructions that affect the Program Bank Register are: RTI, RTL, JML, JSL, and JMP Absolute Long. Program code may exceed 64K bytes, although code segments may not span bank boundaries.

DATA ADDRESS SPACE

The data address space is contiguous throughout the 16M Byte address space. Words, arrays, records, or any data structures may span 64k Byte bank

boundaries with no compromise in code efficiency. The following addressing modes generate 24-bit effective addresses:

- Direct Indexed Indirect (d,x)
- Direct Indirect Indexed (d), y
- Direct Indirect (d)
- Direct Indirect Long [d]
- Direct Indirect Long Indexed [d], y
- Absolute a
- Absolute a, x
- Absolute a, y
- Absolute Long al
- Absolute Long Indexed al, x
- Stack Relative Indirect Indexed (d), y

The following addressing modes are available for use in the VL65C816 microprocessor. Detailed descriptions of the 24 addressing modes are given in the following section.

ADDRESSING MODES

1. Immediate Addressing—#

The operand is the second byte (second and third bytes when in the 16-bit mode) of the instruction.

2. Absolute—a

With Absolute addressing the second and third bytes of the instruction form the low-order 16 bits of the effective address. The Data Bank Register contains the high-order 8 bits of the operand address.

Instruction:	opcode	addrl	addrh
Operand Address:	DBR	addrh	addrl

3. Absolute Long—al

The second, third, and fourth byte of the instruction form the 24-bit effective address.

Instruction:	opcode	addrl	addrh	baddr
Operand Address:	baddr	addrh	addrl	

4. Direct—d

The second byte of the instruction is added to the Direct Register (D) to form the effective address. An additional cycle is required when the Direct Register is not page aligned (DL not equal 0). The Bank register is always 0.

Instruction:	opcode	offset
		Direct Register
	+	offset
Operand Address:	00	effective address

5. Accumulator—A

This form of addressing always uses a single byte instruction. The operand is the Accumulator.

6. Implied—i

Implied addressing uses a single byte instruction. The operand is implicitly defined by the instruction.

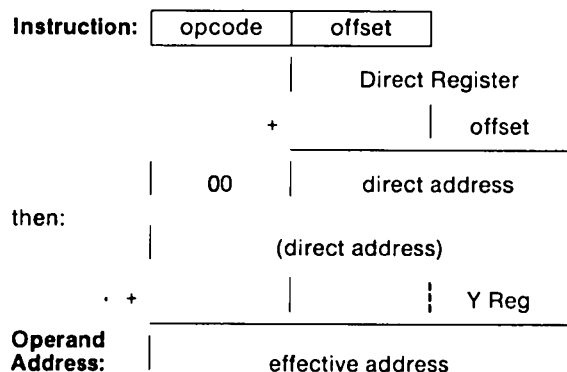
7. Direct Indirect Indexed—(d),y

This address mode is often referred to as Indirect,Y. The second byte of the instruction is added to the Direct Register (D). The 16-bit contents of this memory location is then combined with the Data Bank register to form a 24-bit base address. The Y Index Register is added to the base address to form the effective address.

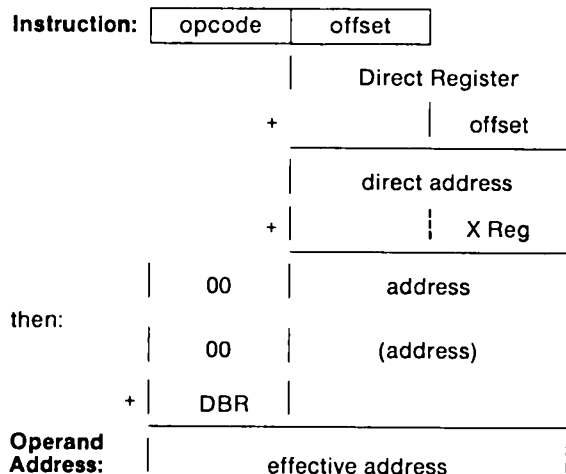
instruction:	opcode		offset	
			Direct Register	
		+		offset
	00		direct address	
then:	00		(direct address)	
	+	DBR		
	base address			
	+			Y Reg
Operand Address:	effective address			

8. Direct Indirect Long Indexed—[d],y

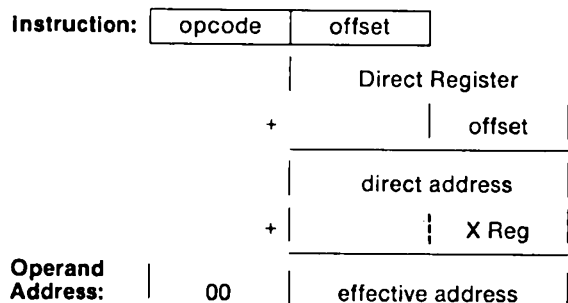
With this addressing mode, the 24-bit base address is pointed to by the sum of the second byte of the instruction and the Direct Register. The effective address is this 24-bit base address plus the Y Index Register.

ADDRESSING MODES (Cont.)

9. Direct Indexed Indirect—(d,x)

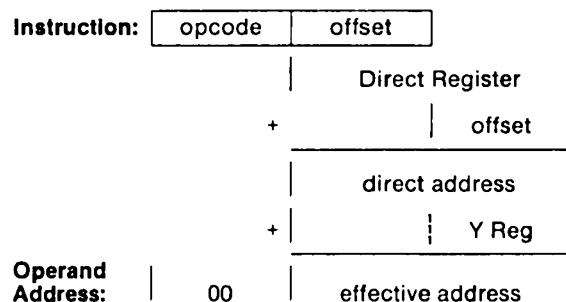
This address mode is often referred to as Indirect,X. The second byte of the instruction is added to the sum of the Direct Register and the X Index Register. The result points to the low-order 16 bits of the effective address. The Data Bank Register contains the high-order 8 bits of the effective address.


10. Direct Indexed With X—d,x

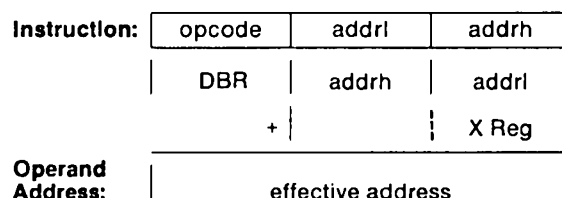
The second byte of the instruction is added to the sum of the Direct Register and the X Index Register to form the 16-bit effective address. The operand is always in Bank 0.


11. Direct Indexed With Y—d,y

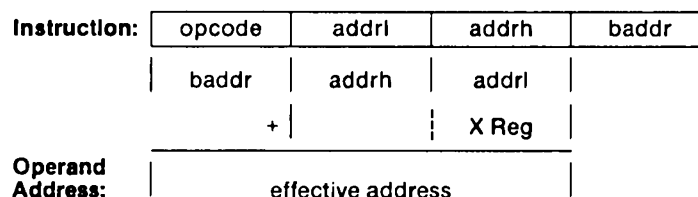
The second byte of the instruction is added to the sum of the Direct Register and the Y Index Register to form the 16-bit effective address. The operand is always in Bank 0.


12. Absolute Indexed With X—a,x

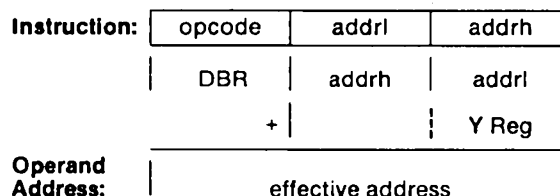
The second and third bytes of the instruction are added to the X Index Register to form the low-order 16 bits of the effective address. The Data Bank Register contains the high-order 8 bits of the effective address.


13. Absolute Long Indexed With X—al,x

The second, third and fourth bytes of the instruction form a 24-bit base address. The effective address is the sum of this 24-bit address and the X Index Register.


14. Absolute Indexed With Y—a,y

The second and third bytes of the instruction are added to the Y Index Register to form the low-order 16 bits of the effective address. The Data Bank Register contains the high-order 8 bits of the effective address.


15. Program Counter Relative—r

This address mode, referred to as Relative Addressing, is used only with the Branch instructions. If the condition being tested is met, the second byte of the instruction is added to the Program Counter, which has been updated to point to the opcode of the next instruction. The offset is a signed 8-bit quantity in the range from -128 to 127. The Program Bank Register is not affected.

16. Program Counter Relative Long—rl

This address mode, referred to as Relative Long Addressing, is used only with the Unconditional Branch Long instruction (BRL) and the Push Effective Relative instruction (PER). The second and third bytes of the instruction are added to the Program Counter, which has been updated to point to the opcode of the next instruction. With the branch instruction, the Program Counter is loaded with the result. With the Push Effective Relative instruction, the result is stored on the stack. The offset is a signed 16-bit quantity in the range from -32768 to 32767. The Program Bank Register is not affected.

ADDRESSING MODES (Cont.)

17. Absolute Indirect—(a)

The second and third bytes of the instruction form an address to a pointer in Bank 0. The Program Counter is loaded with the first and second bytes at this pointer. With the Jump Long (JML) instruction, the Program Bank Register is loaded with the third byte of the pointer.

Instruction:	opcode	addrl	addrh
Indirect Address =		00	addrh addrl
New PC = (indirect address)			
with JML:			
New PC = (indirect address)			
New PBR = (indirect address +2)			

18. Direct Indirect—(d)

The second byte of the instruction is added to the Direct Register to form a pointer to the low-order 16 bits of the effective address. The Data Bank Register contains the high-order 8 bits of the effective address.

Instruction:	opcode	offset
		Direct Register
		+ offset
	00	direct address
then:		
	00	(direct address)
	+ DBR	
Operand Address:		effective address

19. Direct Indirect Long—[d]

The second byte of the instruction is added to the Direct Register to form a pointer to the 24-bit effective address.

Instruction:	opcode	offset
		Direct Register
		+ offset
	00	direct address
then:		
Operand Address:		(direct address)

20. Absolute Indexed Indirect—(a,x)

The second and third bytes of the instruction are added to the X Index Register to form a 16-bit pointer in Bank 0. The contents of this pointer are loaded in the Program Counter. The Program Bank Register is not changed.

Instruction:	opcode	addrl	addrh
		addrh	addrl
			X Reg
	PBR		address
then:			
			PC = (address)

21. Stack—s

Stack addressing refers to all instructions that push or pull data from the stack, such as Push, Pull, Jump to Subroutine, Return from Subroutine, Interrupts, and Return from Interrupt. The bank address is always 0. Interrupt Vectors are always fetched from Bank 0.

22. Stack Relative—d,s

The low-order 16 bits of the effective address is formed from the sum of the second byte of the instruction and the Stack Pointer. The high-order 8 bits of the effective address is always zero. The relative offset is an unsigned 8-bit quantity in the range of 0 to 255.

Instruction:	opcode	offset
		Stack Pointer
		+ offset
Operand Address:	00	effective address

23. Stack Relative Indirect Indexed—(d,s),y

The second byte of the instruction is added to the Stack Pointer to form a pointer to the low-order 16-bit base address in Bank 0. The Data Bank Register contains the high-order 8 bits of the base address. The effective address is the sum of the 24-bit base address and the Y Index Register.

Instruction:	opcode	offset
		Stack Pointer
		+ offset
	00	S + offset
then:		
		S + offset
	+ DBR	
		base address
		+ Y Reg
Operand Address:		effective address

24. Block Source Bank, Destination Bank—xyc

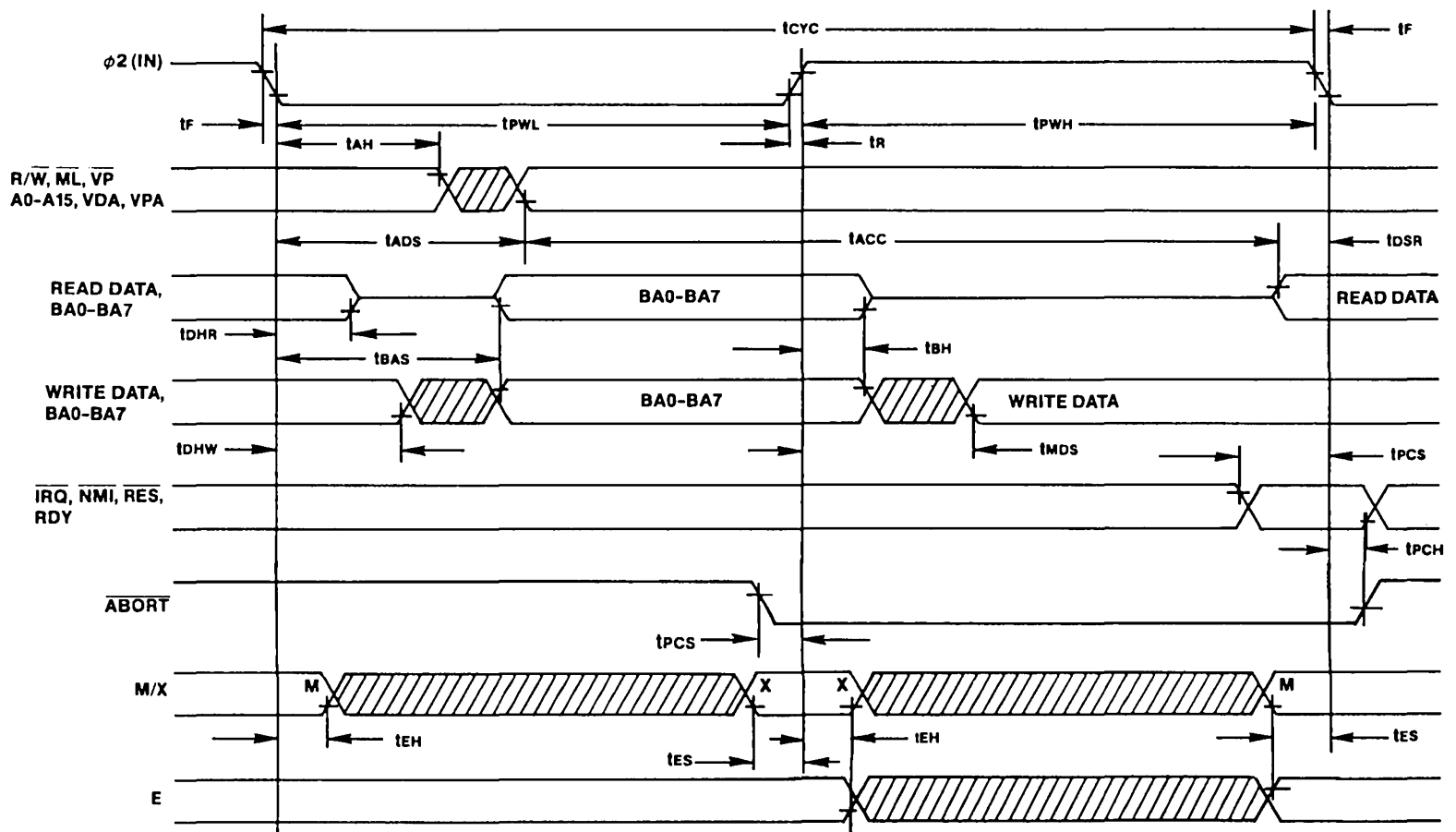
This addressing mode is used by the Block Move instructions. The second byte of the instruction contains the high-order 8 bits of the destination address. The Y index Register contains the low-order 16 bits of the destination address. The third byte of the instruction contains the high-order 8 bits of the source address. The X Index Register contains the low-order 16 bits of the source address. The C Accumulator contains one less than the number of bytes to move. The second byte of the block move instructions is also loaded into the Data Bank Register.

Instruction:	opcode	dstbnk	srcbnk
		dstbnk	DBR
Source Address:		srcbnk	X Reg
Destination Address:		DBR	Y Reg

Increment (MVN) or decrement (MVP) X and Y.
Decrement C (if greater than zero), then PC+3 → PC.

TABLE 11. VL65C816 TIMING CHARACTERISTICS $T_A = 0^\circ\text{C to } 70^\circ\text{C}$, $V_{DD} = 5.0\text{ V} \pm 5\%$

Parameter	Symbol	2 MHz		4 MHz		6 MHz		8 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Cycle Time	t _{CYC}	500	DC	250	DC	167	DC	125	DC	nS
Clock Pulse Width Low	t _{PWL}	0.240	10	0.120	10	0.080	10	0.060	10	μS
Clock Pulse Width High	t _{PWH}	240	∞	120	∞	80	∞	60	∞	nS
Fall Time, Rise Time	t _F , t _R	—	10	—	10	—	5	—	5	nS
A0-A15 Hold Time	t _{AH}	10	—	10	—	10	—	10	—	nS
A0-A15 Setup Time	t _{ADS}	—	100	—	75	—	60	—	40	nS
BA0-BA7 Hold Time	t _{BH}	10	—	10	—	10	—	10	—	nS
BA0-BA7 Setup Time	t _{BAS}	—	100	—	90	—	65	—	45	nS
Access Time	t _{ACC}	365	—	130	—	87	—	70	—	nS
Read Data Hold Time	t _{DHR}	10	—	10	—	10	—	10	—	nS
Read Data Setup Time	t _{DSR}	40	—	30	—	20	—	15	—	nS
Write Data Delay Time	t _{MDS}	—	100	—	70	—	60	—	40	nS
Write Data Hold Time	t _{DHW}	10	—	10	—	10	—	10	—	nS
Processor Control Setup Time	t _{PCS}	40	—	30	—	20	—	15	—	nS
Processor Control Hold Time	t _{PCH}	10	—	10	—	10	—	10	—	nS
E,MX Output Hold Time	t _{EH}	10	—	10	—	5	—	5	—	nS
E,MX Output Setup Time	t _{ES}	50	—	50	—	25	—	15	—	nS
Capacitive Load (Address, Data, and R/W)	C _{EXT}	—	100	—	100	—	35	—	35	pF
BE to High Impedance State	t _{BHZ}	—	30	—	30	—	30	—	30	nS
BE to Valid Data	t _{BVD}	—	30	—	30	—	30	—	30	nS

FIGURE 3. VL65C816 TIMING DIAGRAM




USER INFORMATION

STACK ADDRESSING

When in the Native mode, the Stack Register may use memory locations 000000 to 00FFFF. The effective address of Stack, Stack Relative and Stack Relative Indirect Indexed addressing modes is always within this range. In the Emulation mode, the Stack address range is 000100 to 0001FF. The following opcodes and addressing modes increment or decrement beyond this range when accessing two or three bytes:

JSL; JSR(a,x); PEA; PEI; PER;
PHD; PLD; RTL; d,s; (d,s),y

DIRECT ADDRESSING

The Direct Addressing modes are often used to access memory registers and pointers. The effective address generated by Direct, Direct X, and Direct Y, addressing modes are always in the Native mode range 000000 to 00FFFF. When in the Emulation mode, the Direct addressing range is 000000 to 0000FF, except for [Direct] and [Direct] Y addressing modes and the PEI instruction, which increment from 0000FE or 0000FF into Stack area.

When in the Emulation mode and DH is not equal to zero, the Direct addressing range is 00DH00 to 00DHFF, except for [Direct] and [Direct] Y addressing modes and the PEI instruction which increment from 00DHFE or 00DHFF into the next higher page.

When in the Emulation mode and DL is not equal to zero, the direct addressing range is 000000 to 00FFFF.

ABSOLUTE INDEXED ADDRESSING

The Absolute Indexed addressing modes are used to address data outside the Direct addressing range. The 65C02 addressing range is 0000 to FFFF. Indexing from page FFFX may result in a 00YY data fetch when using the VL65C02. In contrast, indexing from page ZZFFFX may result in ZZ+1,00YY when using the VL65C816.

ABORT INPUT (VL65C816 ONLY)

ABORT should be held low for a period not to exceed one cycle. Also, if ABORT is held low during the Abort Interrupt sequence, the Abort Interrupt

will be aborted. It is not recommended to abort the Abort Interrupt. The ABORT internal latch is cleared during the second cycle of the Abort Interrupt. Asserting the ABORT input after the following instruction cycles causes registers to be modified:

- Read-Modify-Write: Processor Status Register modified if ABORT is asserted after a modify cycle.
- RTI: Processor Status Register modified if ABORT is asserted after cycle 3.
- IRQ, NMI, ABORT BRK, COP: When ABORT is asserted after cycle 2, PBR and DBR become 00 (Emulation mode) or PBR becomes 00 (Native mode).

The Abort Interrupt has been designed for virtual memory systems. For this reason, asynchronous ABORTs may cause undesirable results due to the above conditions.

VDA AND VPA

When VDA or VPA are high and during all write cycles, the Address Bus is always valid. VDA and VPA should be used to qualify all memory cycles. Note that when VDA and VPA are both low, invalid addresses may be generated. The Page and Bank addresses could also be invalid. This will be due to low-byte addition only. The cycle when only low-byte addition occurs is an optional cycle for instructions that read memory when the Index Register consists of eight bits. This optional cycle becomes a standard cycle for the Store instruction, all instructions using the 16-bit Index Register mode, and the Read-Modify-Write instruction when using 8- or 16-bit Index Register modes.

APPLE II, IIe, IIc, AND II+ DISK SYSTEMS

VDA and VPA should not be used to qualify addresses during disk operation on Apple systems. Consult your Apple representative for hardware/software configurations.

DB/BA OPERATION (WHEN RDY IS PULLED LOW)

When RDY is low, the Data Bus is held in the data transfer state (i.e., $\sigma 2$ high). The Bank address external transparent latch should be latched when the $\sigma 2$ clock or RDY is low.

M/X OUTPUT

The M/X output reflects the value of the M and X bits of the processor Status Register. The REP, SEP, and PLP instructions may change the state of the M and X bits. Note that the M/X output is invalid during the instruction cycle following REP, SEP, and PLP instruction execution. This cycle is used as the opcode fetch cycle of the next instruction.

INSTRUCTIONS

Opcodes - It should be noted that all opcodes function in all modes of operation. The following instructions have limited use in the Emulation mode:

- The REP and SEP instructions cannot modify the M and X bits when in the Emulation mode. In this mode the M and X bits are always high (logic 1).
- When in the Emulation mode, the MVP and MVN instructions use the X and Y Index Registers for the memory address. Also, the MVP and MVN instructions can only move data within the memory range 0000 (Source Bank) to 00FF (Destination Bank).

Indirect Jumps - The JMP (a) and JML (a) instructions use the direct Bank for indirect addressing, while JMP (a,x) and JSR (a,x) use the Program Bank for indirect address tables.

Switching Modes - When switching from the Native mode to the Emulation mode, the X and M bits of the Status Register are set high (logic 1), the high byte of the Stack is set to 01, and the high bytes of the X and Y Index Registers are set to 00. To save previous values, these bytes must always be stored before changing modes. Note that the low byte of the S, X, and Y Registers and the low and high bytes of the Accumulator (A and B) are not affected by a mode change.

How hardware interrupts, BRK, and COP instructions affect the Program Bank and the Data Bank Registers, when in the Native mode, the Program Bank register (PBR) is cleared to 00 when a hardware interrupt, BRK or COP is executed. In the Native mode, the previous PBR contents are automatically saved.

USER INFORMATION (CONT.)

Note that a Return from Interrupt (RTI) should always be executed from the same mode that originally generated the interrupt.

Binary Mode-The Binary mode is set whenever a hardware or software interrupt is executed. The D flag within the Status Register is cleared to zero.

WAI Instruction-The WAI instruction pulls RDY low and places the processor in the WAI low-power mode. $\overline{\text{NMI}}$, $\overline{\text{IRQ}}$, or $\overline{\text{RESET}}$ terminate the WAI condition and transfer control to the interrupt handler routine. Note that an $\overline{\text{ABORT}}$ input aborts the WAI instruction, but does not restart the processor. When the Status Register 1 flag is set ($\overline{\text{IRQ}}$ disabled), the $\overline{\text{IRQ}}$ interrupt causes the next instruction (following the WAI instruction) to be executed without going to the $\overline{\text{IRQ}}$ interrupt handler. This method results in the highest speed response to an $\overline{\text{IRQ}}$ input. When an interrupt is received after an $\overline{\text{ABORT}}$ that occurs during the WAI instruction, the processor returns to the WAI instruction. Other than $\overline{\text{RES}}$ (highest priority), $\overline{\text{ABORT}}$ is the next-highest priority, followed by $\overline{\text{NMI}}$ or $\overline{\text{IRQ}}$ interrupts.

STP Instruction-The STP instruction

disables the $\phi 2$ clock to all circuitry. When disabled, the $\phi 2$ clock is held in the high state. In this case, the Data Bus remains in the data transfer state and the Bank address is not multiplexed onto the Data Bus. Upon executing the STP instruction, the $\overline{\text{RES}}$ signal is the only input that can restart the processor. The processor is restarted by enabling the $\phi 2$ clock, which occurs on the falling edge of the $\overline{\text{RES}}$ input. Note that the external oscillator must be stable and operating properly before $\overline{\text{RES}}$ goes high.

COP Signatures - Signatures 00-7F may be user defined, while signatures 80-FF are reserved.

RDY Pulled During Write-The NMOS 6502 does not stop during a write operation. In contrast, both the 65C02 and the VL65C816 do stop during write operations.

MVN and MVP effects on the Data Bank Register - The MVN and MVP instructions change the Data Bank Register to the value of the second byte of the instruction (destination bank address).

INTERRUPTS

Interrupt Priorities - The following interrupt priorities are in effect should

more than one interrupt occur at the same time:

$\overline{\text{RES}}$	Highest
$\overline{\text{ABORT}}$	
$\overline{\text{NMI}}$	
$\overline{\text{IRQ}}$	Lowest

TRANSFERS

Transfers from 8-bit to 16-bit, or 16-bit to 8-bit, Registers - All transfers from one register to another result in a full 16-bit output from the source register. The Destination Register size determines the number of bits actually stored in the destination register and the values stored in the processor Status Register. The following are always 16-bit transfers, regardless of the accumulator size:

TCS; TSC; TCD; TDC

Stack Transfers - When in the Emulation mode, a 01 is forced into SH. In this case, the B Accumulator is not loaded into SH during a TCS instruction. When in the Native mode, the B Accumulator is transferred to SH. Note that in both the Emulation and Native modes, the full 16 bits of the Stack Register are transferred to the A, B, and C Accumulators, regardless of the state of the M bit in the Status Register.

DC CHARACTERISTICS: $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{DD} = 5\text{ V} \pm 5\%$

Parameter	Symbol	Min	Max	Unit
Input High Voltage RES, RDY, IRQ, Data, BE, $\phi 2$ (IN), NMI, ABORT	V_{IH}	2.0 0.7 V_{DD}	$V_{DD} + 0.3$ $V_{DD} + 0.3$	V V
Input Low Voltage RES, RDY, IRQ, Data, BE, $\phi 2$ (IN), NMI, ABORT	V_{IL}	-0.3 -0.3	0.8 0.2	V V
Input Leakage Current ($V_{IN} = 0$ to V_{DD}) RES, NMI, RDY, IRQ, BE, ABORT (Internal Pullup) $\phi 2$ (IN) Address, Data, R/W (Off State, BE = 0)	I_{IN}	-100 -1 -10	1 1 10	μA μA μA
Output High Voltage ($I_{OH} = -100\mu\text{A}$) Data, Address, R/W, ML, VP, M/X, E, VDA, VPA, $\phi 2$ (OUT)	V_{OH}	0.7 V_{DD}	—	V
Output Low Voltage ($I_{OL} = 1.6\text{mA}$) Data, Address, R/W, ML, VP, M/X, E, VDA, VPA, $\phi 2$ (OUT)	V_{OL}	—	0.4	V
Supply Current (No Load)	I_{DD}	—	4	mA/MHz
Standby Current (No Load, Data Bus = V_{SS} or V_{DD}) RES, NMI, IRQ, BE, ABORT, $\phi 2 = V_{DD}$)	I_{SB}	—	10	μA
Capacitance ($V_{IN} = 0\text{V}$, $T_A = 25^\circ\text{C}$, $f = 2\text{ MHz}$) Logic, $\phi 2$ (IN) Address, Data, R/W (Off State)	C_{IN} C_{TS}	— —	10 15	pF pF

ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	0°C to +70°C	Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device under these or any conditions other than those indicated in this data sheet is not implied. Exposure to absolute maximum rating	conditions for extended periods may affect device reliability. This device contains input protection against damage due to high static voltages or electric fields. However, precautions should be taken to avoid application of voltages higher than the maximum rating.
Storage Temperature	-55°C to +150°C		
Supply Voltage to Ground Potential	-0.3 V to +7.0 V		
Applied Input Voltage	-0.3 V to VDD+ 0.3 V		

DOUBLE-DENSITY FLOPPY DISK CONTROLLER (DDFDC)

FEATURES

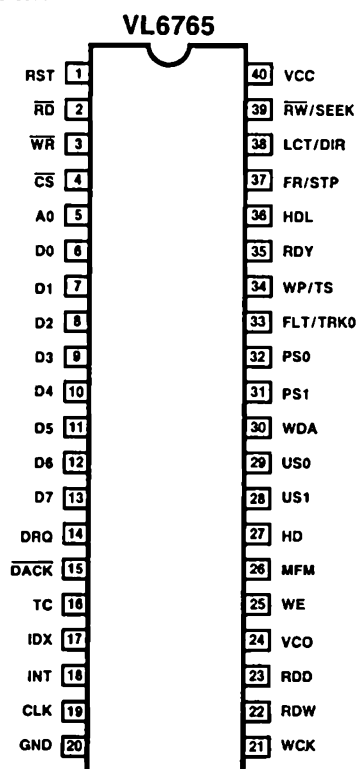
- Address mark detection circuitry
- Software control of
 - Track stepping rate
 - Head load time
 - Head unload time
- IBM compatible in both single- and double-density format
- Programmable data record lengths: 128, 256, 512, 1024, 2048, 4096 or 8192 bytes/sector
- Multi-sector and multi-track transfer capability
- Controls up to four floppy disk drives
- Data scan capability—will scan a single sector or an entire track of data fields, comparing on a byte-by-byte basis data in the processor's memory with data read from the disk
- Data transfers in DMA or non-DMA mode
- Parallel seek operations on up to four drives
- Directly compatible with an 8-bit or 16-bit synchronous microprocessor bus including Z-80/8080A/8085A, 8086, and 8088
- Replaces the NEC μ PD765A, Intel 8272A, and Rockwell 6765A
- Single phase 4 or 8 MHz clock
- Single +5 volt power supply

DESCRIPTION

The VL6765 Double-Density Floppy Disk Controller (DDFDC) interfaces up to four floppy disk drives to an 8-bit or 16-bit microprocessor-based system including Z80, 8080A, 8085A, 8086, and 8088. The DDFDC simplifies the system design by minimizing both the number of external hardware components and software steps needed to implement the floppy disk drive (FDD) interface. Control signals supplied by the DDFDC reduce the number of components required in external phase locked loop and write precompensation circuitry. Memory-mapped registers containing commands, status and data simplify the software interface. Built-in functions reduce the software overhead needed to control the FDD interface. The DDFDC supports both the IBM 3740 Single-Density (FM) and IBM System 34 Double-Density (MFM) formats.

The DDFDC interfaces directly to the synchronous microprocessor bus and operates with 8-bit byte length data transferred on the bus in either DMA or non-DMA mode. In DMA mode, the CPU need only load the command into the DDFDC and all data transfers occur under DMA control. The VL6765 is directly compatible with the Z8410/ μ PD8257 Direct Memory Access Controller (DMAC). In non-DMA mode, the DDFDC generates an interrupt to the CPU indicating that a byte of data is available.

PIN DIAGRAM



ORDER INFORMATION

Part Number	Clock Frequency	Package
VL6765-04PC VL6765-04CC VL6765-04QC	4 MHz	Plastic DIP Ceramic DIP Plastic Leaded Chip Carrier (PLCC)
VL6765-08PC VL6765-08CC VL6765-08QC	8 MHz	Plastic DIP Ceramic DIP Plastic Leaded Chip Carrier (PLCC)

Note:

Operating temperature range: 0°C to +70°C.



PIN DIAGRAM

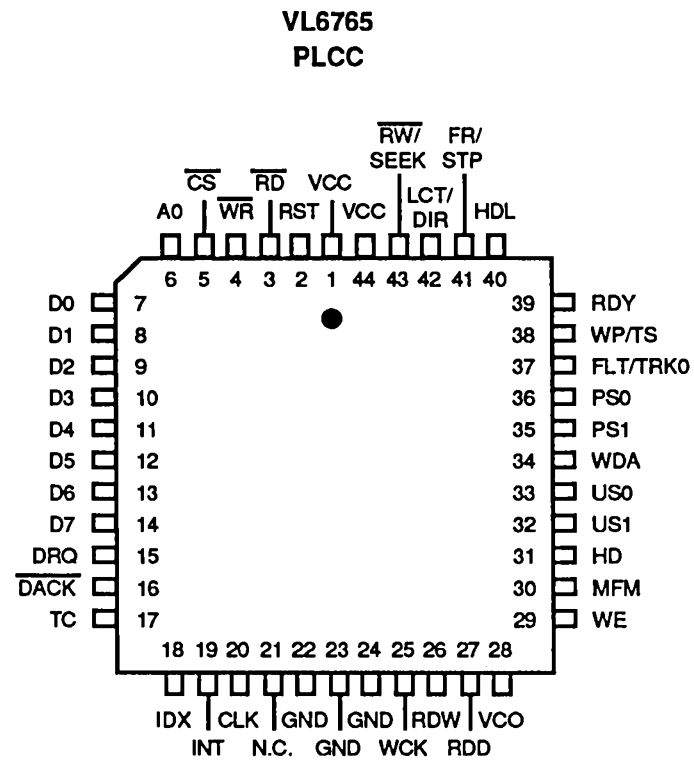
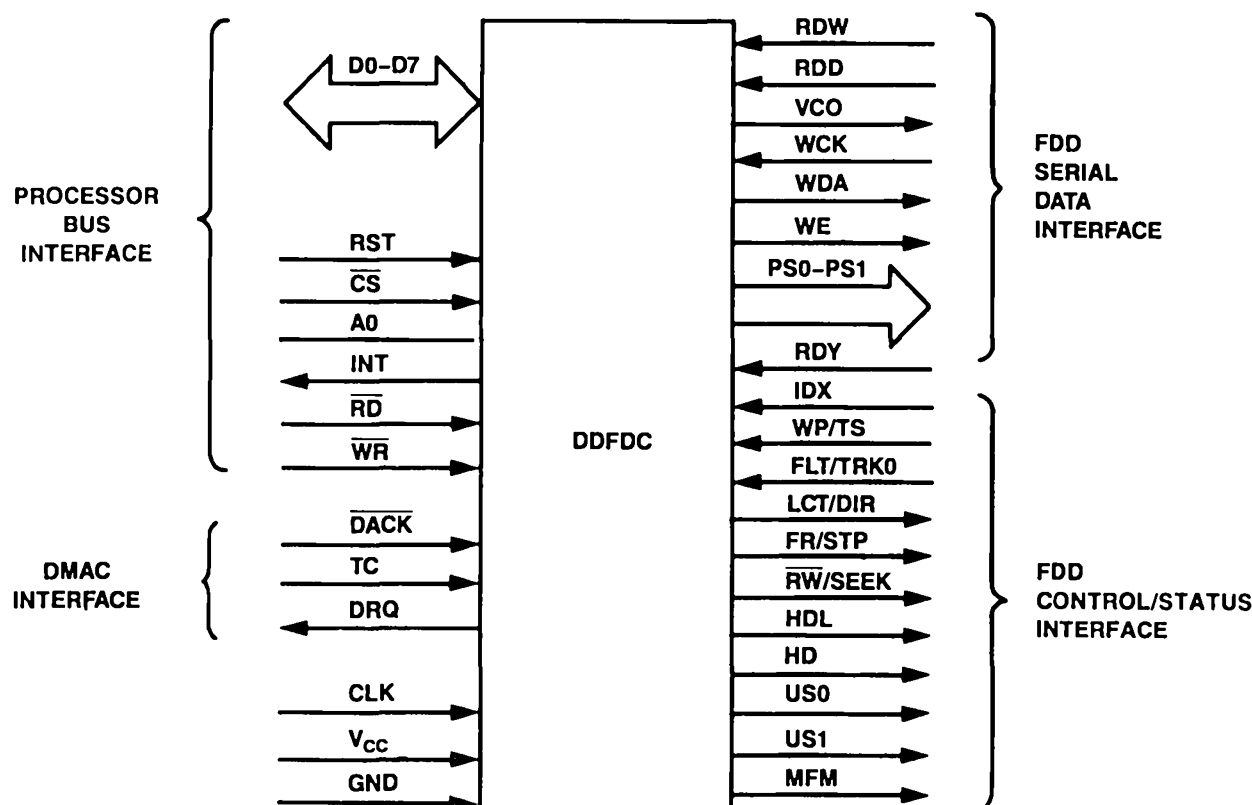


Figure 1. DDFDC Input and Output Signals



PIN DESCRIPTION

Throughout this document signals are presented using the terms active and inactive, or asserted and negated, independent of whether the signal is active in the high-voltage state or low-voltage state. (The active state of each logic pin is described below.) Active low signals are denoted by a superscript bar.

BUS INTERFACE

D0-D7—Data Lines. The bidirectional data lines transfer data between the DDFDC and the 8-bit data bus.

CLK—CLOCK. The clock is a TTL compatible 4 or 8 MHz square wave signal.

RST—RESET. This active high input places the DDFDC in the idle state and resets the output lines to the floppy disk drive (FDD) to the low state. RST does not affect the Step Rate Time (SRT), Head Unload Time (HUT) or Head Load Time (HLT) set by a Specify command. If RDY goes high while RST is high, the DDFDC will assert INT within 1.024 ms. This interrupt can be cleared by issuing a Sense Interrupt Status command.

CS—Chip Select. The DDFDC is selected when the $\overline{\text{CS}}$ input is low.

A0—Data/Status Register Select. This input selects the Data or Status Register for reading from or writing to. When A0 = high, the Data Register is selected and the state of $\overline{\text{RD}}$ or $\overline{\text{WR}}$ determines whether it is a read ($\overline{\text{RD}}$ = low) or a write ($\overline{\text{WR}}$ = low)

operation. When A0 = low, the Status Register is selected. This register may only be read ($\overline{\text{RD}}$ = low); the state $\overline{\text{WR}}$ = low is invalid when the Status Register is selected.

INT—Interrupt Request. This active high output is the interrupt request generated by the DDFDC to the CPU. INT is asserted upon completion of some DDFDC commands and before a data byte is transferred between the DDFDC and the data bus (in the Non-DMA mode).

$\overline{\text{RD}}$ —Read. This active low input defines the data bus transfer as a read cycle. When low, the data transfer is from the DDFDC to the data bus.

$\overline{\text{WR}}$ —Write. This active low input defines the data bus transfer as a write cycle. When low, the data transfer is from the data bus to the DDFDC.

DIRECT MEMORY ACCESS CONTROLLER (DMAC) INTERFACE

$\overline{\text{DACK}}$ —DMA Acknowledge. The DMA transfer acknowledge signal is a TTL compatible input generated by the DMA controller (DMAC) controlling the DDFDC. The DMA cycle is active when $\overline{\text{DACK}}$ is low and the DDFDC is performing a DMA transfer.

DRQ—Data DMA Request. The transfer request signal is a TTL compatible output generated by the DDFDC to request a data transfer operation under control of the DMAC (in the DMA mode). The request is active when $\overline{\text{DRQ}}$ = high. The signal is reset inactive when DMA Acknowledge ($\overline{\text{DACK}}$) is asserted (low).

TC—Terminal Count. This input signal is issued to the DDFDC when the DMA transfer for a channel is complete. The signal is active high concurrent with the $\overline{\text{DACK}}$ input when the DMA operation is complete as a result of that transfer.

FDD SERIAL DATA INTERFACE

RDD—Read Data. Read Data input from the floppy disk drive (FDD) containing clock and data bits.

RDW—Read Data Window. Data Window input generated by the Phase Locked Loop (PLL) and used to sample data from the FDD.

VCO—Voltage Controlled Oscillator Sync. This output signal inhibits the VCO in the PLL circuit when low and enables the VCO in the PLL circuit when high. This inhibits RDD and RDW from being generated until valid data is detected from the FDD.

WCK—Write Clock. This input clock determines the Write Data rate to the FDD. The data rate is 500 KHz in the FM mode (MFM = low) and 1 MHz in the MFM mode (MFM = high). The pulse width is 250 ns (typical) in both modes.

WDA—Write Data. Serial write data output to the FDD containing both clock and data bits.

WE—Write Enable. This output signal enables the Write Data into the FDD when high.

PS0-PS1—Preshift. These outputs are encoded to convey write compensation status during the MFM mode to determine early, late or normal times as follows:

Write Precompensation Status	Preshift Outputs	
	PS0	PS1
Normal	0	0
Late	0	1
Early	1	0
Invalid	1	1

0 = Low, 1 = High

FDD STATUS INTERFACE

RDY—Ready. An active high input signal indicates the FDD is ready to send data to, or receive data from, the DDFDC.

IDX—Index. An active high input signal from the FDD indicates the index hole is under the index sensor. Index is used to synchronize DDFDC timing.

RW/SEEK—Read Write/Seek. Mode selection signal to the FDD which controls the multiplexer from the multiplexed signals. When $\overline{\text{RW/SEEK}}$ is low, the Read/Write mode is commanded; when $\overline{\text{RW/SEEK}}$ is high, the Seek mode is commanded.

$\overline{\text{RW/SEEK}}$	Mode	Active FDD Interface Signals
Low	Read/Write	WP, FLT, LCT, FR
High	Seek	TS, TRK0, DIR, STP

WP/TS—Write Protect/Two Side. An active high multiplexed input signal from the FDD. In the Read/Write mode, WP/TS high indicates the media is write-protected. In the Seek mode, WP/TS high indicates the media is two-sided.

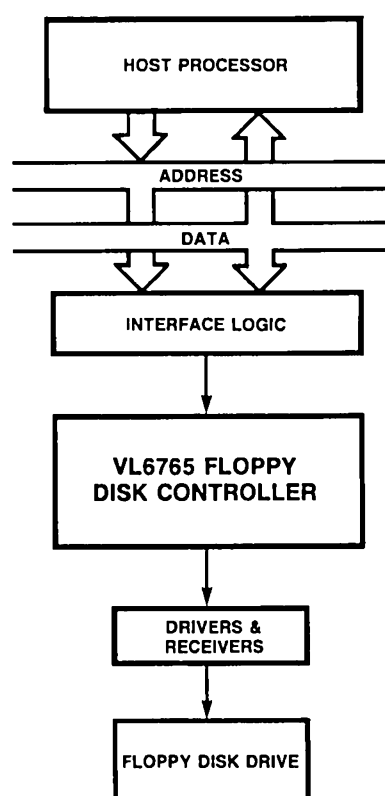
FLT/TRK0—Fault/Track Zero. An active high multiplexed input from the FDD. In the Read/Write mode ($\overline{\text{RW/SEEK}}$ = low), FLT/TRK0 high indicates an FDD fault. In the Seek mode, FLT/TRK0 high indicates that the read/write head is positioned over track zero.

LCT/DIR—Low Current/Direction. A multiplexed output to the FDD. In the Read/Write mode, LCT/DIR is low when the read/write head is to be positioned over the inner tracks and the LCT/DIR is high when the head is to be positioned over the outer tracks. In the Seek mode, LCT/DIR controls the head direction. When LCT/DIR is high, the head steps to the outside of the disk; when LCT/DIR is low, the head steps to the inside of the disk.

FR/STP—Fault Reset/Step. A multiplexed output to the FDD. In the Read/Write mode, FR/STP high resets the fault indicator in the FDD. An FR pulse is issued at the beginning of each read or write command prior to issuing HDL. In the Seek mode, FR/STP provides the step pulses to move the read/write head to another track in the direction indicated by the LCT/DIR signal.

HDL—Head Load. An active high output to notify the FDD that the read/write head should be loaded (placed in contact with the media). A low level indicates the head should be unloaded.

Figure 2. Typical VL6765 Application



HD—Head Select. An output to the FDD to select the proper read/write head. Head One is selected when HD = high and Head Zero is selected when HD = low.

US0-US1—Unit Select. Output signals for floppy disk drive selection as follows:

Unit Select		Floppy Disk Drive Select
US0	US1	
0	0	0
0	1	1
1	0	2
1	1	3

0 = Low, 1 = High

MFM—MFM Mode. Output signal to the FDD to indicate MFM or FM mode. Selects the MFM mode when MFM = high and the FM mode MFM = Low.

VCC—Power. +5 Vdc.

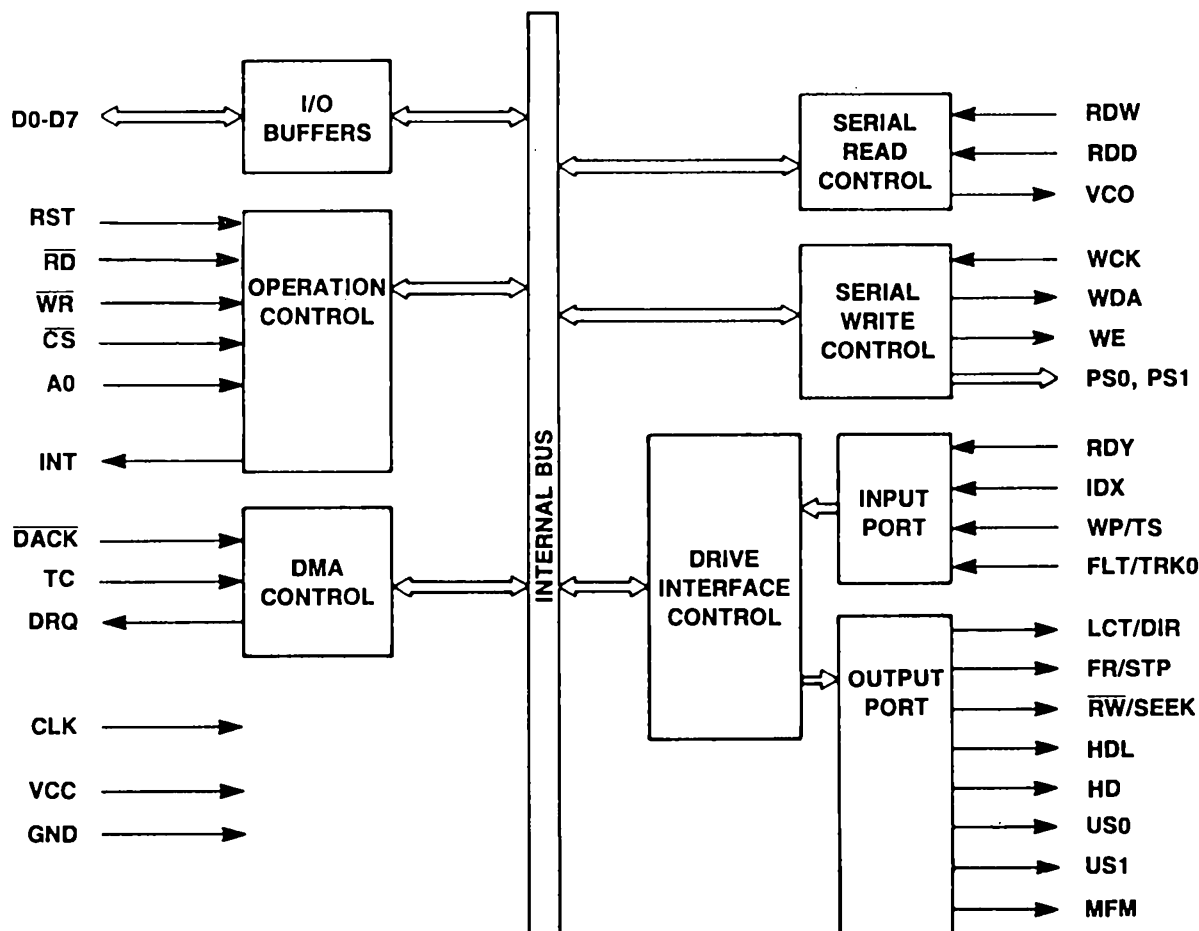
GND—Ground (V_{ss}).

DDFDC REGISTERS

The DDFDC contains six registers which may be accessed by the processor or DMA controller via the system (i.e., micro-processor) bus: a Main Status Register, a Data Register, and four Result Status Registers. The 8-bit Main Status Register (MSR) contains the status information of the DDFDC, and may be accessed at any time. The 8-bit Data Register, consisting of several registers in a stack with only one register presented to the data bus at a time, stores data, commands, parameters and FDD status information. Bytes of data are read out of, or written into, the Data Register in order to initiate a command or to obtain the results of a command execution.

The read-only Main Status Register facilitates the transfer of data between the system and the DDFDC. The other Status Registers (ST0, ST1, ST2 and ST3) are only available during the result phase, and may be read only after completing a command. The particular command which has been executed determines how many of the Status Registers will be read.

Figure 3. DDFDC Block Diagram



The relationship between the status/data registers and the \overline{WR} , \overline{RD} and A0 signals is shown below.

A0	\overline{RD}	\overline{WR}	Function
0	0	0	Illegal
0	0	1	Read Main Status Register
0	1	0	Illegal
1	0	0	Illegal
1	0	1	Read from Data Register
1	1	0	Write into Data Register

0 = Low, 1 = High

Table 1 shows each of the status registers used by the DDFDC and each bit assignment within the individual registers. Table 2 defines the symbols used throughout the command definitions. Each register bit symbol is defined in the register descriptions that follow Table 2.

REGISTER DEFINITIONS

Main Status Register (MSR)

7	6	5	4	3	2	1	0
RQM	DIO	EXM	CB	D3B	D2B	D1B	D0B

The Main Status Register (MSR) contains the status information of the DDFDC, and must be read by the processor before each byte is written to, or read from, the Data Register during the command or result phase. MSR reads are not required during the execution phase. The Data Input/Output (DIO) and Request for Master (RQM) bits in the MSR indicate when data is ready and in which direction data will be transferred on the data bus. The maximum time between the last \overline{RD} or \overline{WR} during command or result phases and the DIO and RQM getting set or reset is 12 μ s. For this reason, every time the MSR is read the processor should wait 12 μ s. The maximum time from the trailing edge of the last \overline{RD} in the result phase to when bit 4 (DDFDC Busy) goes low is also 12 μ s.

The DIO and RQM timing chart is shown in Figure 4.

MSR

- 7 RQM —Request for Master.**
 0 Data Register is not ready.
 1 Data Register is ready.

MSR

- 6 DIO —Data Input/Output.**
 0 Data transfer is from system to the Data Register.
 1 Data transfer is from Data Register to the system.

MSR

- 5 EXM —Execution Mode. (Non-DMA mode only).**
 0 Execution phase ended, result phase begun.
 1 Execution phase started.

MSR

- 4 CB —Controller (DDFDC) Busy.**
 0 DDFDC is not busy, will accept a command.
 1 DDFDC is busy, will not accept a command.

MSR

- 3 D3B —Floppy Disk Drive (FDD) 3 Busy.**
 0 FDD 3 is not busy, DDFDC will accept read or write command.
 1 FDD 3 is busy, DDFDC will not accept read or write command.

MSR

- 2 D2B —FDD 2 Busy.**
 0 FDD 2 is not busy, DDFDC will accept read or write command.
 1 FDD 2 is busy, DDFDC will not accept read or write command.

MSR

- 1 D1B —FDD 1 Busy.**
 0 FDD 1 is not busy, DDFDC will accept read or write command.
 1 FDD 1 is busy, DDFDC will not accept read or write command.

MSR

- 0 D0B —FDD 0 Busy.**
 0 FDD 0 is not busy, DDFDC will accept read or write command.
 1 FDD 0 is busy, DDFDC will not accept read or write command.

Status Register 0 (ST0)

7	6	5	4	3	2	1	0
IC		SE	EC	NR	HD	US	
						US1	US0

The Status Register 0 (ST0) as well as the other status registers (ST1-ST3), are available only during the result phase, and may be read only after completing a command. The particular command executed determines which status registers are used and may be read.

ST0

- 7 6 IC —Interrupt Code.**
 0 0 Normal Termination (NT). Command was properly executed and completed.
 0 1 Abnormal Termination (AT). Command execution was started, but was not successfully completed.
 1 0 Invalid Command (IC). Received command was invalid.
 1 1 Abnormal Termination (AT). The Ready (RDY) signal from the FDD changed state during command execution.

ST0

- 5 SE —Seek End.**
 0 Seek command is not completed.
 1 Seek command completed by DDFDC.

ST0

- 4 EC —Equipment Check.**
 0 No error.
 1 Either a fault signal is received from the FDD or the track 0 signal failed to occur after 256 step pulses (Recalibrate command).

Table 1. DDFDC Status Register Bit Assignments

	Bit Number							
	7	6	5	4	3	2	1	0
Main Status Register (MSR)	RQM	DIO	EXM	CB	D3B	D2B	D1B	D0B
Status Register 0 (ST0)	IC		SE	EC	NR	HD	US	
Status Register 1 (ST1)							US1	US0
Status Register 2 (ST2)	EN	0	DE	OR	0	ND	NW	MA
Status Register 3 (ST3)	0	CM	DD	WT	SH	SN	BT	MD
	FLT	WP	RDY	TRK0	TS	HD	US1	US0

Table 2. Command Symbol Description

Symbol	Name	Description
A0	Address Line A0	Controls selection of Main Status Register (A0 = low) or Data Register (A0 = high).
D	Data	The data pattern which is going to be written into a sector.
D0-D7	Data Bus	8-bit data bus, where D0 is the least significant data line and D7 is the most significant data line.
DTL	Data Length	When N is defined as 00, DTL is the number of data bytes to read from or write into the sector.
EOT	End of Track	The final sector number on a track. During read or write operation, the DDFDC stops data transfer after reading from or writing to the sector equal to EOT.
GPL	Gap Length	The length of Gap 3. During read/write commands this value determines the number of bytes that the VCO will stay low after two CRC bytes. During the Format a Track command it determines the size of Gap 3.
H	Head Address	Head number 0 or 1, as specified in ID field.
HD (H)	Head	A selected head number 0 or 1 which controls the polarity of pin 27. (H = HD in all command words).
HLT	Head Load Time	The head load time in the FDD (2 to 254 ms in 2 ms increments).
HUT	Head Unload Time	The head unload time after a read or write operation has occurred (16 to 240 ms in 16 ms increments).
MF	FM or MFM Mode	When MF = 0, FM mode is selected; and when MF = 1, MFM mode is selected.
MT	Multi-Track	When MT = 1, a multi-track operation is to be performed. After finishing a read/write operation on side 0, the DDFDC will automatically start searching for sector 1 on side 1.
N	Bytes/Sector	The number of data bytes written in a sector.
ND	Non-DMA Mode	When ND = 1, operation is in the Non-DMA mode; when ND = 0, operation is in the DMA mode.
NTN	New Track Number	A new track number, which will be reached as a result of the Seek command. Desired head position.
PTN	Present Track Number	The track number at the completion of Sense Interrupt Status command. Present head position.
R	Record (Sector)	The sector number to be read or written.
R/W	Read/Write	Either read (R) or write (W) signal.
ST	Sectors/Track	The number of sectors per track.
SK	Skip	Skip Deleted Data Address Mark.
SRT	Step Rate Time	The stepping rate for the FDD (1 to 16 ms in 1 ms increments). Stepping rate applies to all drives (F = 1 ms, E = 2 ms, etc.)
ST0 ST1 ST2 ST3	Status 0 Status 1 Status 2 Status 3	Four registers which store the status information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the Main Status Register (selected by A0 = low). ST0-ST3 may be read only after a command has been executed and contain information relevant to that particular command.
STP	Sector Test Process	During a Scan command, if STP = 01, the data in contiguous sectors is compared byte by byte with data sent from the processor (or DMA controller); and if STP = 02, then alternate sectors are read and compared.
T	Track Number	The current/selected track number of the medium (0-255).
US0,US1	Unit Select	A selected drive number (0-3).

ST0

- 3 NR** —Not Ready.
0 FDD is ready.
1 FDD is not ready at issue of read or write command. If a read or write command is issued to side 1 of a single-sided drive, this bit is also set.

ST0

- 2 HD** —Head Address. (At Interrupt).
0 Head Select 0.
1 Head Select 1.

ST0

- 1 0 US** —Unit Selected. (At Interrupt).
0 0 FDD 0 selected.
0 1 FDD 1 selected.
1 0 FDD 2 selected.
1 1 FDD 3 selected.

Status Register 1 (ST1)

7	6	5	4	3	2	1	0
EN	0	DE	OR	0	ND	NW	MA

ST1

- 7 EN** —End of Track.
0 No error.
1 DDFDC attempted to access a sector beyond the last sector of a track.

ST1

- 6** —Not Used. Always Zero.

ST1

- 5 DE** —Data Error.
0 No error.
1 DDFDC detected a CRC error in ID field or the Data field.

ST1

- 4 OR** —Overrun.
0 No error.
1 DDFDC was not serviced by the system during data transfers, within a predetermined time interval.

ST1

- 3** —Not Used. Always Zero.

ST1

- 2 ND** —No Data.
0 No error.
1 3 possible errors.
 1. DDFDC cannot find sector specified in the Internal Data Register (IDR) during execution of Read Data, Write Deleted Data or Scan commands.
 2. DDFDC cannot read ID field without an error during Read ID command.
 3. DDFDC cannot find starting sector during execution of Read a Track command.

ST1

- 1 NW** —Not Writable.
0 No error.
1 DDFDC detected a write protect signal from FDD during execution of Write Data, Write Deleted Data or Format a Track commands.

ST1

- 0 MA** —Missing Address Mark.
0 No error.
1 2 possible errors.
 1. DDFDC cannot detect the ID Address Mark after encountering the index hole twice.
 2. DDFDC cannot detect the Data Address Mark or Deleted Data Address Mark. The MD (Missing Address Mark in Data field) of Status Register 2 is also set.

Status Register 2 (ST2)

7	6	5	4	3	2	1	0
0	CM	DD	WT	SH	SN	BT	MD

ST2

- 7** —Not Used. Always Zero.

ST2

- 6 CM** —Control Mark.
0 No error.
1 DDFDC encountered a sector which contained a Deleted Data Address Mark during execution of a Read Data, Read a Track, or Scan command, or which contained a Data Address Mark during execution of a Read Deleted Data command.

ST2

- 5 DD** —Data Error in Data Field.
0 No error.
1 DDFDC detected a CRC error in the Data field.

ST2

- 4 WT** —Wrong Track.
0 No error.
1 Contents of T on the disk is different from that stored in IDR. Bit is related to ND (Bit 2) of Status Register 1.

ST2

- 3 SH** —Scan Equal Hit.
0 No "equal" condition during a scan command.
1 "Equal" condition satisfied during a scan command.

ST2

- 2 SN** —Scan Not Satisfied.
0 No error.
1 DDFDC cannot find a sector on the track which meets the scan command condition.

ST2

- 1 BT —Bad Track.**
0 No error.
1 Contents of T on the disk is different from that stored in the IDR and T = FF. Bit is related to ND (Bit 2) of Status Register 1.

ST2

- 0 MD —Missing Address Mark in Data Field.**
0 No error.
1 DDFDC cannot find a Data Address Mark or Deleted Data Address Mark during a data read from the disk.

Status Register 3 (ST3)

7	6	5	4	3	2	1	0
FLT	WP	RDY	TRK0	TS	HD	US1	US0

Status Register 3 (ST3) holds the results of the Sense Drive Status command.

ST3

- 7 FLT —Fault.**
0 Fault (FLT) signal from the FDD is low.
1 Fault (FLT) signal from the FDD is high.

ST3

- 6 WP —Write Protect.**
0 Write Protect (WP) signal from the FDD is low.
1 Write Protect (WP) signal from the FDD is high.

ST3

- 5 RDY —Ready.**
0 Ready (RDY) signal from the FDD is low.
1 Ready (RDY) signal from the FDD is high.

ST3

- 4 TRK0 —Track 0.**
0 Track 0 (TRK0) signal from the FDD is low.
1 Track 0 (TRK0) signal is from the FDD is high.

ST3

- 3 TS —Two Side.**
0 Two Side (TS) signal from the FDD is low.
1 Two Side (TS) signal from the FDD is high.

ST3

- 2 HD —Head Select.**
0 Head Select (HD) signal to the FDD is low.
1 Head Select (HD) signal to the FDD is high.

ST3

- 1 US1 —Unit Select 1.**
0 Unit Select 1 (US1) signal to the FDD is low.
1 Unit Select 1 (US1) signal to the FDD is high.

ST3

- 0 US0 —Unit Select 0.**
0 Unit Select 0 (US0) signal to the FDD is low.
1 Unit Select 0 (US1) signal to the FDD is high.

COMMAND SEQUENCE

The DDFDC is capable of performing 15 different commands. Each command is initiated by a multi-byte transfer of data from the system. After command execution, the result of the command may be a multi-byte transfer of data back to the system. Because of this multi-byte transfer of information between the DDFDC and the system, each command consists of three phases:

Command Phase—The DDFDC receives all information required to perform a particular operation from the system.

Execution Phase—The DDFDC performs the instructed operation.

Result Phase—After completion of the operation, status and other housekeeping information are made available to the system.

The bytes of data sent to the DDFDC to form a command, and read out of the DDFDC in the result phase, must occur in the order shown for each command sequence. That is, the command code byte must be sent first followed by the other bytes in the specified sequence. All command bytes must be written and all result bytes must be read in each phase. After the last byte of data in the command phase is received by the DDFDC, the execution phase starts. Similarly, when the last byte of data is read out in the result phase, the command is ended and the DDFDC is ready to accept a new command. A command can be terminated by asserting the Terminal Count (TC) signal to the DDFDC. This ensures that the processor can always get the DDFDC's attention even if the command in process hangs up in an abnormal manner.

COMMAND DESCRIPTION
READ DATA

A command set of nine bytes places the DDFDC into the Read Data mode. After the Read Data command has been received the DDFDC loads the head (if it is unloaded), waits the specified Head Settling Time (defined in the Specify command), then begins reading ID Address Marks and ID fields from the disk. When the current sector number (R) stored in the ID Register (IDR) matches the sector number read from the disk, the DDFDC transfers data from the disk Data field to the data bus.

After completion of the read operation from the current sector, the DDFDC increments the Sector Number (R) by one, and the data from the next sector is read and output to the data bus. This continuous read function is called a "Multi-Sector Read Operation." The Read Command terminates after reading the last data byte from sector R when R = EOT. ST0 bits 7 and 6 are set to 0 and 1, respectively, and ST1 bit 7 (EN) is set to a 1.

The Read Data command can also be terminated by a high Terminal Count (TC) signal. TC should be issued at the same time that the DACK for the last byte of data is sent. Upon receipt of TC, the DDFDC stops outputting data to the data bus, but continues to read data from the current sector, checks CRC (Cyclic Redundancy Count) bytes, and then at the end of that sector terminates the Read Data command and sets bits 7 and 6 in ST0

to 0. The amount of data which can be handled with a single command to the DDFDC depends upon MT (Multi-Track), MF (MFM/FM), and N (Number of Bytes/Sector) values. Table 3 shows the transfer capacity.

The multi-track function (MT) allows the DDFDC to read data from both sides of the disk. For a particular track, data is transferred starting at sector 1, side 0 and completed at sector L, side 1 (sector L = last sector on the side). This function pertains to only one track (the same track) on each side of the disk.

When N = 0 in command byte 6 (FM mode), the Data Length (DTL) in command byte 9 defines the data length that the DDFDC must treat as a sector. If DTL is smaller than the actual data length in a sector, the data beyond the DTL is not sent to the data bus. The DDFDC reads (internally) the complete sector, performs the CRC check, and depending upon the manner of command termination, may perform a multi-sector Read operation. When N is non-zero (MFM mode), DTL has no meaning and should be set to FF.

At the completion of the Read Data command, the head is not unloaded until the Head Unload Time (HUT) interval defined in the Specify command has elapsed. The head settling time may be avoided between subsequent reads if the processor issues another command before the head unloads. This time savings is considerable when disk contents are copied from one drive to another.

If the DDFDC detects the Index Hole twice in succession without finding the right sector (indicated in R), then the DDFDC sets the No Data (ND) flag in Status Register 1 (ST1) to a 1, sets Status Register 0 (ST0) bits 7 and 6 to 0 and 1, respectively, and terminates the Read Data command.

After reading the ID and Data fields in each sector, the DDFDC checks the CRC bytes. If a read error is detected (incorrect CRC in ID field), the DDFDC sets the Data Error (DE) flag in ST1 to a 1, sets the Data Error in Data Field (DD) flag in ST2 to a 1 if a CRC error occurs in the Data field, sets bits 7 and 6 in ST0 to 0 and 1, respectively, and terminates the command.

If the DDFDC reads a **Deleted Data Address Mark** from the disk, and the Skip Deleted Data Address Mark bit in the first command byte is not set (SK = 0), then the DDFDC reads all the data in the sector, sets the Control Mark (CM) flag in ST2 to a 1, and terminates the command. If SK = 1, the DDFDC skips the sector with the **Deleted Data Address Mark** and reads the next sector. The CRC bits in the deleted data field are not checked when SK = 1.

During disk data transfers from the DDFDC to the system, the DDFDC must be serviced by the system within 27 μ s in the FM mode, and within 13 μ s in the MFM mode, otherwise the DDFDC sets the Over Run (OR) flag in ST1 to a 1, sets bits 7 and 6 in ST0 to 0 and 1, respectively, and terminates the command.

If the processor terminates a read (or write) operation in the DDFDC, then the ID information in the result phase is dependent upon the state of the IDT bit in the first command byte and the End of Track (EOT) byte. Table 4 shows the values for Track Number (T), Head Number (H), Sector Number (R), and Number of Data Bytes/Sector (N), when the processor terminates the command.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	MT	MF	SK	0	0	1	1	0
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number (T)							
	4	Head Number (H)							
	5	Sector Number (R)							
	6	Number of Data Bytes per Sector (N)							
	7	End of Track (EOT)							
	8	Gap Length (GPL)							
	9	Data Length (DTL)							

Table 3. DDFDC Transfer Capacity

Multi-Track (MT)	MFM/FM (MF)	Bytes/Sector (N)	Maximum Transfer Capacity (Bytes/Sector) (Number of Sectors)	Final Sector Read from Disk
0	0	00	(128) (26) = 3,328	26 at Side 0
0	1	01	(256) (26) = 6,656	or 26 at Side 1
1	0	00	(128) (52) = 6,656	26 at Side 1
1	1	01	(256) (52) = 13,312	
0	0	01	(256) (15) = 3,840	15 at Side 0
0	1	02	(512) (15) = 7,680	or 15 at Side 1
1	0	01	(256) (30) = 7,680	15 at Side 1
1	1	02	(512) (30) = 15,360	
0	0	02	(512) (8) = 4,096	8 at Side 0
0	1	03	(1024) (8) = 8,192	or 8 at Side 1
1	0	02	(512) (16) = 8,192	8 at Side 1
1	1	03	(1024) (16) = 16,384	

Table 4. DDFDC Command Termination Values

Command Phase ID		Final Sector Transferred to/from Data Bus	Result Phase ID			
Multi-Track (MT)	Head Number (HD)		Track Number (T)	Head Number (H)	Sector Number (R)	No. of Data Bytes (N)
0	0	Less than EOT	NC	NC	R + 1	NC
	0	Equal to EOT	T + 1	NC	01	NC
	1	Less than EOT	NC	NC	R + 1	NC
	1	Equal to EOT	T + 1	NC	01	NC
1	0	Less than EOT	NC	NC	R + 1	NC
	0	Equal to EOT	NC	LSB	01	NC
	1	Less than EOT	NC	NC	R + 1	NC
	1	Equal to EOT	T + 1	LSB	01	NC

Notes:

1. NC (No Change): The same value as the one at the beginning of command execution.
2. LSB (Least Significant Bit): The least significant bit of H is complemented.

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector (N)

WRITE DATA

A command set of nine bytes places the DDFDC in the Write Data mode. After the Write Data command has been received the DDFDC loads the head (if it is unloaded), waits the specified Head Settling Time (defined in the Specify command), then begins reading ID fields from the disk. When the four bytes (T, H, R, N) loaded during the command match the four bytes of the ID field from the disk, the DDFDC transfers data from the data bus to the disk Data field.

After writing data into the current sector, the DDFDC increments the sector number (R) by one, and writes into the Data field in the next sector. The DDFDC continues this multi-sector write operation until the last byte is written to sector R when R = EOT. ST0 bits 7 and 6 are set to 0 and 1, respectively, and ST1 bit 7 (EN) is set to a 1.

The command can also be terminated by a high on Terminal Count (TC). If TC is sent to the DDFDC while writing into the current sector, then the remainder of the Data field is filled with 00 (zeros). In this case, ST0 bits 7 and 6 are set to 0 and the command is terminated.

The DDFDC reads the ID field of each sector and checks the CRC bytes. If the DDFDC detects a read error (incorrect CRC) in one

of the ID fields, it terminates the Write Data command, sets the DE flag in ST1 to a 1, and sets bits 7 and 6 in ST0 to 0 and 1, respectively.

The Write Data command operates in much the same manner as the Read Data command. Refer to the Read Data command for the handling of the following items:

- Transfer Capacity
- End of Track (EN) flag
- No Data (ND) flag
- Head Unload Time (HUT) interval
- ID information when the processor terminates command (see Table 4)
- Definition of Data Length (DTL) when N = 0 and when N ≠ 0

In the Write Data mode, data transfers from the data bus to the DDFDC must occur within 27 μs in the FM mode, and within 13 μs in the MFM mode. If the time interval between data transfers is longer than this, then the DDFDC terminates the Write Data command, sets the Over Run (OR) flag in ST1 to a 1, and sets bits 7 and 6 in ST0 to 0 and 1, respectively.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	MT	MF	0	0	0	1	0	1
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number (T)							
	4	Head Number (H)							
	5	Sector Number (R)							
	6	Number of Data Bytes per Sector (N)							
	7	End of Track (EOT)							
	8	Gap Length (GPL)							
	9	Data Length (DTL)							

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector (N)

WRITE DELETED DATA

The Write Deleted Data command is the same as the Write Data command except a Deleted Data Address Mark is written at the beginning of the Data field instead of the normal Data Address Mark.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	MT	MF	0	0	1	0	0	1
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number (T)							
	4	Head Number (H)							
	5	Sector Number (R)							
	6	Number of Data Bytes per Sector (N)							
	7	End of Track (EOT)							
	8	Gap Length (GPL)							
	9	Data Length (DTL)							

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector(N)

READ DELETED DATA

The Read Deleted Data command is the same as the Read Data command except that if SK = 0 when the DDFDC detects a **Data Address Mark** at the beginning of a Data field, it reads all the data in the sector and sets the CM flag in ST2 to a 1, and then terminates the command. If SK = 1, then the DDFDC skips the sector with the **Data Address Mark** and reads the next sector.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	MT	MF	SK	0	1	1	0	0
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number (T)							
	4	Head Number (H)							
	5	Sector Number (R)							
	6	Number of Data Bytes per Sector (N)							
	7	End of Track (EOT)							
	8	Gap Length (GPL)							
	9	Data Length (DTL)							

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector (N)

READ A TRACK

The Read a Track command is similar to the Read Data command except that this is a continuous read operation where all Data fields from each of the sectors on a track are read and transferred to the data bus. Immediately after encountering the Index Hole, the DDFDC starts reading the Data fields as continuous blocks of data. This command terminates when the number of sectors read is equal to EOT. Multi-track operations are not allowed with this command.

If the DDFDC finds an error in the ID or Data CRC check bytes, it continues to read data from the track. The DDFDC compares the ID information read from each sector with the value stored in the IDR, and sets the ND flag in ST1 to a 1 if there is no match.

If the DDFDC does not find an ID Address Mark on the disk after it encounters the Index Hole for the second time it terminates the command, sets the Missing Address Mark (MA) flag in ST1 to a 1, and sets bits 7 and 6 of ST0 to 0 and 1, respectively.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	0	MF	SK	0	0	0	1	0
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number (T)							
	4	Head Number (H)							
	5	Sector Number (R)							
	6	Number of Data Bytes per Sector (N)							
	7	End of Track (EOT)							
	8	Gap Length (GPL)							
	9	Data Length (DTL)							

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector (N)

READ ID

The two-byte Read ID command returns the present position of the read/write head. The DDFDC obtains the value from the first ID field it is able to read, sets bits 7 and 6 in ST0 to 0 and terminates the command.

If no proper ID Address Mark is found on the disk before the Index Hole is encountered for the second time then the Missing Address Mark (MA) flag in ST1 is set to a 1, and if no data is found then the ND flag in ST1 is also set to a 1. Bits 7 and 6 in ST0 are set to 0 and 1, respectively and the command is terminated.

During this command there is no data transfer between DDFDC and the data bus except during the result phase.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	0	MF	0	0	1	0	1	0
	2	X	X	X	X	X	HD	US1	US0

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector (N)

FORMAT A TRACK

The six-byte Format a Track command formats an entire track. After the Index Hole is detected, data is written on the disk: Gaps, Address Marks, ID fields and Data fields; all are recorded in either the double-density IBM System 34 format (MF = 1) or the single-density IBM 3740 format (MF = 0). The particular format written is also controlled by the values of Number of Bytes/Sector (N), Sectors/Track (ST), Gap Length (GPL) and Data Pattern (D) which are supplied by the processor during the command phase. The Data field is filled with the data pattern stored in D.

The ID field for each sector is supplied by the processor in response to four data requests per sector issued by the DDFDC. The type of data request depends upon the Non-DMA flag (ND) in the Specify command. In the DMA mode (ND = 0), the DDFDC asserts the DMA Request (DRQ) output four times per sector. In the Non-DMA mode (ND = 1), the DDFDC asserts Interrupt Request (INT) output four times per sector.

The processor must write one data byte in response to each request, sending (in the consecutive order) the Track Number (T), Head Number (H), Sector Number (R) and Number of Bytes/Sector (N). This allows the disk to be formatted with non-sequential sector numbers, if desired.

The processor must send new values for T, H, R, and N to the DDFDC for each sector on the track. For sequential formatting R is incremented by one after each sector is formatted, thus, R contains the total numbers of sectors formatted when it is read during the result phase. This incrementing and formatting continues for the whole track until the DDFDC, upon encountering the Index Hole for the second time, terminates the command and sets bits 7 and 6 in ST0 to 0.

If the Fault (FLT) signal is high from the FDD at the end of a write operation, the DDFDC sets the Equipment Check (EC) flag in ST0 to a 1, sets bits 7 and 6 of ST0 to 0 and 1, respectively, and terminates the command. Also, a low (RDY) signal at the beginning of a command execution phase causes bits 7 and 6 of ST0 to be set to 0 and 1, respectively.

Table 5 shows the relationship between N, ST, and GPL for various disk and sector sizes.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	0	MF	0	0	1	1	0	1
	2	X	X	X	X	X	HD	US1	US0
	3	Number of Bytes per Sector (N)							
	4	Sectors per Track (ST)							
	5	Gap Length (GPL)							
	6	Data Pattern (D)							

Table 5. Standard Floppy Disk Sector Size Relationship

Disk Size	Mode	Sector Size Bytes/Sector	No. of Data Bytes/Sector (N)	No. of Sectors/Track (ST)	Gap Length (GPL) ⁴		Remarks
					Read/Write Command ¹	Format Command ²	
8"	FM	128	00	1A	07	1B	
		256	01	0F	0E	2A	
		512	02	08	1B	3A	
		1024	03	04	47	8A	
		2048	04	02	C8	FF-	
		4096	05	01	C8	FF	
	MFM ³	256	01	1A	0E	36	
		512	02	0F	1B	54	
		1024	03	08	35	74	
		2048	04	04	99	FF	
		4096	05	02	C8	FF	
		8192	06	01	C8	FF	
5¼"	FM	128	00	12	07	09	
		128	00	10	10	19	
		256	01	08	18	30	
		512	02	04	46	87	
		1024	03	02	C8	FF	
		2048	04	01	C8	FF	
	MFM ³	256	01	12	0A	0C	
		256	01	10	20	32	
		512	02	08	2A	50	
		1024	03	04	80	F0	
		2048	04	02	C8	FF	
		4096	05	01	C8	FF	

Notes:

1. Suggested values of GPL in Read or Write commands to avoid overlapping between Data field and ID field of contiguous sections.
2. Suggested values of GPL in Format a Track command.
3. In MFM mode the DDFDC cannot perform a read/write/format operation with 128 bytes/sector (N = 00).
4. Values of ST and GPL are in hexadecimal.

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)*
	5	Head Number (H)*
	6	Sector Number (R)*
	7	Number of Data Bytes per Sector (N)*

* The ID information has no meaning in this command.

SCAN COMMANDS

The scan commands compare data read from the disk to data supplied from the data bus. The DDFDC compares the data, and looks for a sector of data which meets the conditions of $D_{FDD} = D_{BUS}$, $D_{FDD} \leq D_{BUS}$, or $D_{FDD} \geq D_{BUS}$ (D = the data pattern in hexadecimal). A magnitude comparison is performed (FF = largest number, 00 = smallest number). The hexadecimal byte of FF either from the bus or from FDD can be used as a mask byte because it always meets the condition of the compare. After a whole sector of data is compared, if the conditions are not met, the sector number is incremented ($R + STP \rightarrow R$), and the scan operation is continued. The scan operation continues until one of the following events occur: the conditions for scan are met (equal, low or equal, or high or equal), the last sector on the track is reached (EOT), or TC is received.

If conditions for scan are met, the DDFDC sets the Scan Hit (SH) flag in ST2 to a 1, and terminates the command. If the conditions for scan are not met between the starting sector (as specified by R) and the last sector on the track (EOT), then the DDFDC sets the Scan Not Satisfied (SN) flag in ST2 to a 1, and terminates the command. The receipt of TC from the processor or DMA controller during the scan operation will cause the DDFDC to complete the comparison of the particular byte which is in process, and then to terminate the command. Table 6 shows the status of bits SH and SN under various conditions of scan.

Table 6. Scan Status Codes

Command	Status Register 2		Comments
	Bit 2 = SN	Bit 3 = SH	
Scan Equal	0	1	$D_{FDD} = D_{BUS}$
	1	0	$D_{FDD} \neq D_{BUS}$
Scan Low or Equal	0	1	$D_{FDD} = D_{BUS}$
	0	0	$D_{FDD} < D_{BUS}$
	1	0	$D_{FDD} > D_{BUS}$
Scan High or Equal	0	1	$D_{FDD} = D_{BUS}$
	0	0	$D_{FDD} > D_{BUS}$
	1	0	$D_{FDD} < D_{BUS}$

If SK = 0 and the DDFDC encounters a Deleted Data Address Mark on one of the sectors, it regards that sector as the last sector of the track, sets the Control Mark (CM) bit in ST2 to a 1 and terminates the command. If SK = 1, the DDFDC skips the sector with the Deleted Data Address Mark, sets the CM flag to a 1 in order to show that a Deleted Sector has been encountered, and reads the next sector.

When either the STP sectors are read (contiguous sectors = 01, or alternate sectors = 02) or MT (Multi-Track) is set, **the last sector on the track must be read.** For example, if STP = 02, MT = 0, the sectors are numbered sequentially 1 through 26, and the scan command starts reading at sector 21. Sectors 21, 23, and 25 are read, then the next sector (26) is skipped and the Index Hole is encountered before the EOT value of 26 can be read. This results in an abnormal termination of the command. If the EOT had been set at 25 or the scanning started at sector 20, then the scan command would be completed in a normal manner.

During a scan command data is supplied from the data bus for comparison against the data read from the disk. In order to avoid having the Over Run (OR) flag set in ST1, data must be available from the data bus in less than 27 μ s (FM mode) or 13 μ s (MFM mode). If an OR occurs, the DDFDC terminates the command and sets bits 7 and 6 of ST0 to 0 and 1, respectively.

The following tables specify the command bytes and describe the result bytes for the three scan commands.

SCAN EQUAL

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	MT	MF	SK	1	0	0	0	1
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number (T)							
	4	Head Number (H)							
	5	Sector Number (R)							
	6	Number of Data Bytes per Sector (N)							
	7	End of Track (EOT)							
	8	Gap Length (GPL)							
	9	Sector Test Process (STP)							

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector (N)

SCAN LOW OR EQUAL

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	MT	MF	SK	1	1	0	0	1
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number (T)							
	4	Head Number (H)							
	5	Sector Number (R)							
	6	Number of Data Bytes per Sector (N)							
	7	End of Track (EOT)							
	8	Gap Length (GPL)							
	9	Sector Test Process (STP)							

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector (N)

SCAN HIGH OR EQUAL

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	MT	MF	SK	1	1	1	0	1
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number (T)							
	4	Head Number (H)							
	5	Sector Number (R)							
	6	Number of Data Bytes per Sector (N)							
	7	End of Track (EOT)							
	8	Gap Length (GPL)							
	9	Sector Test Process (STP)							

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector (N)

SEEK

The three-byte Seek command steps the FDD read/write head from track to track. The DDFDC has four independent Present Track Registers for each drive. They are cleared only by the Recalibrate command. The DDFDC compares the Present Track Number (PTN) which is the current head position with the New Track Number (NTN), and if there is a difference, performs the following operation:

If $PTN < NTN$: Sets the direction output (LCT/DIR) high and issues step pulses (FR/STP) to the FDD to cause the read/write head to step in.

If $PTN > NTN$: Sets the direction output (LCT/DIR) low and issues step pulses to the FDD to cause the read/write head to step out.

The rate at which step pulses are issued is controlled by the Step Rate Time (SRT) in the Specify command. After each step pulse is issued, NTN is compared against PTN. When $NTN = PTN$, then the Seek End (SE) flag in ST0 is set to a 1, bits 7 and 6 in ST0 are set to 0, and the command is terminated. At this point DDFDC asserts INT.

The FDD Busy flag (bit 0-3) in the Main Status Register (MSR) corresponding to the FDD performing the Seek operation is set to a 1.

After command termination, all FDD Busy bits set are cleared by the Sense Interrupt Status command.

During the command phase of the Seek operation the DDFDC sets the Controller Busy (CB) flag in the MSR to 1; but during the execution phase the CB flag is set to 0 to indicate DDFDC non-busy. While the DDFDC is in the non-busy state, another Seek command may be issued, and in this manner parallel seek operations may be performed on all drives at once.

No command other than Seek will be accepted while the DDFDC is sending step pulses to any FDD. If a different command type is attempted, the DDFDC will set bits 7 and 6 in ST0 to a 1 and 0, respectively, to indicate an invalid command.

If the FDD is in a not ready state at the beginning of the command execution phase or during the seek operation, then the DDFDC sets the Not Ready (NR) flag in ST0 to a 1, sets ST0 bits 7 and 6 to 0 and 1, respectively, and terminates the command.

If the time to write the three bytes of the Seek command exceeds $150\ \mu\text{s}$, the time between the first two step pulses may be shorter than the Step Rate Time (SRT) defined by the Specify command by as much as 1 ms.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	0	0	0	0	1	1	1	1
	2	X	X	X	X	X	0	US1	US0
	3	New Track Number (NTN)							

Result Phase: None.

RECALIBRATE

This two-byte command retracts the FDD read/write head to the Track 0 position. The DDFDC clears the contents of the PTN counters, and checks the status of the Track 0 signal from the FDD. As long as the Track 0 signal (TRK0) is low, the direction signal (LCT/DIR) output remains low and step pulses are issued on FR/STP. When TRK0 goes high the DDFDC sets the Seek End (SE) flag in ST0 to a 1 and terminates the command. If the TRK0 is still low after 256 step pulses have been issued, the DDFDC sets Seek End (SE) and Equipment Check (EC) flags in ST0 to 1s, sets bits 7 and 6 of ST0 to 0 and 1, respectively, and terminates the command.

The ability to do overlap Recalibrate commands to multiple FDDs and the loss of the RDY signal, as described in the Seek command, also applies to the Recalibrate command.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	0	0	0	0	0	1	1	1
	2	X	X	X	X	X	0	US1	US0

Result Phase: None.

SENSE INTERRUPT STATUS

Interrupt Request (INT) is asserted by the DDFDC when any of the following conditions occur:

1. Upon entering the result phase of:
 - a. Read Data command
 - b. Read a Track command
 - c. Read ID command
 - d. Read Deleted Data command
 - e. Write Data command
 - f. Format a Track command
 - g. Write Deleted Data command
 - h. Scan commands
2. Ready (RDY) line from the FDD changes state
3. Seek or Recalibrate command termination
4. During execution phase in the Non-DMA mode

INT caused by reasons 1 and 4 above occur during normal command operations and are easily discernible by the processor. During an execution phase in Non-DMA mode, bit 5 in the MSR is set to 1. Upon entering result phase this bit is set to 0. Reasons 1 and 4 do not require the Sense Interrupt Status command. The interrupt is cleared by reading or writing data to DDFDC. Interrupts caused by reasons 2 and 3 are identified with the aid of the Sense Interrupt Status command. This command resets INT and sets/resets bits 5, 6, and 7 of ST0 to identify the cause of the interrupt. Table 7 defines the seek and interrupt codes.

The Sense Interrupt Status command is used in conjunction with the Seek and Recalibrate commands which have no result phase. When the disk drive has reached the desired head position the DDFDC asserts interrupt output. The host CPU must then issue a Sense Interrupt Status command to determine the actual cause of the interrupt, which could be Seek End or a change in ready status from one of the drives (see example in Figure 4).

Issuing a Sense Interrupt Status command without an interrupt pending is treated as an invalid command.

Table 7. ST0 Seek and Interrupt Code Definition for Sense Interrupt Status

Status Register 0 (ST0) Bits			Cause
Interrupt Code (IC)	Seek End (SE)		
7	6	5	
1	1	0	RDY line changed state, either polarity
0	0	1	Normal termination of Seek or Recalibrate command
0	1	1	Abnormal termination of Seek or Recalibrate command

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	0	0	0	0	1	0	0	0

Result Phase:

R	1	Status Register 0 (ST0)
	2	Present Track Number (PTN)

SPECIFY

The three-byte Specify command sets the initial values for each of the three internal timers. The Head Unload Time (HUT) defines the time from the end of the execution phase of one of the read/write commands to the head unload state. This timer is programmable from 16 to 240 ms in increments of 16 ms (1 = 16 ms, 2 = 32 ms, . . . F = 240 ms).

The Step Rate Time (SRT) defines the time interval between adjacent step pulses. This timer is programmable from 1 to 16 ms in increments of 1 ms (F = 1 ms, E = 2 ms, D = 3 ms, . . . 0 = 16 ms.)

The Head Load Time (HLT) defines the time between the Head Load (HDL) signal going high and the start of the read/write operation. This timer is programmable from 2 to 254 ms in increments of 2 ms (01 = 2 ms, 02 = 4 ms, 03 = 6 ms, . . . 7F = 254 ms).

The time intervals are a direct function of the clock (CLK on pin 19). Times indicated above are for an 8 MHz clock. If the clock is reduced to 4 MHz (mini-floppy application) then all time intervals are increased by a factor of two.

The choice of DMA or Non-DMA operation is made by the Non-DMA mode (ND) bit. When this bit = 1 the Non-DMA mode is selected, and when ND = 0 the DMA mode is selected.

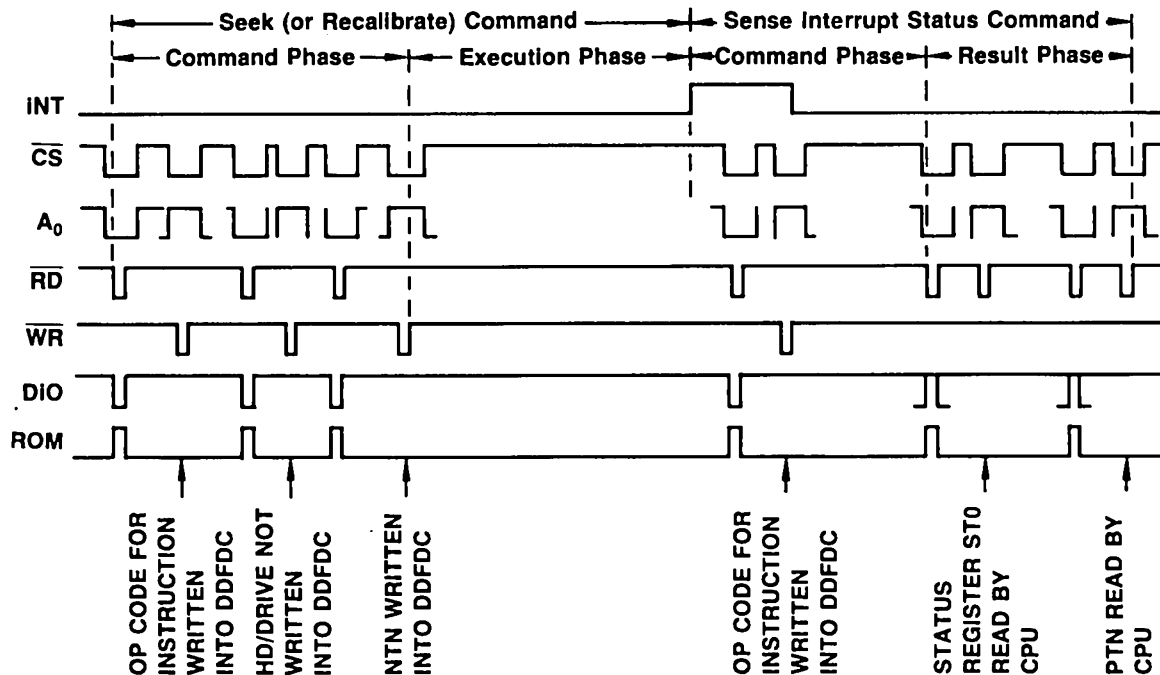
Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	0	0	0	0	0	0	1	1
	2	SRT				HUT			
	3	HLT							ND

SRT — Step Rate Time
 HUT — Head Unload Time
 HLT — Head Load Time
 ND — Non-DMA mode

Result Phase: None.

Figure 4. Sense Interrupt Status



SENSE DRIVE STATUS

This two-byte command obtains and reports the status of the FDDs. Status Register 3 (ST3) is returned in the result phase and contains the drive status.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	0	0	0	0	0	1	0	0
	2	X	X	X	X	X	HD	US1	US0

Result Phase:

R	1	Status Register 3 (ST3)
---	---	-------------------------

INVALID COMMAND

If an invalid command (i.e., a command not previously defined) is received by the DDFDC, then the DDFDC terminates the command after setting bits 7 and 6 of ST0 to 1 and 0, respectively. The DDFDC does not generate an interrupt during this condition. Bits 6 and 7 (DIO and RQM) in the MSR are both set to a 1 indicating to the processor that the DDFDC is in the result phase and that ST0 must be read. A hex 80 in ST0 indicates that an invalid command was received.

A Sense Interrupt Status command must be sent after a Seek or Recalibrate interrupt, otherwise the DDFDC considers the next command to be an invalid command.

In some applications the user may wish to use this command as a No-Op command, to place the DDFDC in a standby or no operation state.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	Invalid Codes							

Result Phase:

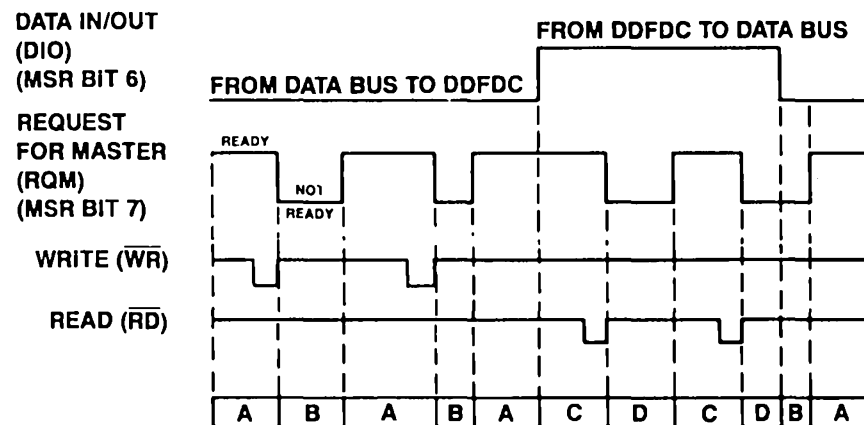
R	1	Status Register 0 (ST0) = 80
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PROCESSOR INTERFACE

During the command or result phases, the Main Status Register (MSR) must be read by the processor before each byte of information is transferred to, or from, the DDFDC Data Register. After each byte of data is written to, or read from, the Data Register, the processor should wait 12 μ s before reading the MSR. Bits 6 and 7 in the MSR must be a 0 and 1, respectively, before each command byte can be written to the DDFDC. During the result phase, bits 6 and 7 of the MSR must both be 1s prior to reading each byte from the Data Register onto the data bus. Note that this status reading of bits 6 and 7 of the MSR before each byte transfer to and from the DDFDC is required in only the command and result phases and not during the execution phase.

During the result phase all bytes shown in the result phase must be read by the processor. The Read Data command, for example, has seven bytes of data in the result phase. All seven bytes must be read to successfully complete the Read Data command. The DDFDC will not accept a new command until all seven bytes have been read. Other commands may require fewer bytes to be read during the result phase.

Figure 5. DDFDC and System Data Transfer Timing



NOTES

- | | |
|---|--|
| A DATA REGISTER READY TO BE WRITTEN INTO | C DATA REGISTER READY FOR NEXT DATA BYTE TO BE READ |
| B DATA REGISTER NOT READY TO BE WRITTEN INTO | D DATA REGISTER NOT READY FOR NEXT DATA BYTE TO BE READ |

INTERRUPT REQUEST MODE

During the execution phase, the MSR need not be read. The receipt of each data byte from the FDD is indicated by INT high on pin 18. When the DDFDC is in Non-DMA mode, INT is asserted during the execution phase. When the DDFDC is in the DMA mode, INT is asserted at the result phase. The INT signal is reset by a read (\overline{RD} low) or write (\overline{WR} low) of data to the DDFDC. A further explanation of the INT signal is described in the Sense Interrupt Status command on page 16. If the system cannot handle interrupts fast enough (within 13 μ s for MFM mode or 27 μ s for FM mode), it should poll bit 7 (RQM) in the MSR. In this case, RQM in the MSR functions as an Interrupt Request (INT). If the RQM bit is not set, the Over Run (OR) flag in ST1 will be set to a 1 and bits 7 and 6 of ST0 will be set to a 0 and 1, respectively.

the EOT sector is read), INT is asserted to indicate the beginning of the result phase. When the first byte of data is read during the result phase, INT is reset low.

During a write command, the DDFDC asserts DRQ as each byte of data is required. The DMA controller responds to this request with \overline{DACK} (DMA Acknowledge) and \overline{WR} low (write). When \overline{DACK} goes low the DMA Request is reset (DRQ low). After the execution phase has been completed (TC high or the EOT sector is written), INT is asserted. This signals the beginning of the result phase. When the first byte of data is read during the result phase, the INT is reset low.

DMA MODE

When the DDFDC is in the DMA mode ($ND = 0$ in the third command byte of the Specify command), DRQ (DMA Request) is asserted during the execution phase (rather than INT) to request the transfer of a data byte between the data bus and the DDFDC.

During a read command, the DDFDC asserts DRQ as each byte of data is available to be read. The DMA controller responds to this request with \overline{DACK} low (DMA Acknowledge) and \overline{RD} low (read). When \overline{DACK} goes low the DMA Request is reset (DRQ low). After the execution phase has been completed (TC high or

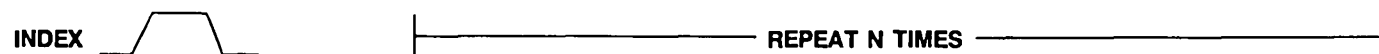
FDD POLLING

After the Specify command has been received by the DDFDC, the Unit Select lines (US0 and US1) begin the polling mode. Between commands (and between step pulses in the Seek Command) the DDFDC polls all the FDD's looking for a change in the RDY line from any of the drives. If the RDY line changes state (usually due to the door opening or closing) then the DDFDC asserts INT. When Status Register 0 (ST0) is read (after Sense Interrupt Status command is issued), Not Ready ($NR = 1$) will be indicated. The polling of the RDY line by the DDFDC occurs continuously between commands, thus notifying the processor which drives are on- or off-line. Each drive is polled every 1.024 ms except during read/write commands.

Figure 6. DDFDC Formats

FM MODE

FIELD	GAP 4a	SYNC	IAM	GAP 1	SYNC	IDAM	CYL	HD	SEC	NO	CRC	GAP 2	SYNC	DATA AM	DATA		GAP 3	GAP 4b
NO. OF BYTES	40 x	6 x		26 x	6 x							11 x	6 x		①	CRC	①	
DATA	FF	00	FC	FF	00	FE						FF	00	FB OR F8				



MFM MODE

GAP 4a	SYNC	IAM		GAP 1	SYNC	IDAM		CYL	HD	SEC	NO	CRC	GAP 2	SYNC	DATA AM		DATA		GAP 3	GAP 4b
80 x	12 x	3 x		50 x	12 x	3 x							22x	12 x	3 x	FB	①	CRC	①	
4E	00	C2	FC	4E	00	A1	FE						4E	00	A1	F8				

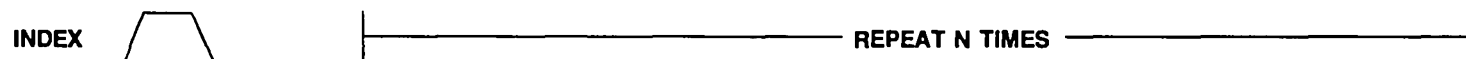


Figure 7. DDFDC Formats

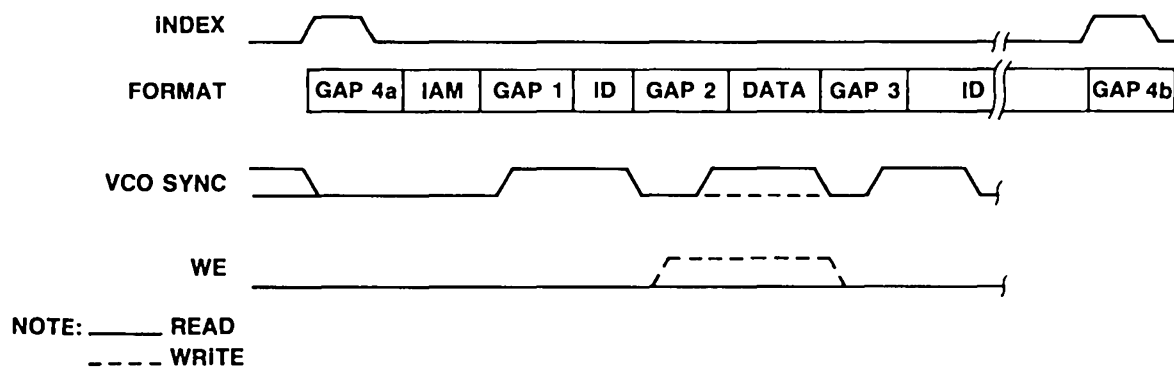


Figure 8. VL6765 DDFDC Interface to Z80

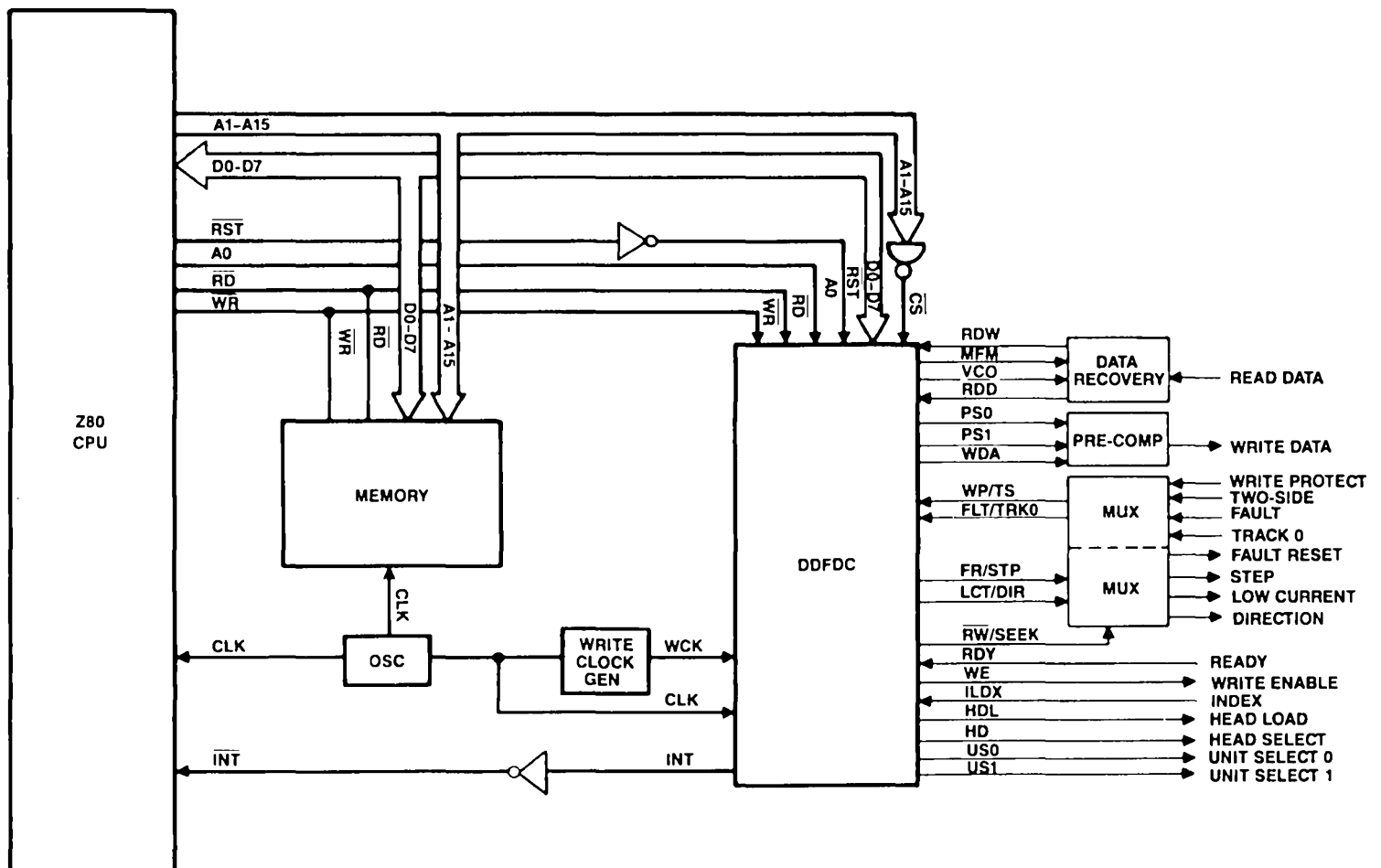


Figure 9. Clock Timing

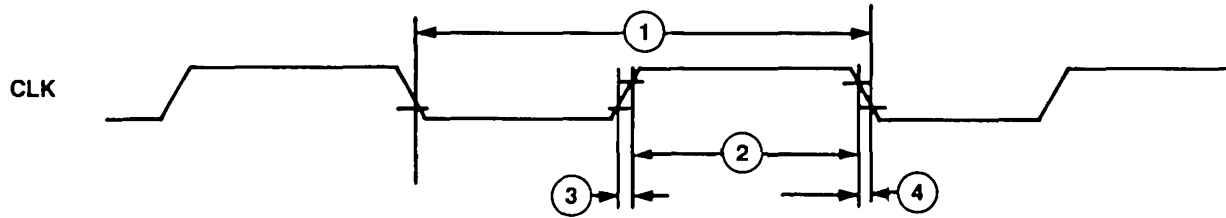


Figure 10. Read Cycle Timing

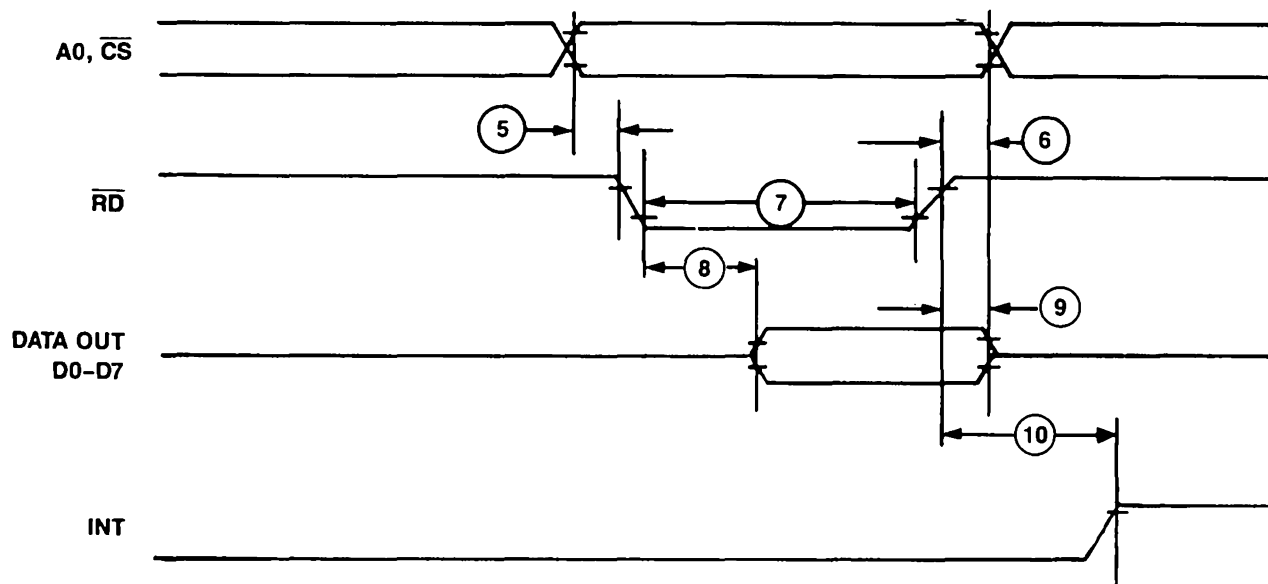


Figure 11. Write Cycle Timing

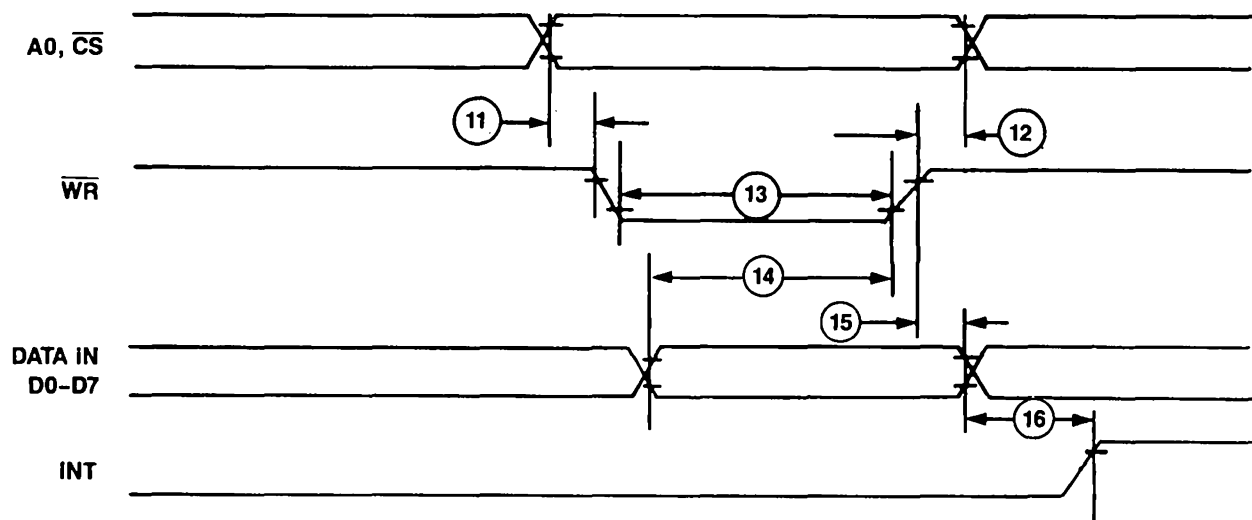


Figure 12. DMA Operation Timing

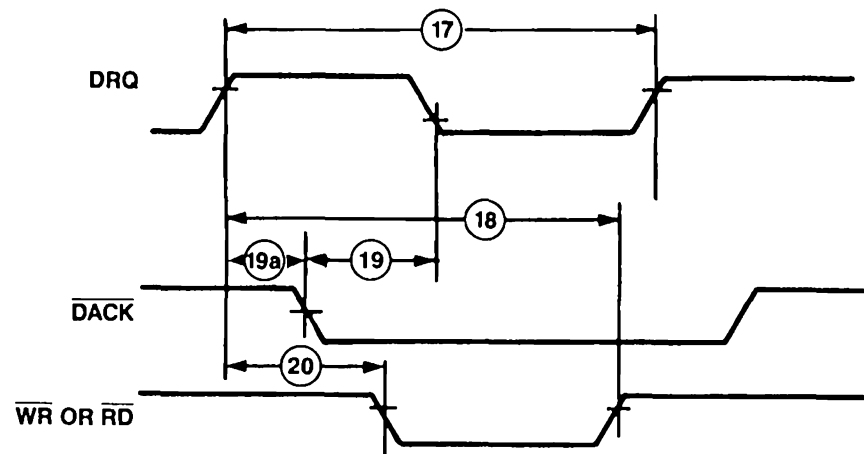


Figure 13. FDD Write Operation Timing

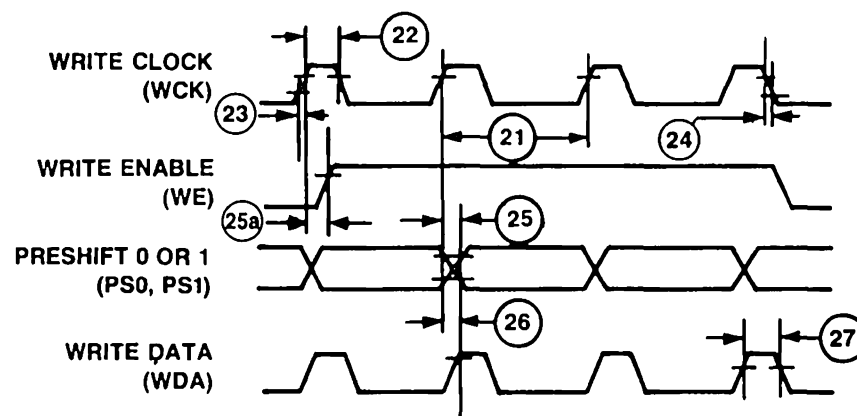
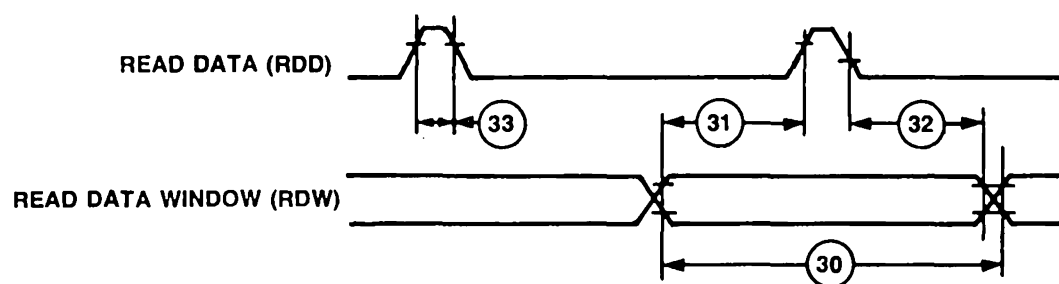


Figure 14. FDD Read Operation Timing



NOTE:
EITHER POLARITY DATA WINDOW IS VALID

Figure 15. Seek Operation Timing

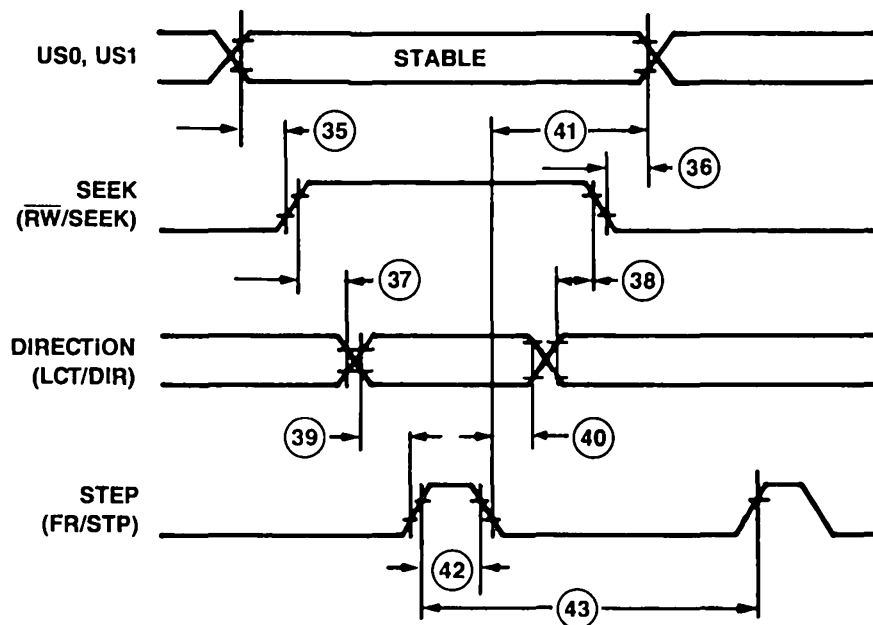


Figure 16. Fault Reset Timing

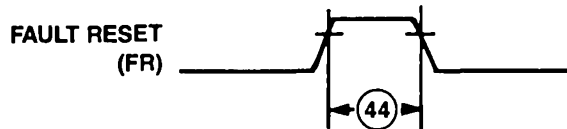


Figure 17. Index Timing

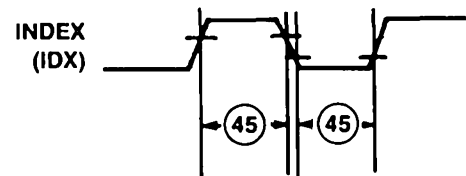


Figure 18.. Terminal Count Timing

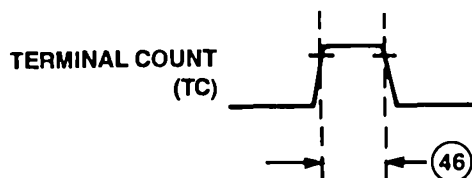


Figure 19. Reset Timing

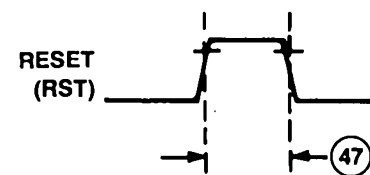
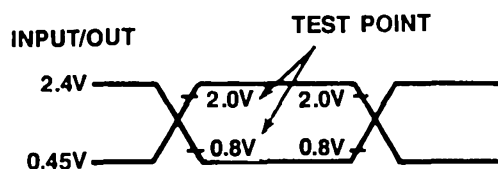
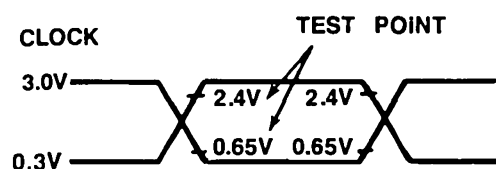


Figure 20. AC Timing Measurement Conditions



INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" AND 0.45 V FOR A LOGIC "0." TIMING MEASUREMENTS ARE MADE AT 2.0V FOR A LOGIC "1" AND 0.8V FOR A LOGIC "0."



CLOCKS ARE DRIVEN AT 3.0V FOR A LOGIC "1" AND 0.3V FOR A LOGIC "0." TIMING MEASUREMENTS ARE MADE AT 2.4V FOR A LOGIC "1" AND 0.65V FOR A LOGIC "0."

AC CHARACTERISTICS
 $(V_{CC} = 5.0 \text{ Vdc} \pm 5\%, V_{SS} = 0 \text{ Vdc}, T_A = 0^\circ\text{C to } 70^\circ\text{C})$

Ref. Fig.	No.	Characteristic	Symbol	Alt. Sym.	Min.	Typ.	Max.	Unit	Test Conditions
8	1	Clock Period	t_{CY}	ϕ_{CY}	120	125	500	ns	CLK = 8 MHz
					—	250	—	ns	CLK = 4 MHz
	2	Clock High	t_{CA}	ϕ_O	40	—	—	ns	CLK = 8 MHz
	3	Clock Rise Time	t_{CLCH}	ϕ_r	—	—	20	ns	
9	4	Clock Fall Time	t_{CHCL}	ϕ_f	—	—	20	ns	
	5	A0, \overline{CS} , \overline{DACK} Valid to \overline{RD} Low (Setup)	t_{SLRL}	t_{AR}	0	—	—	ns	
	6	\overline{RD} High to A0, \overline{CS} , \overline{DACK} Invalid (Hold)	t_{RHSH}	t_{RA}	0	—	—	ns	
	7	\overline{RD} Low Width	t_{RLRH}	t_{RR}	250	—	—	ns	
10	8	\overline{RD} Low to Data Valid (Access)	t_{RLDV}	t_{RD}	—	—	200	ns	$C_L = 100 \text{ pF}$
	9	\overline{RD} High to Output High Z	t_{RHDZ}	t_{DF}	20	—	100	ns	
	10	\overline{RD} High to INT High	t_{RHHH}	t_{RI}	—	—	500	ns	CLK = 8 MHz
	11	A0, \overline{CS} , \overline{DACK} Valid to \overline{WR} Low (Setup)	t_{SLWL}	t_{AW}	0	—	—	ns	
11	12	\overline{WR} High to A0, \overline{CS} , \overline{DACK} Invalid (Hold)	t_{WHSW}	t_{WA}	0	—	—	ns	
	13	\overline{WR} Low Width	t_{WLWH}	t_{WW}	250	—	—	ns	
	14	Data Valid to \overline{WR} High (Setup)	t_{DVWH}	t_{DW}	150	—	—	ns	
	15	\overline{WR} High to Data Invalid (Hold)	t_{WHDH}	t_{WD}	5	—	—	ns	
11	16	\overline{WR} High to INT High	t_{WHHH}	t_{WI}	—	—	500	ns	
	17	DRQ Cycle Time	t_{OCY}	t_{MCY}	13	—	—	μs	CLK = 8 MHz
	18	DRQ High to \overline{RD} , \overline{WR} High (Response)	t_{OHXH}	t_{MRW}	—	—	12	μs	
	19	\overline{DACK} Low to DRQ Low (Delay)	t_{ALQL}	t_{AM}	—	—	200	ns	
11	19a	DRQ High to \overline{DACK} Low (Delay)	t_{OHAL}	t_{MA}	200	—	—	ns	$t_{CY} = 125 \text{ ns}$
	20	DRQ High to \overline{RD} Low (Delay)	t_{OHRH}	t_{MR}	800	—	—	ns	CLK = 8 MHz
12	21	WCK Cycle Time	t_{KCY}	t_{CY}	—	2	—	μs	MFM = 0
					—	1	—	μs	MFM = 1
	22	WCK High Width	t_{KHKL}	t_0	—	4	—	μs	MFM = 0
					—	2	—	μs	MFM = 1
12	23	WCK High Width	t_{KHKL}	t_0	80	250	350	ns	
	24	WCK Rise Time	t_{KLKH}	t_r	—	—	20	ns	
	25	WCK Fall Time	t_{KHKL}	t_f	—	—	20	ns	
	26	WCK High to PS0, PS1 Valid (Delay)	t_{KHPV}	t_{CP}	20	—	100	ns	
13	27	WCK High to WE High (Delay)	t_{DHEN}	t_{CWE}	20	—	100	ns	
	28	WCK High to WDA High	t_{PVDH}	t_{CD}	20	—	100	ns	
	29	WDA High Width	t_{DHDH}	t_{WDD}	$t_{KHKL} - 50$	—	—	ns	
	30	RDW Cycle Time	t_{WCY}	t_{WCY}	—	2	—	μs	MFM = 0
13	31	RDW Valid to RDD High (Setup)	t_{WVRH}	t_{WRD}	—	1	—	μs	MFM = 1
					—	4	—	μs	MFM = 0
	32	RDD Low to RDW Invalid (Hold)	t_{RLWH}	t_{RDW}	—	2	—	μs	MFM = 1
					—	—	—	μs	MFM = 0
14	33	RDD High Width	t_{RHRL}	t_{RDD}	40	—	—	ns	
	35	US0, US1 Valid to SEEK High (Setup)	t_{UVSH}	t_{US}	12	—	—	μs	
	36	SEEK Low to US0, US1 Invalid (Hold)	t_{SLUI}	t_{SU}	15	—	—	μs	
	37	SEEK High to DIR Valid (Setup)	t_{SHDV}	t_{SD}	7	—	—	μs	
14	38	DIR Invalid to SEEK Low (Hold)	t_{DXSL}	t_{DS}	30	—	—	μs	CLK = 8 MHz
	39	DIR Valid to STP High (Setup)	t_{DVTH}	t_{DST}	1	—	—	μs	
	40	STP Low to DIR Invalid (Hold)	t_{TLDX}	t_{STD}	24	—	—	μs	
	41	STP Low to US0, US1 Invalid (Hold)	t_{TLUX}	t_{STU}	5	—	—	μs	
15	42	STP High Width	t_{HTHL}	t_{STP}	6	7	8	μs	
	43	STP Cycle Time	t_{TCY}	t_{SC}	33 ³	—	note 1	μs	
	44	FR High Width	t_{FHFL}	t_{FR}	8	—	10	μs	
	45	IDX High Width	t_{IHIL}	t_{IDX}	10	—	—	t_{CY}	
16	46	TC High Width	t_{HTHL}	t_{TC}	1	—	—	t_{CY}	
17	47	RST High Width	t_{RHRL}	t_{RST}	14	—	—	t_{CY}	

1. $t_{SC} = 33 \mu\text{s}$ min. is for different drive units. In the case of the same unit, t_{SC} can range from 1 ms to 16 ms with 8 MHz clock period, and 2 ms to 32 ms with 4 MHz clock, under software control.

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	V
Input Voltage	V_{IN}	-0.3 to +7.0	V
Output Voltage	V_{OUT}	-0.3 to +7.0	V
Operating Temperature Range	T_A	0 to +70	C°
Storage Temperature Range	T_{STG}	-55 to +150	C°

***NOTE:** Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	Range
V_{CC} Power Supply	5.0V \pm 5%
Operating Temperature	0°C to 70°C

DC CHARACTERISTICS

($V_{CC} = 5.0$ Vdc \pm 5%, $V_{SS} = 0$ Vdc, $T_A = 0^\circ\text{C}$ to 70°C , unless otherwise noted)

Parameter	Symbol	Min	Max	Unit	Test Conditions
Input Low Voltage Logic CLK and WCK	V_{IL}	-0.5 -0.5	0.8 0.65	V	
Input High Voltage Logic CLK and WCK	V_{IH}	2.0 2.4	$V_{CC} + 0.5$ $V_{CC} + 0.5$	V	
Output Low Voltage	V_{OL}		0.45	V	$V_{CC} = 4.75\text{V}$, $I_{OL} = 2.0$ mA
Output High Voltage	V_{OH}	2.4	V_{CC}	V	$V_{CC} = 4.75\text{V}$, $I_{OH} = -200$ μA
V_{CC} Supply Current	I_{CC}		150	mA	$V_{CC} = 4.75\text{V}$
Input Load Current All Inputs	I_{IL}		10 -10	μA μA	$V_{IN} = V_{CC}$ $V_{IN} = 0\text{V}$
High Level Output Leakage Current	I_{LOH}		10	μA	$V_{CC} = 0\text{V}$ to 5.25V , $V_{SS} = 0\text{V}$ $V_{OUT} = V_{CC}$
Low Level Output Leakage Current	I_{LOL}		-10	μA	$V_{CC} = 0\text{V}$ to 5.25V , $V_{SS} = 0\text{V}$ $V_{OUT} = +0.45\text{V}$
Internal Power Dissipation	P_{INT}	—	1.0	W	$T_A = 25^\circ\text{C}$

CAPACITANCE

($T_A = 25^\circ\text{C}$; $f_c = 1$ MHz; $V_{CC} = 0\text{V}$)

Parameter	Symbol	Max Limit	Unit
Clock Input	$C_{IN(\emptyset)}$	20	pF
Input	C_{IN}	10	pF
Output	C_{OUT}	20	pF

Note: All pins except pin under test tied to ground.

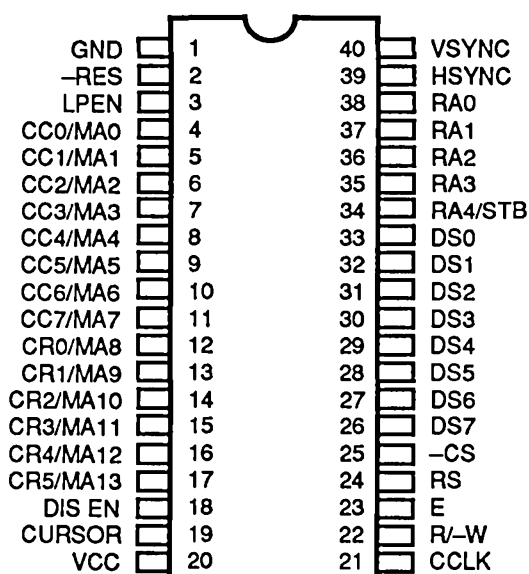
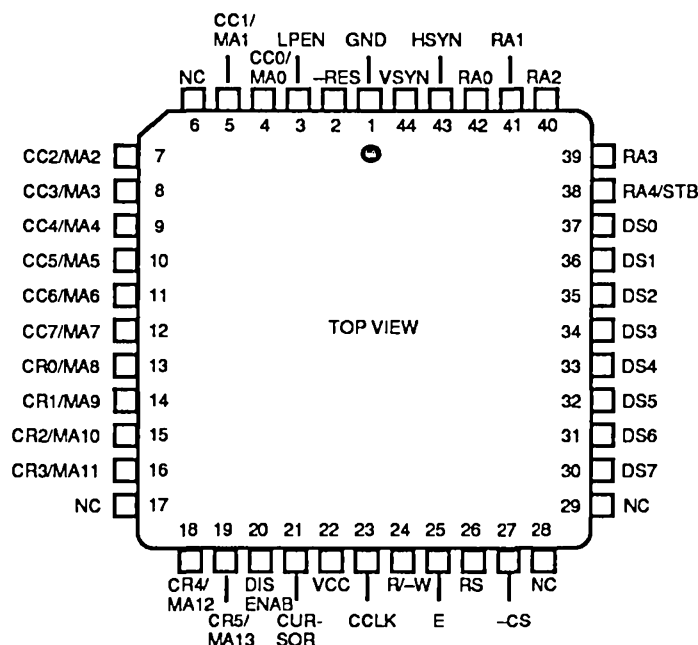
CRT CONTROLLER FAMILY
FEATURES

- CMOS technology
 - Rev R compatible with MC6845R1, MC6845 and MC146845
 - Rev S compatible with HD6845S
- Internal refresh address generation
- Light pen interface
- Character clocks up to 8 MHz
- Bus clocks up to 3 MHz
- Single 5 V power supply

DESCRIPTION

The VL68C45X is a family of CRT controllers that are widely used in both bit-mapped and character-mapped applications for both terminals and personal computers. VL68C45 family allows designs to consume less power through the use of CMOS technology.

In addition to compatibility with both the Motorola and Hitachi families, the VL68C45R also contains enhancements found in the MC6845R1. These enhancements allow for higher resolution displays without extra external hardware.

PIN DIAGRAMS
VL68C45R/S-PC,CC

VL68C45R/S-QC

ORDER INFORMATION

Part Number	Clock Frequency		Package
	Bus	Character	
VL68C45R-23 VL68C45S-23	2 MHz	3 MHz	To specify package type, add the appropriate suffix to the part number: PC = Plastic DIP CC = Ceramic DIP QC = Plastic Leaded Chip Carrier (PLCC)
VL68C45R-35 VL68C45S-35	3 MHz	5 MHz	
VL68C45R-36 VL68C45S-36		6 MHz	
VL68C45R-38 VL68C45S-38		8 MHz	

Note: Operating temperature range is 0°C to +70°C.

SIGNAL DESCRIPTIONS

Signal Name	Pin Number (DIP)	Signal Description
E	23	Enable - Input that is used as a data strobe; does not have to be a free-running clock. This capability allows the VL68C45 to interface with other non-6800/6500-type microprocessors.
R/-W	22	Read/-Write - Input that, when high, allows the processor to read the data supplied by the VL68C45; when this signal is low, the processor writes into the VL68C45.
-CS	25	-Chip Select - Input that, when high, deselects VL68C45; when this signal is low, the VL68C45 is selected. This signal is typically connected to the system address bus either directly or through an address decoder.
RS	24	Register Select - Input that, when low, selects the Address Register of the VL68C45 for a write operation. When this signal is high, an internal register of the VL68C45 specified by the contents of the address register is selected.
D0 - D7	26 - 33	Data Bus - Eight bidirectional data lines that are used for transferring data between the microprocessor and the VL68C45. These lines are normally high-impedance, except during read and write cycles when the chip is selected.
CC0/MA0 - CC5/MA13	4 - 17	Video Memory Address - Active-high output signals that are used to address the video display memory in binary addressing mode. These memory addresses are generated in a binary sequential fashion. In row/column addressing mode, MA0-MA7 function as column addresses, and MA8-MA13 function as row addresses.
RA0 - RA4/STB	34 - 38	Raster Address - Active-high output signals that are used as address lines to the external character generator ROM. In the transparent addressing mode, RA4 functions as an active-high output strobe.
HSYNC	39	Horizontal Sync - Active-high TTL-compatible output signal that is used to determine the horizontal position of the displayed text. VSYNC may be used to drive a CRT monitor directly or may be used for composite video generation. VSYNC position is fully programmable.
VSYNC	40	Vertical Sync - Active-high, TTL-compatible output signal that is used to determine the vertical position of the displayed text. VSYNC may be used to drive a CRT monitor directly or may be used for composite video generation. VSYNC position is fully programmable.
DISPLAY	18	Display Enable - TTL-compatible output that, when high, indicates that the VL68C45 is generating active display information. The number of horizontal displayed characters and the number of vertical displayed rows are both fully programmable and together are used to generate the Display Enable signal.
CURSOR	19	Cursor - TTL-compatible output that when high, indicates a valid cursor address to the external video processing logic.
LPSTB	3	Light Pen Strobe - high impedance, edge-sensitive input signal that latches the current refresh address into the light pen register. Latching occurs on the low-to-high transition edge.
CCLK	21	Character Clock - Input signals derived from the external dot clock, that is used as the time base for all internal count and control functions.
-RES	2	-Reset - Input signal that when low, resets all internal counters. All scan and video outputs are low and all control registers are unaffected. RES can be used to synchronize display frame timing with the line frequency.
VCC	20	Power Supply Voltage is 5 V.
GND	1	Ground - Supply and signal ground

FUNCTIONAL DESCRIPTION

The VL68C45 CRT Controller (CRTC) consists of programmable horizontal and vertical timing generators, programmable linear address registers, programmable cursor logic, a light pen capture register and control circuitry for interface to a processor bus.

All CRTC timing is derived from the character clock (CCLK), which is usually the output of an external dot rate counter. Coincidence circuits internal to the chip continuously compare counter contents to the programmed register file (R0-R17) for generation of Horizontal Sync, Vertical Sync, Display Enable, Cursor and other signals required to interface to a CRT display.

The linear address generator is also driven by the CCLK and locates the positions of characters of memory. The CRTC addresses the memory in the binary sequential fashion. Using the start address register, hardware scrolling through the 16k character memory is possible. The linear address generator continues to increment during the blanking period, so memory refresh can be performed during the blanking periods. The linear address generator repeats the same sequence of addresses for each scan line of a character row. Although the linear address generator continues to increment during the horizontal and blanking periods, the

correct address for the first displayed character or row is always maintained.

The Cursor logic determines the cursor location, size and blink rate on the screen.

The Light Pen Strobe latches the current contents of the address counter into the light pen register on low-to-high transition.

INTERLACE MODE SELECTION

In the normal sync mode (non-interlace), only one field is available, as shown in Figure 1a. Each scan line is refreshed at the VSYNC frequency (50 or 60 Hz).

Two interlace modes are available as shown in Figure 1b and Figure 1c. The frame time is divided between even and odd alternating fields. The horizontal and vertical timing relationship (VSYNC delayed by one-half scan line time) results in the displacement of scan lines in the odd field with respect to the even field.

In the interlace sync mode, the same information is painted in both fields, as shown in Figure 1b. This is a useful mode for filling in a character to enhance readability.

In the interlace sync and video mode, as shown in Figure 1c, alternating lines of the character are displayed in the even field and the odd field. This

effectively doubles the given band width of the CRT monitor.

Care must be taken when using either interlace mode to avoid an apparent flicker effect. This flicker effect is due to the doubling of the refresh time for all scan lines since each field is displayed alternately and may be minimized with proper monitor design i.e., longer persistence phosphors.

VL68C45R REGISTER FILE DESCRIPTIONS

The 19 registers of the CRTC may be accessed through the data bus. Only two memory locations are required, as one location is used as a pointer to address one of the remaining 18 registers. These 18 registers control horizontal timing, vertical timing, interlace operation and row address operation. They also define the cursor, cursor address, start address and light pen register. The register addresses and sizes are shown in Table 1.

ADDRESS REGISTER (AR)

The Address Register is a 5-bit write-only register used as an "indirect" or "pointer" register. It contains the address of one of the other 18 registers. When both RS and $\overline{\text{CS}}$ are low, the Address Register is selected. When $\overline{\text{CS}}$ is low and RS is high, the register pointed to by the address register is selected.

FIGURE 1a.
NORMAL SYNC

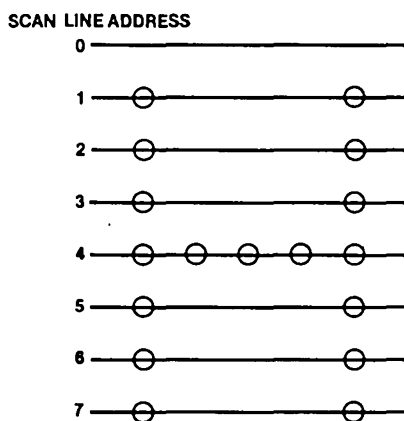


FIGURE 1b.
INTERLACE SYNC

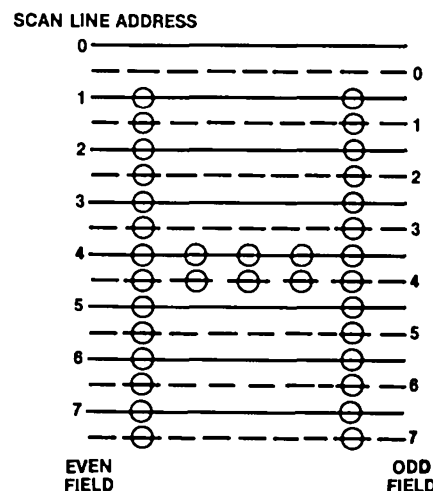
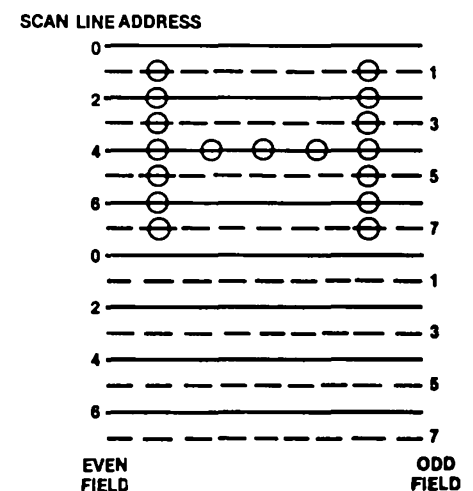


FIGURE 1c.
INTERLACE SYNC AND VIDEO



VL68C45R REGISTER FILE
DESCRIPTIONS (Cont.)
HORIZONTAL TOTAL REGISTER (R0)

This 8-bit write-only register determines the horizontal sync (HSYNC) frequency by defining the HSYNC period in character times. It is the total of the displayed characters plus the non-displayed character times (retrace) minus one.

HORIZONTAL DISPLAYED REGISTER (R1)

This 8-bit write-only register determines the number of displayed characters per line. Any 8-bit number may be programmed as long as the contents of R0 are greater than the contents of R1.

HORIZONTAL SYNC POSITION REGISTER (R2)

This 8-bit write-only register controls the HSYNC position, which defines the horizontal sync delay (front porch) and the horizontal scan delay (back porch).

When the programmed value of this register is increased, the display on the CRT screen is shifted to the left. When the programmed value is decreased, the display is shifted to the right. Any 8-bit number may be programmed as long as the sum of the contents of R2 and R3 is less than the contents of R0. The contents of R2 must be greater than R1.

SYNC WIDTH REGISTER (R3)

This 8-bit write-only register determines the width of the HSYNC pulse. The vertical sync pulse width is fixed at 16 scan-line times. HSYNC pulse width may be programmed from 1 to 15 character clock periods, thus allowing compatibility with the HSYNC pulse width specifications of many different monitors. If zero is written into this register, no horizontal sync is provided.

HORIZONTAL TIMING SUMMARY

The difference between R0 and R1 is the horizontal blanking interval. This

interval in the horizontal scan period allows the beam to return (retract) to the left side of the screen. The retrace time is determined by the monitor horizontal scan components. Retrace time is less than the horizontal blanking interval.

A good rule of thumb is to make the horizontal blanking about 20% of the total horizontal scanning period for a CRT. In inexpensive TV receivers the beam over-scans the display screen so that aging of parts does not result in underscanning. Because of this, the retrace time should be about one-third the horizontal scanning period. The horizontal sync delay is typically programmed with a 1:2:2 ratio.

VERTICAL TOTAL REGISTER (R4) AND VERTICAL TOTAL ADJUST REGISTER (R5)

The vertical sync (VSYNC) frequency is determined by both R4 and R5. The calculated number of character row

TABLE 1. VL68C45R INTERNAL REGISTER ASSIGNMENTS

CS	RS	Address Register					Register #	Register File	Program Unit	Read	Write	Number of Bits								
		4	3	2	1	0						7	6	5	4	3	2	1	0	
1	X	X	X	X	X	X	X	—	—	—	—									
0	0	X	X	X	X	X	AR	Address Register	—	No	Yes									
0	1	0	0	0	0	0	RO	Horizontal Total	Char.	No	Yes									
0	1	0	0	0	0	1	R1	Horizontal Displayed	Char.	No	Yes									
0	1	0	0	0	1	0	R2	H. Sync Position	Char.	No	Yes									
0	1	0	0	0	1	1	R3	Sync Width	—	No	Yes					H	H	H	H	
0	1	0	0	1	0	0	R4	Vertical Total	Char. Row	No	Yes									
0	1	0	0	1	0	1	R5	V. Total Adjust	Scan Line	No	Yes									
0	1	0	0	1	1	0	R6	Vertical Displayed	Char. Row	No	Yes									
0	1	0	0	1	1	1	R7	V. Sync Position	Char. Row	No	Yes									
0	1	0	0	0	1	1	R3	Sync Width	—	No	Yes								I	I
0	1	0	1	0	0	1	R9	Max Scan Line Address	Scan Line	No	Yes									
0	1	0	1	0	1	0	R10	Cursor Start	Scan Line	No	Yes	B		P			(Note 2)			
0	1	0	1	0	1	1	R11	Cursor End	Scan Line	No	Yes									
0	1	0	1	1	0	0	R12	Start Address (H)	—	No	Yes	0	0							
0	1	0	1	1	0	1	R13	Start Address (L)	—	No	Yes									
0	1	0	1	1	1	0	R14	Cursor (H)	—	Yes	Yes	0	0							
0	1	0	1	1	1	1	R15	Cursor (L)	—	Yes	Yes									
0	1	1	0	0	0	0	R16	Light Pen (H)	—	Yes	No	0	0							
0	1	1	0	0	0	1	R17	Light Pen (L)	—	Yes	No									

Notes:

1. The interlace bits are described in Table 2.
2. Bit 5 of the cursor start raster register is used for blink period, control, and bit 6 is used to select blink or no-blink.
3. Registers R4, R6 and R7 in the VL68C45R are eight bits wide, instead of seven, for compatibility with the Motorola 6845R1.

VL68C45R REGISTER FILE DESCRIPTIONS (Cont.)

times is usually an integer plus a fraction to get exactly a 50 Hz or 60 Hz vertical refresh rate. The integer number of character row times minus one is programmed into the 7-bit write-only vertical total register (R4). The fraction of character line times is programmed into the 5-bit write-only vertical total adjust register (R5) as the number of scan lines required.

VERTICAL DISPLAYED REGISTER (R6)

This 7-bit write-only register specifies the number of character rows displayed on the CRT screen, and is programmed in character row times. Any number smaller than contents R4 may be programmed into R6.

VERTICAL SYNC POSITION REGISTER (R7)

This 7-bit write-only register controls the position of vertical sync with respect to the reference. It is programmed in character row times. When programmed value of this register is increased, the display position of the CRT screen is shifted up. When the programmed value is decreased, the display position is shifted down. Any number equal to or less than the contents of R4 and greater than or equal to the R6 may be used.

INTERLACE MODE AND SKEW REGISTER (R8)

The VL68C45R only allows control of the interlace modes as programmed by the low-order two bits of this write-only register. Table 2 shows the interlace modes available to the user. These modes are selected using the two low order bits of this 6-bit write-only register.

TABLE 2: INTERLACE MODE REGISTER

Bit 1	Bit 2	Mode
0	0	Normal Sync Mode
1	0	(Non-interlace)
0	1	Interlace Sync Mode
1	1	Interlace Sync and Video Mode

There are restrictions on the programming of the VL68C45R registers for interlace operation:

1. The Horizontal Total Register (R0) value must be odd (i.e., and even number of character times).
2. For interlace sync and video mode only, the Maximum Scanline Address Register (R9) value must be odd (i.e., an even number of scan lines).
3. For interlace sync and video mode only, the number (Nvd) programmed in to the Vertical Display Register (R6) must be one-half the actual number required. The even-numbered scan lines are displayed in the even field and the off-numbered scan lines are displayed in the odd field.
4. For interlace sync and video mode only, the Cursor Start Register (R10) and Cursor End Register (R11) must both be even or odd, depending on which field the cursor is to be displayed in. A full block cursor will be displayed in both the even and the odd field when the Cursor End Register (R11) is programmed to a value greater than the value in the Maximum Scan Line Address Register (R9).

MAXIMUM SCAN LINE ADDRESS REGISTER (R9)

This 5-bit write-only register determines the number of scan lines per character row, including the spacing, thus controlling operation of the row address counter. The programmed value is a maximum address and is one less than the number of scan lines.

CURSOR CONTROL REGISTERS

CURSOR START REGISTER (R10) AND CURSOR END REGISTER (R11)

These registers allow a cursor of up to 32 lines in height to be placed on any scan line of the character block. Register R10 is a 7-bit write-only register used to define the start scan line and the cursor blink rate. Bits 5 and 6 of the Cursor Start Address Register control the cursor operation as shown in table 3. Non-display, display, and two blink modes (16 times or 32 times the field period) are available. Register R11 is a 5-bit write-only register that defines the last scan cursor.

When an external blink feature on characters is required, it may be

TABLE 3. CURSOR START REGISTER

Bit 6	Bit 5	Cursor Display Mode
0	0	Non-blink
0	1	Cursor Non-display
1	0	Blink, 1/16 field rate
1	1	Blink, 1/32 field rate

necessary to perform cursor blink externally so that both blink rates are synchronized. Note that an invert/non-invert cursor is easily implemented by programming the CRT for a blinking cursor and externally inverting the video signal with an exclusive-OR gate.

CURSOR REGISTER (R14-H, R15-L)

This 14-bit read/write register pair is programmed to position the cursor anywhere in the refresh RAM area, thus allowing hardware paging and scrolling through memory without loss of the original cursor position. It consists of an 8-bit low-order (MA0-MA7) register and a 6-bit high-order (MA8-MA13) register.

START ADDRESS AND LIGHT PEN REGISTERS

START ADDRESS REGISTER (R12-H, R13-L)

This 14-bit write-only register pair controls the first address output by the CRTC after vertical blanking. It consists of an 8-bit low-order (MA0-MA7) register and a 6-bit high-order (MA8-MA13) register. The start address register determines which portion of the refresh RAM is displayed on the CRT screen. Hardware scrolling by character or page may be accomplished by modifying the contents of this register.

LIGHT PEN REGISTER (R16-H, R17-L)

This 14-bit read-only register pair captures the refresh address output by the CRTC on the positive edge of a pulse input to the LPSTB pin. It consists of an 8-bit low-order (MA0-MA7) register and a 6-bit high-order (MA8-MA13) register. Since the light pen pulse is asynchronous with respect to refresh address timing, an internal synchronizer is designed into the CRTC. Due to delays in this circuit, the value of R16 and R17 will need to be corrected in software. (See the bus timing diagram in the Timing Characteristics section).

TABLE 4. VL68C45S INTERNAL REGISTER ASSIGNMENTS, (Note 1)

-CS	RS	Address Register					Register #	Register Name	Program Unit	READ	WRITE	Data Bit							
		4	3	2	1	0						7	6	5	4	3	2	1	0
1	x	x	x	x	x	x			—	—	—								
0	0	x	x	x	x	x	AR	Address Register	—	x	o								
0	1	0	0	0	0	0	R0	Horizontal Total*	Character	x	o								
0	1	0	0	0	0	1	R1	Horizontal Displayed	Character	x	o								
0	1	0	0	0	1	0	R2	Horizontal Sync* Position	Character	x	o								
0	1	0	0	0	1	1	R3	Sync Width	Vertical-Raster, Horizontal-Character	x	o	wv3	wv2	wv1	wv0	wh3	wh2	wh1	wh0
0	1	0	0	1	0	0	R4	Vertical Total*	Line	x	o								
0	1	0	0	1	0	1	R5	Vertical Total Adjust	Raster	x	o								
0	1	0	0	1	1	0	R6	Vertical Displayed	Line	x	o								
0	1	0	0	1	1	1	R7	Vertical Sync* Position	Line	x	o								
0	1	0	1	0	0	0	R8	Interlace & Skew	—	x	o	C1	C0	D1	D0			V	S
0	1	0	1	0	0	1	R9	Maximum Raster Address	Raster	x	o								
0	1	0	1	0	1	0	R10	Cursor Start Raster	Raster	x	o		B	P					
0	1	0	1	0	1	1	R11	Cursor End Raster	Raster	x	o								
0	1	0	1	1	0	0	R12	Start Address (H)	—	o	o								
0	1	0	1	1	0	1	R13	Start Address (L)	—	o	o								
0	1	0	1	1	1	0	R14	Cursor (H)	—	o	o								
0	1	0	1	1	1	1	R15	Cursor (L)	—	o	o								
0	1	1	0	0	0	0	R16	Light Pen (H)	—	o	x								
0	1	1	0	0	0	1	R17	Light Pen (L)	—	o	x								

Note:

1. o = yes; x = no

VL68C45S REGISTER FILE
DESCRIPTIONS (Cont.)
ADDRESS REGISTER (AR)

This is a 5-bit register that is used to select 18 internal control registers (R0-R17). Its contents are the address of one of 18 internal control registers. Programming the data from 18 to 31 produces no results. Access to R0-R17 requires writing the address of the corresponding control register into this register. When RS and CS are LOW, the address is selected.

HORIZONTAL TOTAL REGISTER (R0)

This 8-bit register is used to program the total number of horizontal characters per line, including the retrace period. The data value should be programmed according to the specification of the CRT. When M is the total number of characters, (M-1) must be programmed into this register. When programming for interlace mode, M must be even.

HORIZONTAL DISPLAYED REGISTER (R1)

This 8-bit register is used to program the number of horizontal displayed characters per line. Any 8-bit number that is smaller than that of horizontal total register contents can be programmed.

HORIZONTAL SYNC POSITION REGISTER (R2)

This 8-bit register is used to program horizontal sync position as multiples of the character clock period. Any 8-bit number that is lower than the horizontal total register contents can be programmed. When H is the character number of the horizontal sync position, (H-1) must be programmed into this register. When the programmed value

of this register is increased, the display position on the CRT screen is shifted to the left. When the programmed value is decreased, the position is shifted to the right. Therefore, the optimum horizontal position can be determined by this value.

SYNC WIDTH REGISTER (R3)

This 8-bit register is used to program the horizontal sync (HS) pulse width and the vertical sync (VS) pulse width. The horizontal sync pulse width is programmed in the lower four-bits as multiples of the character clock period (see Table 5); a zero cannot be programmed. The vertical sync pulse width is programmed in the higher four bits as multiples of the raster period (see Table 6). When zeroes are programmed in the higher four bits, a 16-raster period is specified.

VERTICAL TOTAL REGISTER (R4)

This 7-bit register is used to program the total number of lines per frame, including vertical retrace period. The data and its value should be programmed according to the specification of the CRT. When N is the total number of lines, (N-1) must be programmed into this register.

VERTICAL TOTAL ADJUST REGISTER (R5)

This 5-bit register is used to program the optimum number to adjust the total number of rasters per field. This register enables more precise control of the deflection frequency.

VERTICAL DISPLAYED REGISTER (R6)

This 7-bit register is used to program the number of displayed character rows on the CRT screen. Any 7-bit number

that is smaller than that of vertical total register contents can be programmed.

VERTICAL SYNC POSITION REGISTER (R7)

This 7-bit register is used to program the vertical sync position on the screen as multiples of the horizontal character line period. Any number that is equal to or less than the vertical total register content can be programmed. When V is the character number of vertical sync position, (V-1) must be programmed to this register. When programmed value of this register is increased, the display position is shifted up. When the programmed value is decreased, the position is shifted down. Therefore, the optimum vertical position may be determined by this value.

INTERLACE AND SKEW REGISTER (R8)

This register is used to program raster scan mode and skew (delay) of the Cursor signal and Display Enable signals.

INTERLACE MODE PROGRAM BITS (V,S)

Raster scan mode is programmed (see Table 7) by the V and S bits of R8. In the non-interlace mode, duplicate scanning is done of the rasters of even number field and odd number field. In the interlace sync mode, the rasters of the odd number field are scanned in the middle of the even number field. The same character pattern is then displayed in two fields. In the interlace sync and video mode, the raster scan method is the same as in the interlace sync mode, but it is controlled to display different character patterns in two fields.

Table 4 Additional Notes:

1. The registers marked*: (written value) = (specified value) - 1
2. Written value of R9:
 - a) Non-Interlace mode and Interlace Sync Mode (written value Nr) = (specified value) - 1
 - b) Interlace sync and video mode: (Written value Nr) = (specified value) - 2
3. CO and C1 specify skew of CURSOR output signal. DO and D1 specify skew of Display Enable output signal. When S is one, V specifies video mode. S specifies the Interlace sync mode.
4. B specifies cursor blink.
P specifies the cursor blink period.
5. vv0~vv3 specify the pulse width of the vertical sync signal. wh0 ~ wh3 specify the pulse width of the horizontal sync signal.
6. R0 is normally programmed to be an odd number in interlace mode.



VL68C45S

REGISTER FILE DESCRIPTIONS (Cont.)

TABLE 5: PULSE WIDTH OF HORIZONTAL SYNC SIGNAL

VSW/HSW Register (R3)				HSW Pulse Width (multiples of char clock period)
Bit 3	Bit 2	Bit 1	Bit 0	
0	0	0	0	Not Allowed
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

TABLE 6: PULSE WIDTH OF VERTICAL SYNC SIGNAL

VSW/HSW Register (R3)				VSW Pulse Width (multiples of raster period)
Bit 7	Bit 6	Bit 5	Bit 4	
0	0	0	0	16
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

TABLE 7: INTERLACE MODE BITS
(BITS 1 AND 0 of R8)

V Bit 1	S Bit 2	Mode
0	0	Normal Sync Mode
1	0	(Non-interlace)
0	1	Interlace Sync Mode
1	1	Interlace Sync and Video Mode

SKEW PROGRAM BITS
(C1,C0,D1,D0)

These bits are used to program the skew (delay) of the Cursor and Display Enable signals.

Skew of these two kinds of signals is programmed separately. The skew function is used to provide an on-chip delay for the output timing of the Cursor and Display Enable Signals to provide the time required to access refresh memory, character generator or pattern generator, and to ensure that they are

TABLE 8: DISPLAY ENABLE SKEW
BIT (BITS 5 AND 4 OF R8)

D1 Bit 5	D0 Bit 4	Display Enable Signal
0	0	Non-Skew
0	1	One-character Skew
1	0	Two-character Skew
1	1	Non-output

TABLE 9: CURSOR SKEW BITS
(BITS 7 & 6 OF R8)

C1 Bit 7	C0 Bit 6	Display Skew
0	0	Non-Skew
0	1	One-character Skew
1	0	Two-character Skew
1	1	Non-output

VL68C45S REGISTER FILE DESCRIPTIONS (Cont.)

in phase with the serial video signal.

MAXIMUM RASTER ADDRESS REGISTER (R9)

This 5-bit register is used to program the Maximum Raster Address. This register defines total number of rasters per character, including space.

This register is programmed as follows:

1. Non-Interlace Mode,
Interlace Sync Mode: When the total number of rasters is RN, (RN-1) must be programmed.
2. Interlace Sync and Video Mode:
When total number of rasters is RN, (RN-2) must be programmed.

The total number of rasters in non-interlace mode, interlace sync mode and interlace sync and video mode is

TABLE 10: RASTER COUNT IN INTERLACE AND NON-INTERLACE MODES

- 0 _____ Total number of rasters 5
1 _____ Programmed value Nr = 4
2 _____ (The same as displayed
total number of rasters)

3 _____
4 _____

Raster Address

INTERLACE SYNC MODE

- 0 _____ Total number of rasters 5
-----0 programmed value
Nr = 4
1 _____ In the interlace sync
-----1 mode, total number of
rasters in both the
2 _____ even and odd fields is
-----2 ten. On programming,
the half of it is defined
3 _____ as total number of
-----3 rasters.

4 _____
-----4

Raster Address

INTERLACE SYNC AND VIDEO MODE

- 0 _____ Total Number of Rasters 5
-----1 Programmed Value
Nr = 3
2 _____ (Total number of
-----3 rasters displayed in
the even field and the
4 _____ odd field)

Raster Address

In the interlace mode, pulse width is changed + 1/2 raster time when vertical sync signal extends over two fields.

defined as follows in Table 10.

CURSOR START RASTER REGISTER (R10)

This 7-bit register is used to program the cursor start raster address and the cursor display mode. The lower five bits program the raster address and the higher two bits program the display mode (see table 11).

TABLE 11: CURSOR DISPLAY MODE (BITS 6 AND 5 OF R10)

B Bit 6	P Bit 5	Cursor Display Mode
0	0	Non-Blink
0	1	Cursor Non-Display
1	0	Blink, 1/16 Field Rate
1	1	Blink, 1/32 Field Rate

Note:

The blink sequence is follows:

Light	Dark
-------	------

(16 x or 32 x the field period)

CURSER END RASTER REGISTER (R11)

This register is used to program the cursor end raster address.

START ADDRESS REGISTER (R12,R13)

This register pair is used to program the first address of refresh memory read out. Paging and scrolling are easily performed using this register. This register can be read but the higher 2-bits of R12 are always zero.

CURSOR REGISTER (R14, R15)

These two read/write registers store the cursor location. The higher 2 bits of R14 are zero.

LIGHT PEN REGISTER (R16, R17)

These read-only registers are used to capture the detection address of the light pen. The higher 2 bits of R16 are always zero. The value of R16 and R17 needs to be corrected by software because there is a time delay from the address output by the CRT to the signal input to its LPSTB pin that the

light pen detects.

CONSIDERATIONS IN UPDATING REGISTERS

The value programmed into the internal registers directly controls the CRT. Consequently, the display may flicker on the screen when the contents of the registers are changed from the bus side asynchronously with display operation.

RESTRICTIONS ON PROGRAMMING INTERNAL REGISTERS

1. $0 \leq Nhd \leq Nht + 1 \leq 256$
2. $0 \leq Nvd \leq Nvt + 1 \leq 128$
3. $0 \leq Nhsp \leq Nht$
4. $0 \leq Nvsp \leq Nvt$, Note 1
5. $0 \leq NCSTART \leq NCEND \leq Nr$ (non-interlace, interlace sync mode)
 $0, NCSTART \leq NCEND \leq Nr + 1$ (interlace and video mode)
6. $2 \leq Nr \leq 30$
7. $3 \leq Nht$ (except non-interlace mode)
 $5 \leq Nht$ (non-interlace mode only)

UPDATING THE CURSOR REGISTER

Writing into this register at frequent intervals for moving the cursor should be performed during horizontal and vertical retrace periods.

UPDATING THE START ADDRESS REGISTER

Writing into the start address register at frequent intervals for scrolling and paging should be performed during horizontal and vertical display periods.

It is desirable to avoid programming any registers besides the cursor and Start Address Register during display operations.

VL68C45 CHARACTERISTICS

SYSTEM DIAGRAM

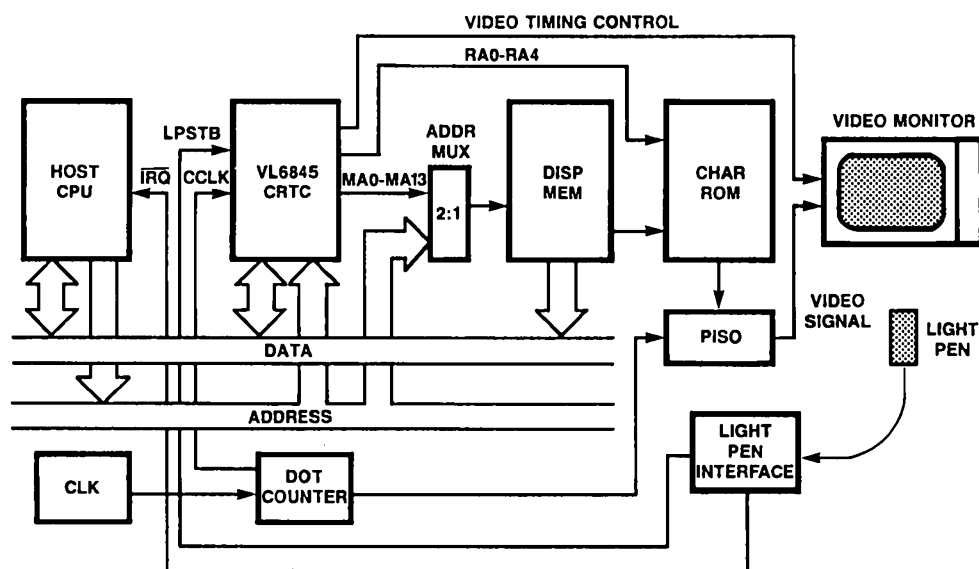
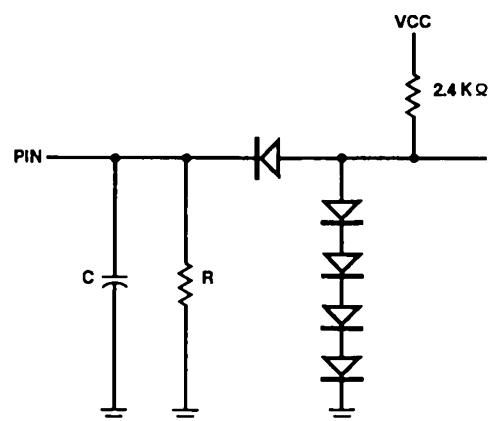


FIGURE 1. TEST LOAD

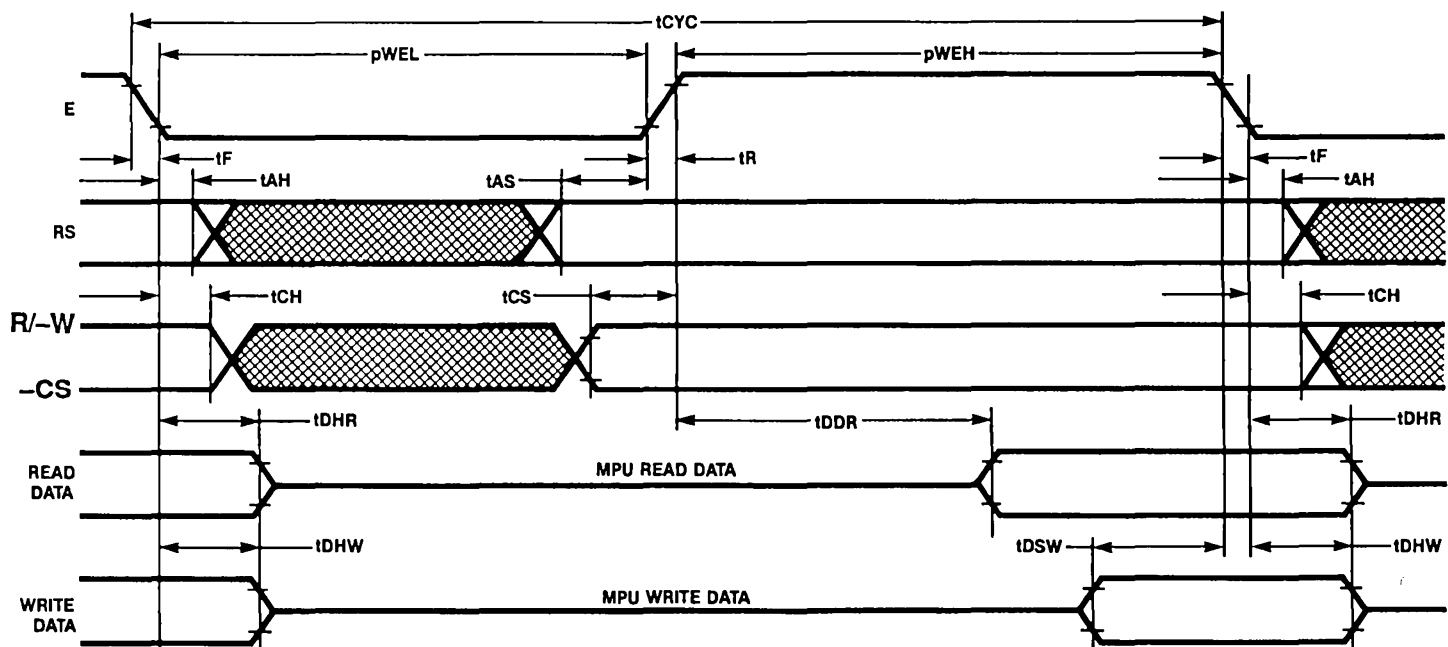


R = 11 KΩ FOR DB0—DB7
R = 24 KΩ FOR ALL OTHER OUTPUTS
C = 130 pF TOTAL FOR DO—D7
C = 30 pF ALL OTHER OUTPUTS

TABLE 12. CRTC BUS TIMING CHARACTERISTICS

Symbol	Parameter	VL68C45R-23 VL68C45S-23		VL68C45R-35 VL68C45S-35 VL68C45R-36 VL68C45S-36 VL68C45R-38 VL68C45S-38		Unit
		Min	Max	Min	Max	
tCYC	Cycle Time	500		333		ns
pWEL	Pulse Width, E Low	190		140		ns
pWEH	Pulse Width, E High	200		150		ns
tR	Clock Rise Time		30		30	ns
tF	Clock Fall Time		30		30	ns
tAH	Address Hold Time (RS)	0		0		ns
tAS	RS Setup Time	40		30		ns
tCS	R/-W, CS Setup	40		30		ns
tCH	R/-W, CS Hold Time	0		0		ns
tDHR	Read Data Hold Time	20	60	20	60	ns
tDHW	Write Data Hold Time	10		10		ns
tDDR	Peripheral Output Delay Time	0	150	0	130	ns
tDSW	Peripheral Setup Time	60		60		ns

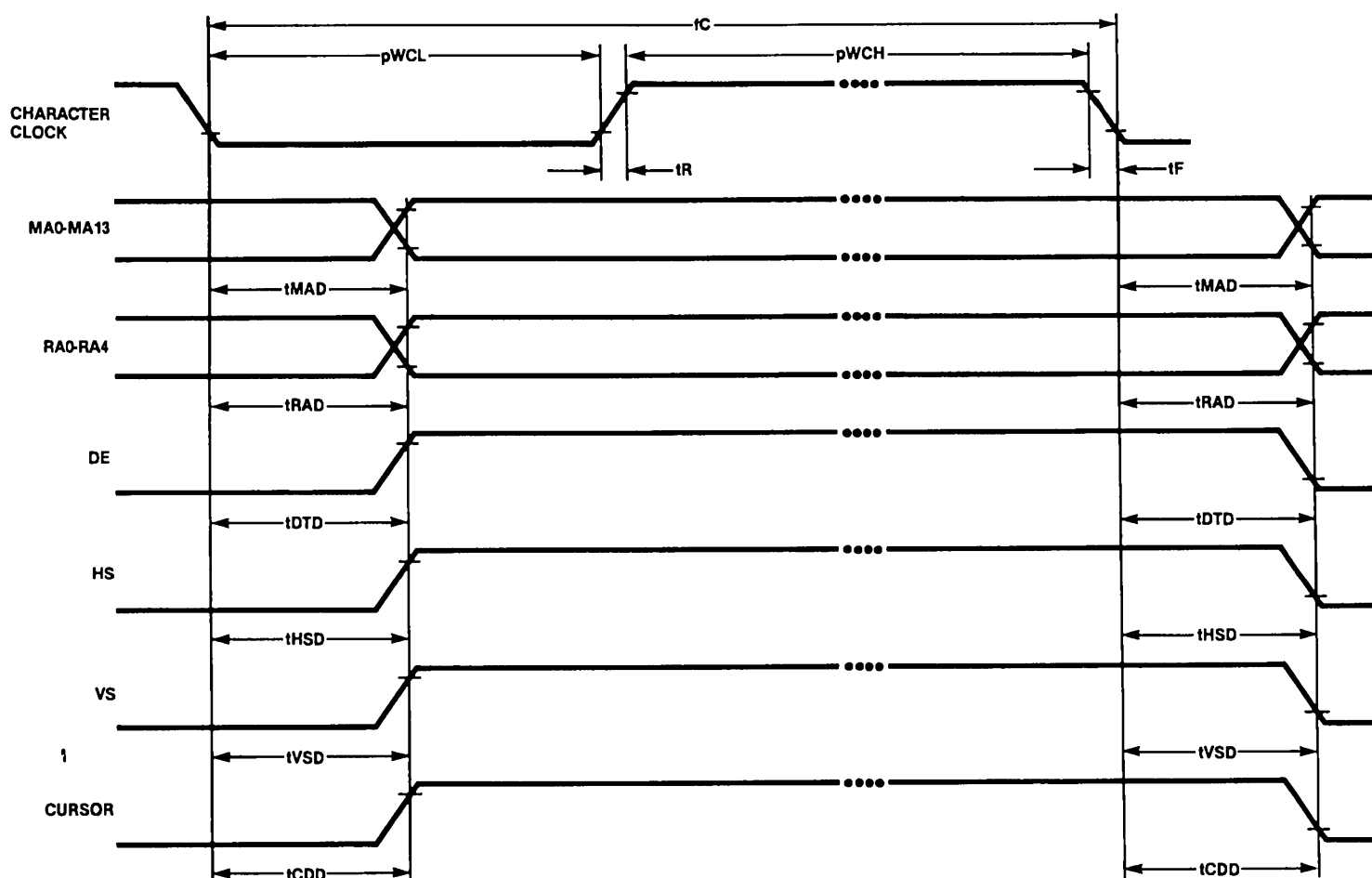
FIGURE 2. BUS TIMING



NOTES:
1. VOLTAGE LEVELS SHOWN ARE $V_L \leq 0.4V$, $V_H \geq 2.4V$
2. MEASUREMENT POINTS SHOWN ARE 0.8V AND 2.0V.

TABLE 13. CRTIC VIDEO TIMING CHARACTERISTICS

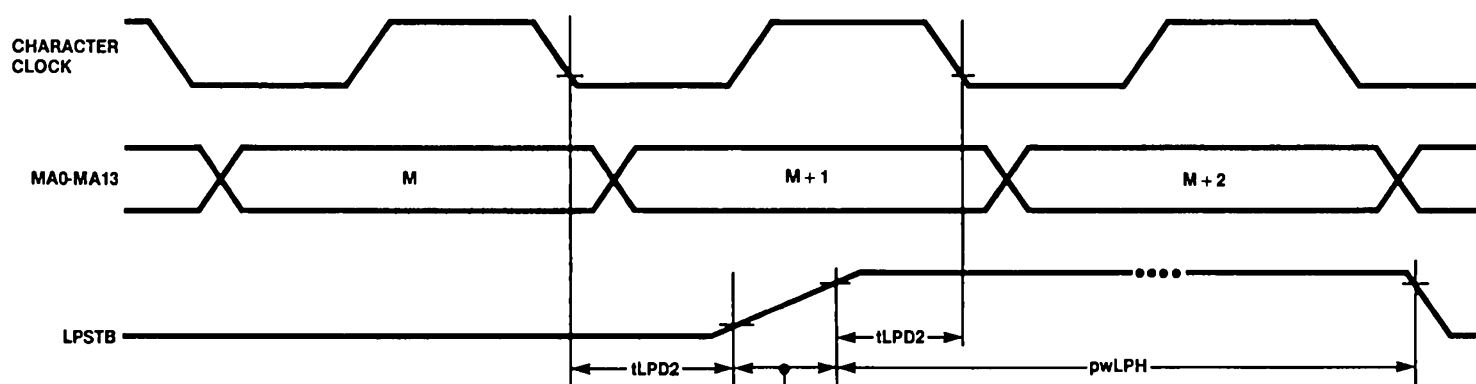
Symbol	Parameter	VL68C45R-23 VL68C45S-23		VL68C45R-35 VL68C45S-35		VL68C45R-36 VL68C45S-36		VL68C45R-38 VL68C45S-38		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
pWCL	Clock Pulse Width, Low	150		100		66		56		ns
pWCH	Clock Pulse Width, High	150		100		72		56		ns
fC	Clock Frequency		3		5		6		8	MHz
tR	Clock Rise Time		20		20		20		15	ns
tF	Clock Fall Time		20		20		8		8	ns
tMAD	Memory Address Delay Time		160		140		100		100	ns
tRAD	Raster Address Delay Time		160		140		100		100	ns
tDTD	Display Timing Delay Time		250		200		100		100	ns
tHSD	Horizontal Sync Delay Time		250		200		100		100	ns
tVSD	Vertical Sync Delay Time		250		200		100		100	ns
tCDD	Cursor Display Delay Time		250		200		100		100	ns

FIGURE 3. VIDEO TIMING


NOTES:
TIMING MEASUREMENTS ARE REFERENCED TO AND
FROM A LOW VOLTAGE OF 0.8 VOLTS AND A HIGH
VOLTAGE OF 2.0 VOLTS UNLESS OTHERWISE SPECIFIED

TABLE 14. CRTC LIGHT PEN TIMING CHARACTERISTICS

Symbol	Parameter	VL68C45R-23 VL68C45S-23		VL68C45R-35 VL68C45S-35 VL68C45R-36 VL68C45S-36 VL68C45R-38 VL68C45S-38		Unit
		Min	Max	Min	Max	
pwLPH	Light Pen Strobe Pulse Width	80		60		ns
tLPD1	Light Pen Display Time 1		120		70	ns
tLPD2	Light Pen Display Time 2		0		0	ns

FIGURE 4: LIGHT PEN TIMING

NOTES:

1. TIMING MEASUREMENTS ARE REFERENCED TO AND FROM A LOW VOLTAGE OF 0.8 VOLTS AND A HIGH VOLTAGE OF 2.0 VOLTS, UNLESS OTHERWISE NOTED.

2. tLPD1 AND tLPD2 ARE THE PERIODS OF UNCERTAINTY FOR THE REFRESH MEMORY ADDRESS.

WHEN THE CRTC DETECTS THE RISING EDGE OF LPSTB IN THIS PERIOD, THE REFRESH MEMORY ADDRESS + 2 IS PUT INTO THE LIGHT PEN REG

**ABSOLUTE MAXIMUM RATINGS**

Ambient Operating Temperature 0°C to 70°C

Storage Temperature -55°C to 150°C

Supply Voltage to Ground Potential -0.3 to +7.0 V

Applied Voltage -0.3 to +7.0 V

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or

any other conditions above those indicated on the operational sections of this specification is not implied and exposure to conditions for extended periods may affect device reliability.

DC CHARACTERISTICS $T_A = 0^\circ\text{C to } 70^\circ\text{C}$, $V_{CC} = \pm 5\%$, unless otherwise specified

Symbol	Parameter	Min.	Typ	Max.	Unit	Conditions
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{IL}	Input Low Voltage	-0.3		0.8	V	
I_{IN}	Input Leakage Current R/-W, RES, RS, CS, LPSTB, CCLK, Ø2			±2.5	µA	
I_{TSI}	Input Leakage Current for Three-State Off DB0 - DB7			±10	µA	$V_{IN} = 0.4\text{ V to } 2.4\text{ V}$ $V_{CC} = 5.25\text{ V}$
V_{OH}	Output High Voltage ILOAD = -205 µA (DB0 - DB7) ILOAD = -100 µA (All Others)	2.4			V	
V_{OL}	Output Low Voltage ILOAD = 1.6 mA			0.4	V	
I_{CC}	Input Power Supply Current			4.0	mA/MHz	
C_I	Input Capacitance Ø2, R/-W, RES, CS, RS, LPSTB, CLK DB0 - DB7			10.0 12.5	pF pF	
C_O	Output Capacitance			10.0	pF	



300/1200 BIT-PER-SECOND MODEM

FEATURES

- FSK and PSK modulators and demodulators, high-band and low-band filters with compromise amplitude and group delay equalizers
- Built-in call progress mode and tone generators for DTMF V.21 and V.22 guard tones
- Bell 212A and CCITT V.21 and V.22 compatible; V.22 notch filters included
- Serial control interface
- Programmable audio output port
- Analog, digital, and remote digital loopback capabilities
- 24-pin DIP and 28-pin plastic leaded chip carrier available

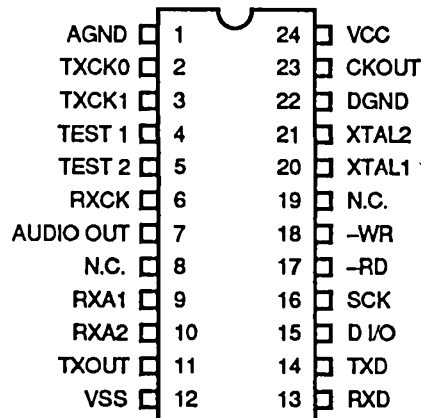
- High level of integration provides a highly cost effective 300/1200 bit-per-second modems
- Eliminates external components, easing design of intelligent modems
- Usable in North American and European modem designs
- Simple board layout
- Simple speaker interface for monitoring phone line
- Testable signal path
- Reduced board area
- Direct replacement for Sierra SC11004 and SC11014

DESCRIPTION

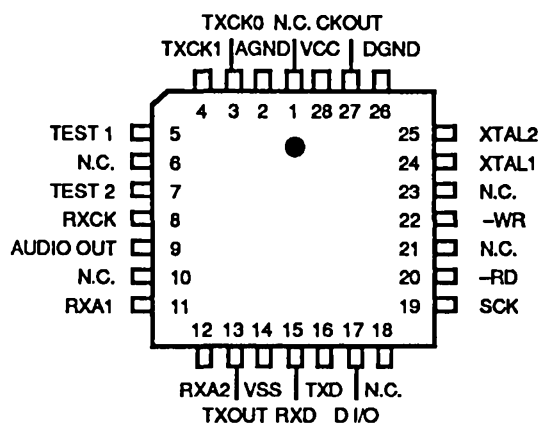
The VL7C212A is a complete 300/1200 bit-per-second modem. All of the signal processing functions needed for a full duplex, 300/1200 bit-per-second 212A (V.21 or V.22) modem, including both FSK and PSK modulators and demodulators and the high-band and low-band filters, are integrated on a single chip. It is built using a three-micron CMOS double-polysilicon process that allows analog and digital functions to be combined on the same chip. This design includes capabilities for progress monitoring and for generating DTMF as well as V.21 or V.22 guard tones. The two-to-four wire hybrid is also included, simplifying the interface to a DAA. The VL7C212A also includes analog loopback and remote digital loopback functions for self-testing.

PIN DIAGRAMS

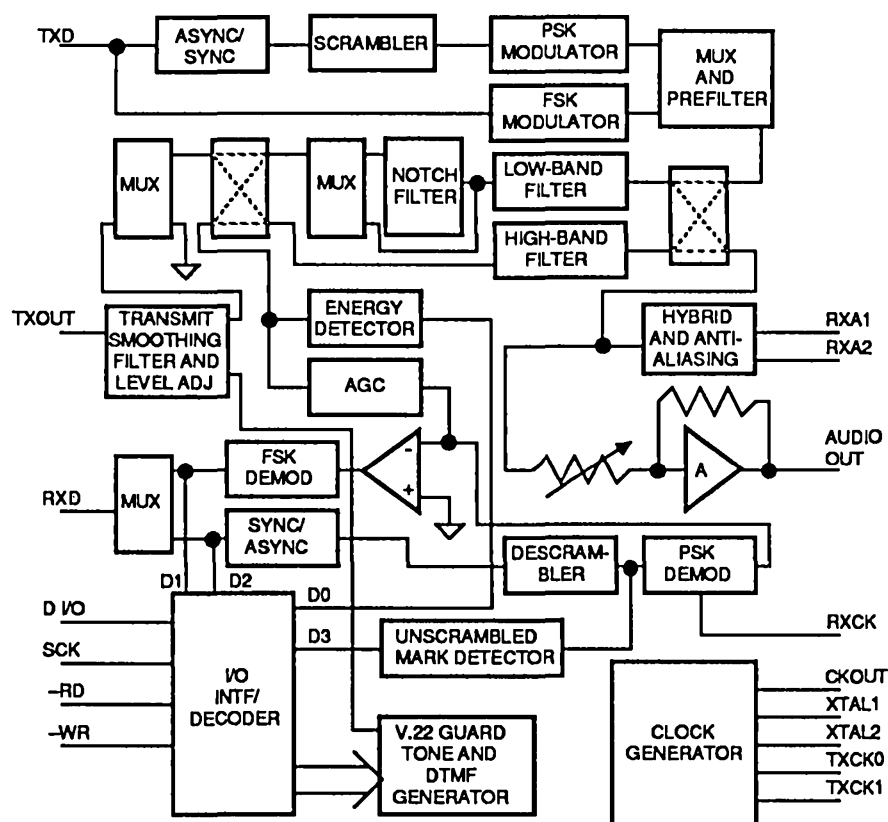
VL7C212A-PC



VL7C212A-QC



BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Package
VL7C212A-PC	Plastic DIP
VL7C212A-QC	Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range is 0°C to +70°C.

SIGNAL DESCRIPTIONS

Signal Name	Pin Number (Note)	Signal Description
TXD	14	Transmit Data- Data on this input is modulated by the modem and output on TXOUT pin. A logic low is space and a logic high is mark.
RXD	13	Receive data- The modem demodulates the received carrier and outputs data on this pin. A logic low level is space and a logic high level is mark. The controller can force the demodulator output to the mark state by sending the code 02.
D I/O	15	Data I/O- Data is shifted in serially when WR is low on rising edges of SCK clock. Data is transferred to a latch when WR goes high. Up to seven data bits can be sent. Input codes are defined in Table 1. Data is read from the modem serially when RD is low, on rising edges of SCK clock. Up to four data bits can be read. Output codes are defined in Table 1.
-WR	18	Strobe output from the controller for shifting data to the modem.
-RD	17	Strobe output from the controller for serially reading data from the modem.
SCK	16	Serial shift clock is applied to this pin. It is normally high until data is sent to, or read from, the modem.
TXOUT	11	Transmit data carrier output.
RXA1, RXA2	9, 10	Received data carriers.
AUDIO OUT	7	Output of the hybrid is passed through a programmable attenuator and brought out on this pin. Four levels of received signal can be programmed using the control codes listed in Table 1.
XTAL1, XTAL	20, 21	Pins for connecting a 7.3728 MHz crystal. An external clock signal can be applied to the XTAL1 pin.
CKOUT	23	Buffered crystal oscillator signal is output on this pin. It can drive one LS TTL load.
TXCKO	2	Transmitter Clock Output- In high speed, synchronous internal mode, this output supplies a 1200 Hz clock to the DTE.
TXCK1	3	In high speed, synchronous external mode this pin is an input for receiving a 1200 Hz clock from the DTE.
RXCK	6	Receiver Clock Output- In high speed, synchronous, external mode, the modem supplies a 1200 Hz clock on this output.
VCC	24	+ 5 V power supply.
VSS	12	- 5 V power supply.
DGND	22	Digital ground.
AGND	1	Analog ground.
TEST1, 2	4, 5	Used by VLSI for testing. Make no connection to these pins. They must be left floating.
N.C.	8, 19	No Connect- No internal connection is made to these pins and they may be left floating.

Note: Pin numbers refer to the DIP package.

FUNCTIONAL DESCRIPTION

With the addition of a digital controller, such as an 8-bit microcontroller and a data access arrangement (DAA), a highly cost effective, integrated, intelligent modem can be built. When used with the VLSI VL7C213A modem controller, which is an 8-bit processor combined with a UART, a complete Hayes command set compatible modem can be configured, taking up a minimum of board area. For stand-alone applications, the VL7C212A modem, the VL7C213 controller, a DAA and an RS232-interface are all that are required.

The VL7C212A is truly a modem on a chip. All of the signal processing functions needed for a full duplex, 300/1200 bps Bell 212A or CCITT V.21 or V.22 modem are integrated on a single chip. It operates in a synchronous or asynchronous mode and handles 8, 9, 10, or 11 bit words.

Like all modems, the VL7C212A needs a controller to determine the mode of operation, initiate the call to the remote modem (either pulse or tone dialing), set up the handshaking sequence with the remote modem, monitor the call progress tones on the line (ringing, busy, answer tone, and voice) and switch into the data mode. A simple four-line serial data interface was designed for the VL7C212A, enabling it to work with just about any 8-bit microcontroller or microprocessor. The control lines are: DATA INPUT/OUTPUT, SHIFT CLOCK, READ and WRITE.

MODEM

Major sections of the VL7C212A modem are a transmitter, a receiver, low-band and high-band filters, a two-to-four wire hybrid, tone generators and interface logic. It also contains an energy detector that's used for detecting the carrier and call progress monitoring and an audio output for monitoring the line.

The VL7C212A modem requires plus and minus five volts and is available in a 24-pin DIP as well as a 28-pin plastic chip carrier with "J" leads for surface mount applications. The transmitter section consists of an async/sync converter, scrambler, PSK modulator, and FSK modulator. In the high speed mode (1200 bps), the PSK modulator is

connected to the filter. In the low speed mode (300 bps), the FSK modulator is connected to the filter.

TRANSMITTER

Since data terminals and computers may not have the timing accuracy required for 1200 bps transmission (0.01%), timing correction on the incoming data stream must be made. The async/sync converter accepts asynchronous serial data clocked at a rate between 1200 Hz + 1%, -2.5%. It outputs serial data at a fixed rate of 1200 Hz +/- 0.01% derived from the master clock oscillator. To compensate for the input and output rate differences, a stop bit is either deleted or inserted when necessary. If the input data rate is slower than the output data rate, a stop bit is inserted. If the input data rate is faster than the output data rate, a stop bit is deleted. The output of the async/sync converter is applied to the scrambler.

The scrambler is a 17-bit shift register clocked at 1200 Hz. Outputs from the 14th and 17th stages are exclusive OR'd and further exclusive OR'd with the input data. The resultant data is supplied to the D input of the shift register. Outputs from the first two stages of the shift register form the dibit that is applied to the PSK modulator. The purpose of the scrambler is to randomize data so that the energy of the modulated carrier is spread over the band of interest. The high-band being centered at 2400 Hz or the low-band, centered at 1200 Hz. A 1200 bps modem actually sends two bits at a time, called a dibit; dibits are sent at 600 baud, the actual rate of transmission; 600 baud is the optimum rate that can be transmitted over the general switched telephone network for a full duplex FDM (frequency division multiplexing) modem because band limit filters in the central office cut off at about 3000 Hz.

The dibit applied to the PSK modulator produces one of four differential phase shifts of the square wave carrier signal (1200 Hz or 2400 Hz) at the 600 Hz baud rate. The resultant waveform is passed through a wave shaping circuit that performs a raised cosine function (this is the shape factor called out in the CCITT V.21 and V.22 specifications,

and it also meets the Bell 212A requirement for optimum transmission). The wave shaped signal is then passed through either the low-band or high-band filter depending upon originate or answer mode selection.

For low speed operation the FSK modulator is used. It produces one of four precision frequencies depending on originate or answer mode and the 1 (mark) or 0 (space) level of the transmit data. The frequencies are produced from the master clock oscillator using programmable dividers. The dividers respond quickly to data changes, introducing negligible bit jitter while maintaining phase coherence. The output of the FSK modulator is applied to the appropriate filter when the low speed mode of the operation is selected.

The filter section consists of low-band (1200 Hz) and high-band (2400 Hz) filters, half-channel compromise amplitude and group delay equalizers for both bands, smoothing filters for both bands and multiplexers for routing of the transmit and receive signals through the appropriate band filters. For CCITT V.21 or V.22 applications, a notch filter is included that can be programmed for either 550 Hz or 1800 Hz. In the call progress monitor mode, the low-band filter is scaled down by a factor of 2.5 to center it over a frequency range of 300 to 660 Hz. Thus, during call establishment in the originate mode, call progress tones can be monitored through the scaled low-band filter and the modem answer tone or voice can be monitored through the unscaled high-band filter.

The low-band filter is a 10th order switched-capacitor band-pass filter with a center frequency of 1200 Hz. In the originate mode, this filter is used in the transmit direction; in the answer mode it is used in the receive direction. When analog loopback is used in the originate mode, this filter, together with the low-band delay equalizer, is in the test loop. In the call progress monitoring mode the filter response is scaled down by 2.5, moving the center frequency to 480 Hz.

The low-band delay equalizer is a 10th order switched-capacitor all-pass filter that compensates for the group delay variation of the low-band filter and half of the compromise line characteristics,



producing a flat delay response within the pass-band.

The high-band filter is a 10th order switched-capacitor band-pass filter with a center frequency of 2400 Hz. In the answer mode, this filter is used in the transmit direction; in the originate mode, it is used in the receive direction. When analog loopback is used in the answer mode, this filter, together with the high-band delay equalizer, will be in the test loop.

The high-band delay equalizer is a 10th order switched-capacitor all-pass filter that compensates for the group delay variation of the high-band filter and half of the compromise line characteristics, producing a flat delay response within the pass-band. The transmit smoothing filter is a second order low-pass switched-capacitor filter that adds the modem transmit signal to the DTMF (V.21 or V.22) guard tones. It also provides a 3 dB per step programmable gain function to set the output level.

RECEIVER

The receiver section consists of an energy detector, AGC, PSK demodulator, FSK demodulator, descrambler, and sync/async converter.

The received signal is routed through the appropriate band-pass filter and applied to both the energy detector and AGC circuit. The energy detector is based on a peak detection algorithm. It provides a detection within 17 to 24 ms. It is set to turn on when the signal exceeds -43 dBm and turn off when the signal falls below -48 dBm. A 2 dB minimum hysteresis is provided between the turn on and turn off levels.

The AGC circuit is a programmable gain amplifier that covers a range of 28 dB in seven steps. The gain is controlled by a 3 bit up/down counter. Output of the AGC amplifier is rectified and compared with two preset levels corresponding to desired high and low limits. Outputs of the comparators control the up/down counter such that the received signal is amplified to the desired level.

The PSK demodulator uses a coherent demodulation technique. Output of the AGC amplifier is applied to a dual phase splitter that produces an in-phase and 90 degree out of phase component. These components are then demodu-

lated to baseband in a mixer stage where individual components are multiplied by the recovered carrier. The baseband components are low-pass filtered to produce I and Q (In-phase and Quadrature) channel outputs. The I and Q channel outputs are rectified, summed, and passed through a band-pass filter giving a 600 Hz signal. This signal is applied to a digital phase lock loop (DPLL) to produce a baud rate clock. Using the recovered clock signal, the I and Q channels are sampled to produce the received dibit data. The recovered carrier for the demodulator is generated by another PLL which is controlled by the amplitude of the error signal formed by the difference of the I and Q outputs.

The descrambler is similar to the scrambler. The received dibit data is applied to the D input of a 17 bit shift register clocked at 1200 Hz. Outputs from the 14th and 17th stages are exclusive OR'd and further exclusive OR'd with input data to produce received data.

In the asynchronous mode, data from the descrambler is applied to the sync/async converter to reconstruct the originally transmitted asynchronous data. For data which had stop bits deleted at the transmitter (overspeed data), these stop bits are reinserted. Underspeed data is passed essentially unchanged. Output of the sync/async converter along with the output of the FSK demodulator is applied to a multiplexer. The multiplexer selects the appropriate output, depending on the operating speed, and outputs received data on the RXD pin.

For low speed operation, the FSK demodulator is used. The output of the AGC amplifier is passed through a zero crossing detector and applied to a counter that is reset on zero crossings. The counter is designed to cycle at a rate four times faster than the carrier signal. The counter output is low-pass filtered and hard limited to generate FSK data.

HYBRID

The signal on the phone line is the sum of the transmit and receive signals. The hybrid subtracts the transmitted signal from the signal on the line to form the received signal. It is important to match

the hybrid impedance as closely as possible to the telephone line to produce only the received signal. This matching is provided by an external resistor connected between the RXA1 and RXA2 pins on the VL7C212A. The filter section provides sufficient attenuation of the out of band signals to eliminate leftover transmit signals from the received signal. The hybrid also acts as a first order low-pass antialiasing filter.

tone generator

The tone generator section consists of a DTMF generator and a V.21 (or V.22) guard tone generator. The DTMF generator produces all of the tones corresponding to digits 0 through 9 and * and # keys. The V.21 (or V.22) guard tone generator produces either 550 Hz or 1800 Hz. Selection of either the 550 Hz or 1800 Hz tone will cascade the corresponding notch filter with the low-band filter. The tones are selected by applying appropriate codes through the Data I/O pin. Before a tone can be generated, tone mode must be selected. Facility is also provided to generate single tones corresponding to the individual rows or column of the DTMF signal.

AUDIO OUTPUT STAGE

A programmable attenuator that can drive a load impedance of 50 K Ω is provided to allow monitoring of the received line signal through an external speaker. The attenuator is connected to the output of the hybrid. Four levels of attenuation: no attenuation, 6 dB attenuation, 12 dB attenuation and squelch are provided through the ALC1, ALC0 and audio output level control codes. Output of the attenuator is available on the audio output pin where an external audio amplifier (LM386 type) can be connected to drive a low impedance speaker. The output can directly drive a high impedance transducer, but the volume level will be low.

VL7C213 AND VL7C214 CONTROLLERS

The VL7C213 modem controller, implemented in VLSI's two-micron CMOS process, was designed specifically to handle all of the modem control functions, as well as the interface to a system bus. Besides including an 8-bit microprocessor, 8K by 8 bytes of ROM,

and 128 by 8 bytes of RAM, it also contains the functionality of a VL82C50 UART, greatly simplifying the interface to a parallel system bus, such as used in an IBM PC-compatible personal computer (PC). In fact, a complete, Hayes compatible modem for the PC consists of the VL7C213 controller, the VL7C212A modem and the DAA. All of the popular communications software written for the PC will work with the VL7C212A/VL7C213 set.

Another version of the controller, the VL7C214, is intended for RS-232 applications. It contains the same processor, memory, and UART as the VL7C213 and has the same interface to the modem chip. The difference is that the UART is turned around so that serial data from the RS-232 port is converted to parallel data handled by the internal processor. Pins are provided for connecting the familiar switches and indicator lamps found on most stand-alone modems, although the switches and lamps are not needed for operation. All of the switch settings can be done through software.

The VL7C214 provides a standard five volt logic level interface. RS-232 drivers are required to interface to the port. Like the VL7C213, the VL7C214 comes preprogrammed with the Hayes "AT" command set, and when used with the VL7C212A modem, emulates a Hayes-type stand-alone modem. The VL7C213 and VL7C212A emulate a Hayes-type IBM PC plug-in card modem. But the chip set is by no means limited to implementing a Hayes-type smart modem. VLSI is in the custom IC business and both chips were designed with this in mind. For example, only about 6K bytes of the VL7C213's ROM is used for the handshaking and smart modem code, leaving 2K bytes for additional features that a customer may specify. Since the controller is ROM programmable, any command set, not just the Hayes "AT" set, can be implemented.

Both the VL7C213 and VL7C214 require plus five volts and are available in either a 28-pin DIP or a 28-pin plastic chip carrier with "J" leads for surface mount applications. Besides the four-line interface for the VL7C212A modem, the

VL7C213 controller has an 8-bit data port, three address lines, a chip select input, an interrupt line, and the DOST and DIST control lines found in the 8250B UART. It also has control lines for ring indication, the off-hook relay and a data/voice relay; these three lines connect to the DAA.

In the VL7C214, the 8-bit port becomes the switch input lines and the address, chip select, DIST and DOST lines become the six lines for the RS-232 interface. These six lines are also used to drive the LEDs. Internally, all of these lines are treated as programmable I/O ports under software control. The primary difference between the VL7C213 and VL7C214 is the ROM code. It also contains the same modem and DAA interface lines as the VL7C213.

The VL7C213 and VL7C214 are truly ASIC controllers. They are designed to control a modem or other peripheral that operates at a moderately slow data rate up to 1200 bits per second. The VL7C213 allows a slow peripheral to interface to a high speed bus, without making the main processor slow down.

This is done through the UART interface and the on-chip registers which look somewhat like dual port registers. The main processor can write to and read from them at will, while the on-chip controller can do the same. The controller was designed this way because most communication software has to have unrestrained access to the UART registers. To make the VL7C213 compatible with this software, the registers were included.

The internal processor monitors the registers to determine the mode of operation. Command mode or data mode: at power-up it is automatically put in the command mode and it looks for instructions. Once carrier is detected, it goes into the data mode, and stays there until escape sequence is three "+" signs (+++) in the default mode, but it can be changed in software.

The actual processor contains an 8-bit data path and can execute 19 instructions with five different addressing modes: direct, indirect, immediate, register direct, and register indirect. There is 8K by 8 of ROM on-chip for

program storage.

To the system bus, the VL7C213 looks and acts just like a VL82C50 UART. All of the communications software written for this UART will work with the VL7C213 and VL7C214. The VLSI chip set is a Hayes-type modem in two chips.

The VL7C212A AND VL7C213/VL7C214 System

The only external components required by the VL7C212A are the 600 Ω line matching resistor, a 7.3728 MHz crystal (a standard frequency) and a 20 pF capacitor from each leg of the crystal to ground. That's all! If it is desired to drive a speaker to monitor the line, an amplifier like the LM386 can be added, but the output provided on the VL7C212A can directly drive a high impedance (50 k Ω) earphone-type transducer.

The VL7C213 modem controller's clock in line is driven by the VL7C212A's clock out line, so only one crystal is needed. The VL7C213 interfaces directly to an IBM PC bus — no buffers are required. The only external parts may be an eight input NAND gate for COM1 and COM2 decoding inside the PC.

For tone dialing, the controller sends a code to the modem chip which in turn puts out the called for DTMF tone on the line via the on-chip DTMF generator. For pulse dialing, the controller pulses the OH (off-hook) relay. Both dialing modes work with the built-in call progress algorithm so they won't start dialing until a dial tone is detected.

All modems require a DAA. A DAA (data access arrangement) is a piece of equipment required by the FCC to connect anything to the general switched telephone network. It consists of an isolation transformer, typically 600 Ω to 600 Ω ; a relay for disconnecting the modem from the line; a ring detector, typically an opto-isolator; and high voltage surge protectors. The DAA has to be FCC registered and this can be done by any of many consultants and labs around the country. Another alternative is to buy a DAA, supplied by several manufacturers.

212A is a Bell specification that calls for 1200 bit per second, full or half duplex data transmission with a fallback mode

of 300 baud (Bell 103). It is not 1200 baud; the spec calls for transmission of dibits, or 2 bits per baud so the 1200 bps transmission takes place at 600 baud. The same is true for V.22; it's 1200 bps or 600 baud. V.22 does not call for a 300 baud fallback; the CCITT standard for 300 baud is V.21. It is not a required fallback for V.22, however, it is included in the VL7C212A.

V.22 also calls for guard tones to be sent along with the data. In most of Europe the tone is 1800 Hz except in Sweden where 550 Hz is used. The VL7C212A modem has the 550 Hz and 1800 Hz tone generators built in as well as the 550 and 1800 Hz notch filter to remove the guard tone when in the receive mode.

All modems require a hybrid. Hybrid is a term used to describe a circuit,

passive or active, that takes the separate transmit and receive signals and combines them to go over the phone line. In the VL7C212A, this is done with op amps, but the separate signals (TXOUT and RXA2) are also brought out so an external hybrid can be used, if desired. The combined signal comes out on the RXA1 pin and a matching resistor (typically 600 Ω) is connected between RXA1 and RXA2.

TABLE 1. DEFINITION OF I/O CODES

1. Instructions to the modem IC

Data on the D I/O pin is shifted into the modem when WR is low, on rising edges of the SCK clock. Data is transferred into a latch when WR goes high. (See Figure 2 for write cycle waveforms.) Up to seven data bits (D0--D6) can be sent to the device. These bits control the operating modes of the modem as show below:

D6	D5	D4	D3-D0	Mode/Function
				Non-Tone Mode:
0	1/0	0	0	Reset (set default values)
0	1/0	0	1	Tone On/Off
0	1/0	0	2	Force Receive Data to Mark Off/On
0	1/0	0	3	TLC0 Transmit Level Control Bit 0 (default 0)
0	1/0	0	4	TLC1 Transmit Level Control Bit 1 (default 0)
0	1/0	0	5	TX Transmitter On/Off
0	1/0	0	6	ALB Analog Loopback On/Off
0	1/0	0	7	CPM Call Progress Monitor Mode On/Off
0	1/0	0	8	Connection Indicator (CI) On/Off
0	1/0	0	9	ALCO Audio Output Level Control Bit 0 (default 0)
0	1/0	0	A	ALC1 Audio Output Level Control Bit 1 (default 0)
0	1/0	0	B	WLS0 Word Length Select 0 (default 0)
0	1/0	0	C	WLS1 Word Length Select 1 (default 1)
0	1/0	0	D	Sync/Async
0	1/0	0	E	LS/HS: Low Speed/High Speed
0	1/0	0	F	A/O: Answer/Originate
0	1/0	1	0	Transmit Mark On/Off
0	1/0	1	1	Transmit Space On/Off
0	1/0	1	2	Scrambler Disable On/Off
0	1/0	1	3	DLB Digital Loopback On/Off
0	1/0	1	4	TXDP Transmit Dotting Pattern On/Off
0	1/0	1	5	Locked/Internal
0	1/0	1	6	External/Slave
0	1/0	1	7	2100 Hz Tone On/Off (Must select low speed mode for operation)
0	1/0	1	8	1300 Hz Tone On/Off (Must select low speed mode for operation)
0	1/0	1	9	V.21 On/Off (Must select low speed mode for operation)

TABLE 1. DEFINITION OF I/O CODES (Cont.)

D6	D5	D4	D3-D0	Mode/Function
1	1/0	0	0	Tone Mode: Dial 0
1	1/0	0	1	Dial 1
1	1/0	0	2	Dial 2
1	1/0	0	3	Dial 3
1	1/0	0	4	Dial 4
1	1/0	0	5	Dial 5
1	1/0	0	6	Dial 6
1	1/0	0	7	Dial 7
1	1/0	0	8	Dial 8
1	1/0	0	9	Dial 9
1	1/0	0	A	Dial *
1	1/0	0	B	Dial #
1	1/0	0	C	Output 550 Hz and Insert 550 Hz Notch in Low-Band Filter
1	1/0	0	D	Output 1800 Hz and Insert 1800 Hz Notch in Low-Band Filter
1	1/0	0	E	Row Disable On/Off
1	1/0	0	F	Column Disable On/Off

WLS1	WLS0	Word Length
0 0	0	8 Bits
0 1	1	9 Bits
1 0	0	10 Bits (default)
1 1	1	11 Bits

TLC1	TLC0	Transmitter Output Level (dBm) at the Phone Line
0 0	0	-12 (default)
0 1	1	-9
1 0	0	-6
1 1	1	0

ALC1	ALC0	Audio Output Level
0 0	0	Output Off (default)
0 1	1	12 dB Attenuation
1 0	0	6 dB Attenuation
1 1	1	No Attenuation

2. Information from the Modem IC

Data is read serially from the modem when RD is low, on rising edges of the SCK clock. (See Figure 1 for read cycle waveforms.) Up to four data bits (D0--D3) can be read as defined below:

D0 Energy Detect 0 - No Energy 1 - Energy Present

In the CPM mode, the energy detector is connected to the output of the high-band filter, if ALB is off, or the scaled low-band filter, if ALB is on.

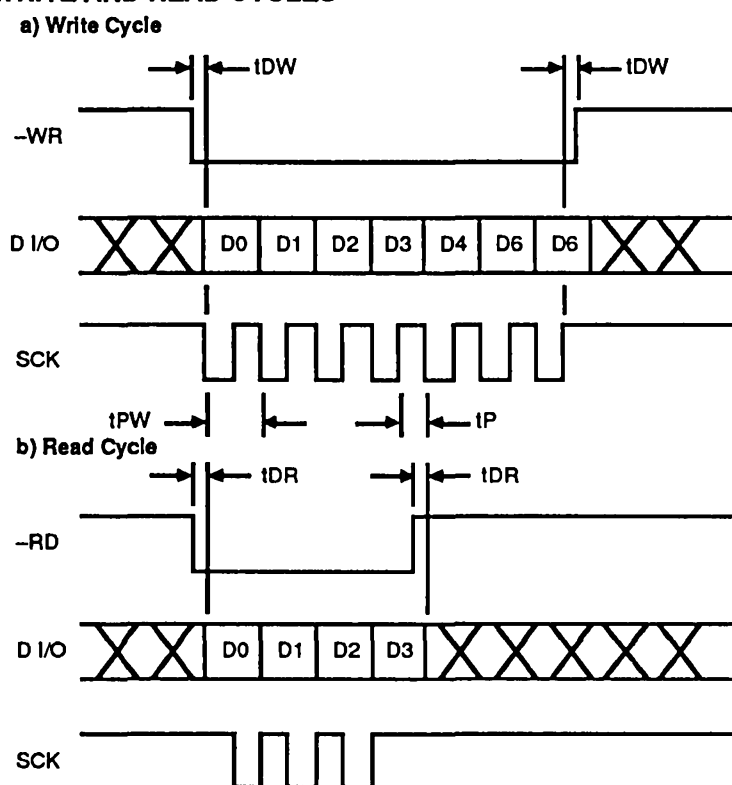
D1	Received Data (FSK)	1 - Mark	0 - Space
D2	Received Data (PSK)	1 - Mark	0 - Space
D3	Unscrambled Mark	1 - Detected	0 - Not Detected

Notes:

1. Default values for the operating modes on power-up are those shown to the right of the "/" unless otherwise specified.
2. Data is shifted in and out of the modem with LSB first.

TABLE 2. AC CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Units	Conditions
tDW	Delay Time to Write	200			ns	
tDR	Delay Time to Read	200			ns	
tPW	Complete SCK Cycle	1.0			ms	
tP	SCK High Pulse Duration	30		70	%	Duty Cycle
fC	Crystal Frequency	7.3721	7.3728	7.3735	MHz	

FIGURE 1. WAVEFORMS FOR WRITE AND READ CYCLES

DTMF GENERATOR CRYSTAL FREQUENCY = 7.372800 MHz $\pm 0\%$

Parameter	Nominal Frequency	Allowable Error	Actual Error
Row 1	697 Hz	$\pm 1\%$	+ 0.17%
Row 2	770 Hz	$\pm 1\%$	- 0.26%
Row 3	852 Hz	$\pm 1\%$	+ 0.16%
Row 4	941 Hz	$\pm 1\%$	- 0.47%
Column 1	1209 Hz	$\pm 1\%$	- 0.74%
Column2	1336 Hz	$\pm 1\%$	-0.89%
Column 3	1477 Hz	$\pm 1\%$	- 0.01%
Guard Tones	550 Hz	± 20 Hz	- 1.4 Hz
	1800 Hz	± 20 Hz	+ 7 Hz

DTMF GENERATOR (Cont.)

Parameter	Conditions	Min	Typ	Max	Units
Second Harmonic Distortion	VCC = + 5 V		- 40		dB
Row Output Level	VSS = - 5 V		0		dBm
Column Output Level	TLC0 = 1		2		dBm
550 Hz Guard Tone Level	TLC1 = 1		- 3		dB (Note 2)
1800 Hz Guard Tone Level	Measured at TXOUT Pin		- 6		dB (Note 2)

Note: Guard tone levels are referenced to the TX signal level. When guard tones are added, the TXOUT level is adjusted to maintain a constant level on the line. For 1800 Hz, the adjustment is -0.97 dB; for 550 Hz, the adjustment is -1.76 dB, per the CCITT specification.

MODEM TRANSMIT SIGNALS CRYSTAL FREQUENCY = 7.372800 MHz ±0%

Mode		Bell 103		CCITT V.21		Bell 212A / CCITT V.22	
		Nominal	Actual	Nominal	Actual	Nominal	Actual
Answer	Mark	2225 Hz	2226 Hz	1650 Hz	1649.4 Hz	2400 Hz	2400 Hz
	Space	2025 Hz	2024.4 Hz	1850 Hz	1850.6 Hz		
Originate	Mark	1270 Hz	1269.4 Hz	980 Hz	978.34 Hz	1200 Hz	1200 Hz
	Space	1070 Hz	1070.4 Hz	1180 Hz	1181.53 Hz		
Calling Tone				1300 Hz	1301.7 Hz	1300 Hz	1301.7 Hz
Answer Tone				2100 Hz	2096.9 Hz	2100 Hz	2096.9 Hz

RECEIVER

Parameter	Conditions	Min	Typ	Max	Units
Input Signal Range	At RXA1 (pin 9)	- 45		0	dBm
Intra - Character Bit Rate	At RXD (pin 13)	1170	1200	1224	bps
Carrier Detect	At RXA1 (pin 9)	- 48		- 43	dBm
Carrier Detect Hysteresis		2			dB
Carrier Detect Delay	For 103, 212A and V.22	10	20	30	ms
Carrier Detect Hold	For 103, 212A and V.22	15	20	24	ms
Carrier Detect Delay	For V.21 mode	15	30	40	ms
Carrier Detect Hold	For V.21 mode	20	30	50	ms

TRANSMITTER

Parameter	Conditions	Min	Typ	Max	Units
Input Character Length	Start Bit + Data Bit + Stop Bit	8		11	bits
Intra - Character Bit Rate	At TXD (pin 14)	1170	1200	1212	bps
Input Break Sequence Length	M = Character Length	2M + 3			bits
Output Level Tolerance			± 1		dB

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature
Under Bias: -10°C to +80°C

Storage Temperature
Range: -65°C to +140°C

Maximum Supply
Voltage: VCC = +7.0 V, VSS = -7.0 V

Input Voltage Range:
Analog Pins; VSS -0.6 V to VCC+0.6 V
Digital Pins; DGND-0.6 V to VCC+0.6 V

Maximum Power
Dissipation @25°C: 500 mW

Stresses above those listed under
"Absolute Maximum Ratings" may
cause permanent damage to the
device. These are stress ratings only.
Functional Operation of this device at
these or any other conditions above

those in the operational sections of this
specification is not implied and expo-
sure to absolute maximum rating
conditions for extended periods may
effect device reliability.

DC CHARACTERISTICS TA= 0°C to 70° C unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Units	Conditions
VCC	Positive Supply Voltage	4.5	5.0	5.5	V	
VSS	Negative Supply Voltage	-4.5	-5.0	-5.5	V	
ICC	Quiescent Current		15		mA	VCC = 5 V
ISS	Quiescent Current			15	mA	VSS = -5 V
VIH	High Level Input Voltage	2.0			V	Digital Signal Pins: -RD, -WR, DI/O, SCK, TXCK1, TXD
VIL	Low Level Input Voltage			0.8	V	Digital Signal Pins: -RD, -WR, DI/O, SCK, TXCK1, TXD
VOH	High Level Output Voltage	4.0 2.0			V V	@IOH= 40 µA (D S Pins: D I/O, CKOUT, @IOH= 500 µA RXD, TXCK0, RXCK)
VOL	Low Level Output Voltage			0.4	V	@IOL=160 µA (D S Pins: D I/O, CKOUT, RXD, TXCK0, RXCK)
VOM	Maximum Output Signal	4.0			Vp-p	TXOUT, RL=1200 Ω (TLC1=1, TLC0=0)
VOM	Maximum Output Signal	1.0			Vp-p	Audio Out, RL= 50 kΩ
VIM	Maximum Input Signal			2.0	Vp-p	RXA1, RXA2



PARALLEL BUS MODEM CONTROLLER

FEATURES

- Direct interface to VL7C212A single-chip modems
- Complete Hayes AT command set in firmware
- Built-in UART
- Direct IBM PC bus interface
- Two-micron CMOS process
- 28-pin DIP or PLCC package
- Complete intelligent modem in two ICs
- Compatible with industry-standard software
- Replacement for Sierra SC11007
- Reduces board space and component count requirements

DESCRIPTION

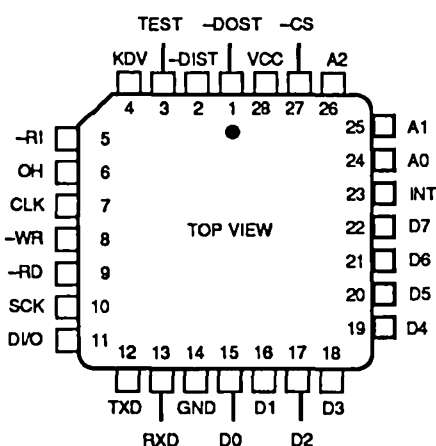
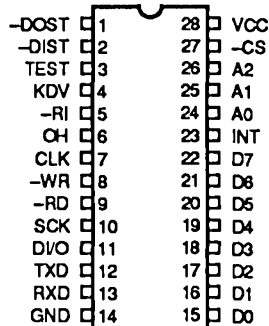
The VL7C213 Parallel Bus Modem Controller is specifically designed to control the VL7C212A single-chip, 300/1200 bit-per-second modem. Built with an advanced two-micron CMOS process, the VL7C213 provides a highly cost effective solution for interfacing a modem IC to a system bus. When connected to the VL7C212A, with the addition of a data access arrangement (DAA), the VL7C213 implements a Hayes-type smart modem for board-level, integral-modem applications. Because the VL7C213 fully emulates the functionality of the VL82C50 UART and includes data bus transceivers, it can be directly interfaced to a computer's parallel data

bus (in particular to the bus of the IBM PC, XT or AT). All of the popular communications software written for the PC will work with the VL7C213/VL7C212A chip set. In addition to including the functionality of the VL82C50 UART, the VL7C213 contains an 8-bit microprocessor, 8K by 8 bits of ROM and 128 by 8 bits of RAM.

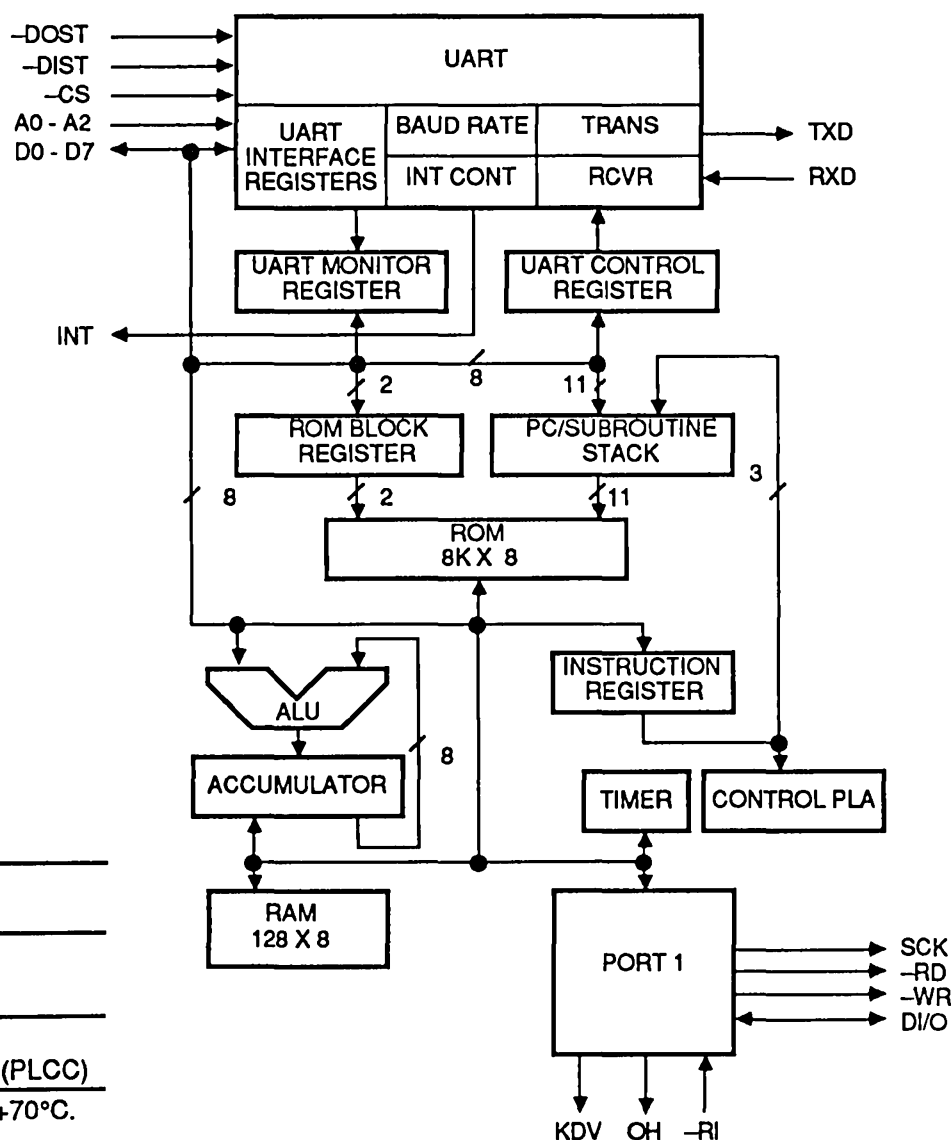
For specific high-volume applications, the control program can be modified by VLSI to include additional command functions.

PIN DIAGRAMS

VL7C213



BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Package
VL7C213-PC	Plastic DIP
VL7C213-QC	Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range is 0°C to +70°C.

SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Description
-DOST	1	The CPU can write data or control words into a selected register of the VL7C213 when -DOST is low and the chip is selected. Data is latched on the rising edge of the signal.
-DIST	2	The CPU can read data or status information from a selected register of the VL7C213 when -DIST is low and the chip is selected.
TEST	3	When the test input is high, the VL7C213 enters a test mode (used for factory testing only). No connection must be made to this pin. It must be left open for normal operation.
KDV	4	This output controls the operation of the data/voice relay. When low, the data/voice relay is off and the phone line is connected to the phone set. During a data call, the VL7C213 makes this output high to operate the data/voice relay, disconnecting the phone set from the phone line. It may also be used to drive a relay for multi-line phone applications to close the A and A1 leads.
-RI	5	The output of the ring detector in the DAA is connected to this input. A low level on this input indicates the "On" duration of the ring cycle. This is a Schmitt-trigger input, allowing for slow rising and falling signals on this pin.
OH	6	This output controls the operation of the hookswitch relay in the DAA. During a data call, this output is high. It operates the hookswitch relay which causes the phone line to be seized. During rotary dialing, the VL7C213 pulses this output at a rate of 10 pulses per second with appropriate Mark/Space ratio depending on 212A or V.22 mode.
CLK	7	A 7.3728 MHz clock signal must be connected to this input. Normally, the CKOUT pin of the VL7C212A modem is connected to this pin. All internal timing is derived from this clock. This clock must be adjusted to within 0.01%.
-WR	8	This pin is used to initiate writing of data to the VL7C212A modem. On power-up, it is an input for a brief time in which the VL7C213 reads the carrier status switch connected to this pin. If the switch is closed to ground through an 18 K Ω resistor, the VL7C213 sets the Received Line Signal Detect (RLSD) Bit in the Modem Status Register. If the switch is open, the VL7C213 resets this bit and writes the actual status of the carrier detector during a data call. If no switch is used, an internal pull-up sets the status during power-up to the default state (pull-up to VCC) which is to follow the remote modem's carrier.
-RD	9	This pin is used to initiate reading of data from the VL7C212A modem. On power-up, this pin is an input for a brief time in which the VL7C213 reads the DTR status switch connected to this pin. If this switch is open, the VL7C213 reacts to the status of the DTR bit in the UART Modem Control Register. If the switch is closed to ground through 18 k Ω , the VL7C213 ignores the state of the DTR bit. When the switch is open, writing a zero to the DTR bit in the Modem Control Register forces the VL7C213 into the command state and when on-line, causes it to hang up. If no switch is used, an internal pull-up to VCC sets the status during power-up to the default state (to follow the DTR status).
SCK	10	The VL7C213 supplies a shift clock on this pin to the VL7C212A modem for reading or writing data. On power-up, this pin is an input for a brief time in which the VL7C213 reads the Bell/CCITT select switch connected to this pin. If this switch is open, Bell protocol is selected. If this switch is closed to ground through 18 k Ω , CCITT V.22 protocol is selected. If no switch is used, an internal pull-up sets the status during power-up to the default state (212A mode).
DI/O	11	The VL7C213 shifts data serially out of this pin to VL7C212A during a write operation and shifts data serially into this pin during a read operation from the VL7C212A. On power-up this pin is an input for a brief time in which the VL7C213 reads the Make/Break ratio select switch connected to this pin for selecting the pulse dialing standard. With the switch open, the Bell standard 39% Make, 61% Break is selected. With the switch closed to ground through 18 k Ω , the CCITT standard 33% Make, 67% Break is selected. If no switch is used, an internal pull-up sets the status during power-up to the default state (Bell standard).

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Description
TXD	12	This pin is a serial output pin. During a data call, after the connection is established, the VL7C213 converts parallel data received from the computer bus and outputs it in a serial, asynchronous format to the VL7C212A modem for modulation. At all other times the VL7C213 holds this output in the Mark (high) condition.
RXD	13	Demodulated data from the VL7C212A modem is received on this pin during a data call. A high level is considered Mark and a low level is Space. The VL7C213 converts the serial data into a parallel data byte and stores it in the Receiver Buffer Register (RBR). The Data Ready bit in the Line Status Register (LSR) is then set, and an appropriate interrupt identification code is written in the Interrupt Identification Register (IIR) to signal to the computer, the reception of a new data byte.
GND	14	Ground reference (0 V).
D0-D7	15-22	This is the 8 bit data bus comprising of three-state input/output lines. This bus provides bidirectional communication between the VL7C213 and the CPU. Data control words and status information are transferred via the D0 - D7 data bus.
INT	23	This output goes high whenever any one of the following interrupt types has an active condition and is enabled via the IER: Receiver Line Status flag, Received Data Available, Transmitter Holding Register Empty, and Modem Status. It is reset low upon the appropriate interrupt servicing. The INT pin is forced to a high impedance state when the OUT2 bit of the Modem Control Register (MCR) is low (power on state).
A0-A2	24-26	These three address inputs are used during read or write operation to select a UART register in the VL7C213 as shown in Table 1. The Divisor Latch Access Bit (DLAB) must be set high by the system software to access the bit rate divisor latches as shown in Table 2.
-CS	27	The VL7C213 is selected when this input is low. When high, the VL7C213 forces the Data bus lines into a high impedance state.
VCC	28	Positive supply (+5 V).

TABLE 1. VL7C213 UART REGISTERS

DLAB	A2	A1	A0	Mnemonic	Register
0	0	0	0	RBR	Receiver Buffer Register (read only)
0	0	0	0	THR	Transmitter Holding Register (write only)
0	0	0	1	IER	Interrupt Enable Register
X	0	1	0	IIR	Interrupt Identification Register (read only)
X	0	1	1	LCR	Line Control Register
X	1	0	0	MCR	Modem Control Register
X	1	0	1	LSR	Line Status Register
X	1	1	0	MSR	Modem Status (read only) Register
X	1	1	1	STR	Speed
1	0	0	0	DLL	Divisor Latch (LSB) (write only)
1	0	0	1	DLM	Divisor Latch (MSB) (write only)

X = "Don't Care" 0 = Logic Low 1 = Logic High

FIGURE 1. UART BLOCK DIAGRAM

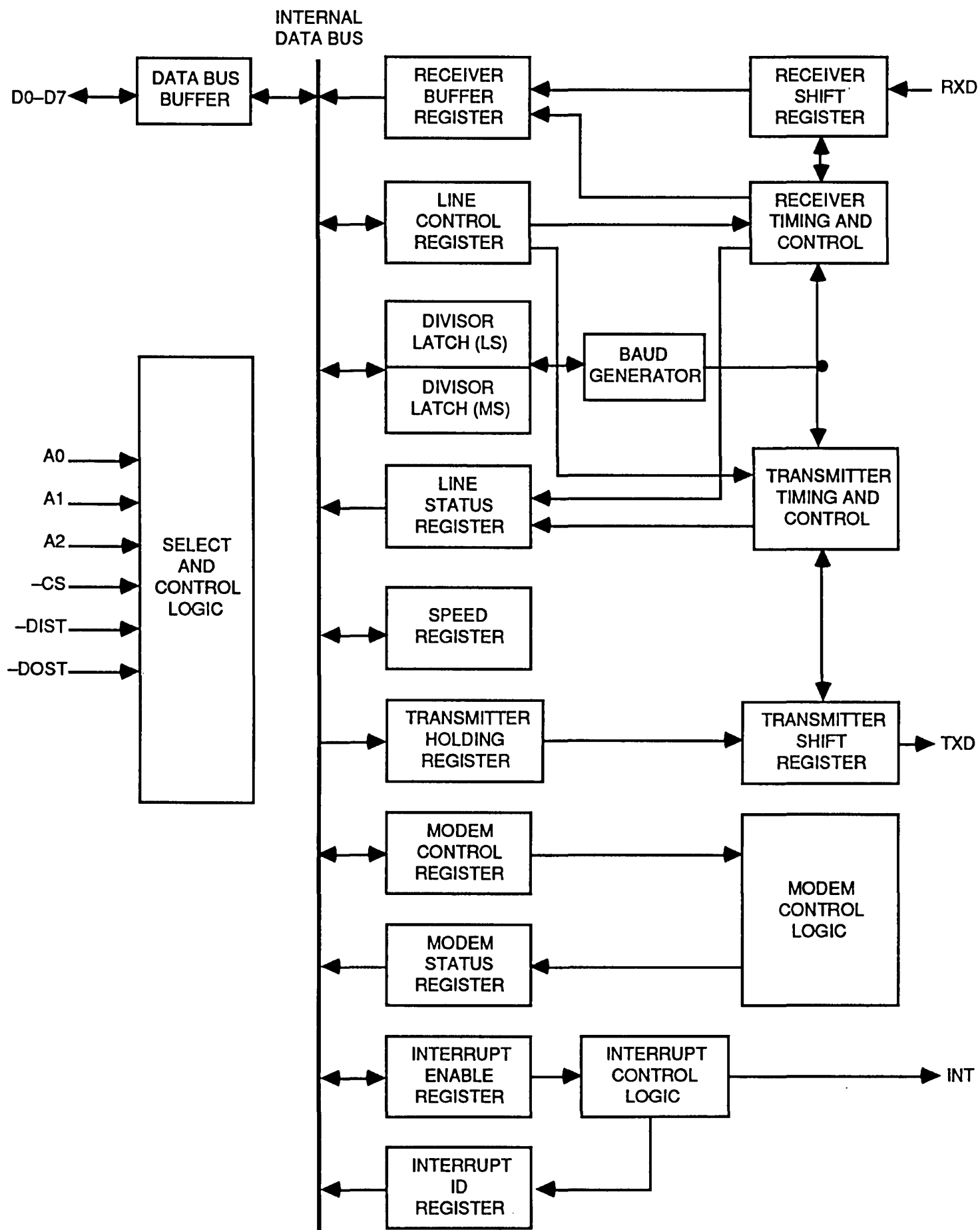


TABLE 2. VL7C213 UART REGISTER FUNCTION SUMMARY

Register Mnemonic	Register Bit Number							
	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
RBR	Data	Data	Data	Data	Data	Data	Data	Data
THR	Data	Data	Data	Data	Data	Data	Data	Data
IER	Receive Data Available Interrupt Enable	THRE Interrupt Enable	Receive Line Status Interrupt Enable	Modem Status Interrupt Enable	0	0	0	0
IIR	0 If Interrupt Pending	Interrupt ID Bit 0	Interrupt ID Bit 1	0	0	0	0	0
LCR	0 = 7 Bit Data 1 = 8 Bit Data	1	0 = 1 Stop Bit 1 = 2 Stop Bits	1 = Parity Enable	1 = Even Parity	1 = Stick Parity	1 = Set Break	DLAB
MCR	Data Terminal Ready	Request to Send	OUT1	OUT2 0 = INT Output to HI-Z	No Function	0	0	0
LSR	Data Ready	Overrun Error	Parity Error	Framing Error	Break Interrupt	THRE	TSRE	0
MSR	0	0	Trailing Edge Ring	Delta RLSD	1 (CTS)	1 (DSR)	RING	RLSD
DLM	Data	Data	Data	Data	Data	Data	Data	Data
DLL	Data	Data	Data	Data	Data	Data	Data	Data
STR	Data	Data	Data	Data	Data	Data	Data	Data

**TABLE 3. VL7C213 SOFTWARE REGISTERS**

Register	Range/Units	Description	Default
S0	0-255 Rings	Ring to answer telephone on	0
S1	0-255 Rings	Number of rings	0
S2	0-127 ASCII	Escape code character	43 (+)
S3	0-127 ASCII	Character recognized as carriage return	13 (CR)
S4	0-127 ASCII	Character recognized as line feedback	10 (LF)
S5	0-32, 127 ASCII	Character recognized as back space	8 (BS)
S6	2-255 sec.	Wait time for dial tone	2
S7	1-255 sec.	Wait time for carrier	30
S8	0-255 sec.	Pause time (caused by comma)	2
S9	1-255 1/10 sec.	Carrier detect response time	6
S10	1-255 1/10 sec.	Delay between loss of carrier and hang up	7
S11	50-255 millisec.	Duration and spacing of Touch-Tones	70
S12	20-255 1/50 sec.	Escape code guard time	50
S13	bit mapped	UART status register	-
S14	bit mapped	Option register	-
S15	bit mapped	Flag register	-
S16	0, 1, 2, 4	Test modes	0

TABLE 4. COMMAND SUMMARY
PREFIX, REPEAT AND ESCAPE COMMANDS

Command	Description (Notes 1 & 2)
AT	Attention prefix: precedes all command lines except + + + (escape) and A/(repeat) commands
A/	Repeat last command line (A/ is not followed by carriage return)
+ + +	Escape code: go from on-line state to command state (one second pause before and after escape code entry; ; + + + is not followed by carriage return)

DIALING COMMANDS

Command	Description (Notes 1 & 2)	Command	Description (Notes 1 & 2)
D	Dial	/	Wait for 1/8 second
P	Pulse*	@	Wait for silence
T	Touch-Tone	W	Wait for second dial tone
,	Pause	;	Return to command state after dialing
!	Flash	R	Reverse mode (to call originate-only modem)

OTHER COMMANDS

Commands	Description (Notes 1 & 2)	Commands	Description (Notes 1 & 2)
A	Answer call without waiting for ring	M1	Speaker on until carrier detected*
B/B0	CCITT V.22 mode (Note 3)	M2	Speaker always on
B1	Bell 103 and 212A mode*	O	Go to on-line state
C/C0	Transmit carrier off	O1	Remote digital loopback off*
C1	Carrier on*	O2	Remote digital loopback request
E/E0	Characters not echoed	Q/Q0	Result codes displayed*
E1	Characters echoed*	Q1	Result codes not displayed
F/F0	Half duplex	Sr?	Requests current value of register r
F1	Full duplex*	Sr = n	Sets register r to value of n
H/H0	On hook (hang up)	V/V0	Digit result codes
H1	Off hook; line and auxiliary relay	V1	Word result codes*
H2	Off hook; line relay only	X/X0	Compatible with Hayes-type 300 modems*
I/I0	Request product ID code (130)	X1	Result code CONNECT 1200 enabled
I1	Firmware revision number	X2	Enables dial tone detection
I2	Test internal memory	X3	Enables busy signal detection
L/L1	Low speaker volume	X4	Enables dial tone and busy signal detection
L2	Medium speaker volume	Y/Y0	Long space disconnect disabled*
L3	High speaker volume	Y1	Long space disconnect enabled
MM0	Speaker always off	Z	Software reset: restores all default settings

Notes:

1. Default modes are indicated by *
2. Commands entered with null parameters assume 0 - X is the same as X0.
3. When the ATB command is used in the answer mode, the VL7C212A is placed in either the V.21 or the V.22 mode, depending on the response from the remote modem. In the originate mode, the VL7C213 will sense if the baud rate is set at 300 or 1200 bits per second and will adjust the VL7C212A accordingly.

TABLE 5. RESULT CODES

Digit Code	Word Code	Description
0	OK	Command executed
1	Connect	Connected at 300 or 1200 bps Connected at 300 bps, if result of X1, X2, X3, or X4 command
2	Ring	Ringing signal detected (Note)
3	No Carrier	Carrier signal not detected or lost
4	Error	Illegal command Error in command line Command line exceeds buffer (40 characters, including punctuation) Invalid character format at 1200 bps
5	Connect 1200	Connected at 1200 bps. Results from X1, X2, X3, or X4 commands only
6	No Dialtone	Dialtone not detected and subsequent commands not processed Results from X2 or X4 commands only
7	Busy	Busy signal detected and subsequent commands not processed Results from X3 or X4 commands only
8	No Answer	Silence not detected and subsequent commands not processed Results from @ command only

Note: When the VL7C213 detects a ringing on the telephone line, it sends a RING result code. However, the VL7C213 will answer the call only if it is in auto-answer mode or is given an A command.

TABLE 6. RESET CONTROL OF REGISTERS AND PINOUT SIGNALS

Register/Signal	Reset Control	Reset State
Receiver Buffer Register	First word received	Data
Transmitter Holding Register	Writing into the Transmitter Holding Register	Data
Interrupt Enable Register	Power on reset	All bits low
Interrupt Identification Register	Power on reset	Bit 0 high; bits 1–7 low
Line Control Register	Writing into the LCR	Data
MODEM Control Register	Power on reset	All bits low
Line Status Register	Power on reset	Bits 0–4, 7 low; bits 5–6 high
Modem Status Register	Power on reset	Bits 0–3, 6–7 low; bits 4–5 high
Divisor Latch (high order bits)	Power on reset	1200 bps
TXD	Master reset	High
INT	Power on reset	Low (high impedance)

UART REGISTERS

Line Control Registers

This register controls the format of the asynchronous data communications.

Bit 0 and 1: Bit 1 is always high. Bit 0 specifies the number of bits in each transmitted or received serial character. The encoding of bit 0 is as follows:

Bit 1	Bit 0	Word Length
1	0	7 Bits
1	1	8 Bits

Bit 2: This bit specifies the number of Stop bits in each transmitted or received serial character. If bit 2 is a logic 0, one Stop bit is generated or checked in the transmit or receive data, respectively. If bit 2 is a logic 1, when 7-bit word length with no Parity is selected, two Stop bits are generated or checked.

Bit 3: This bit is the Parity Enable bit. When bit 0 is a logic 0 and bit 3 is a logic 1, a Parity bit is generated (transmit data) or checked (receive data) between the last data word bit and the Stop bit of the serial data. (The Parity bit is used to produce an even or odd number of 1s when the data word bits and the Parity bit are summed.)

Bit 4: This bit is the Even Parity Select bit. When bit 3 is a logic 1 and bit 4 is logic 0, and odd number of logic 1s is transmitted or checked in the data word bits and Parity bit. When bit 3 is logic 1 and bit 4 is a logic 1, an even number of bits is transmitted or checked.

Bit 5: This bit is the Stick Parity bit. When bit 3 is logic 1 and bit 5 is logic 1, the Parity bit is transmitted and then detected by the receiver in the opposite state indicated by bit 4.

Bit 6: This bit is the Set Break Control bit. When bit 6 is a logic 1, the serial output (TXD) is forced to the Spacing state (logic 0) and remains there (until reset by a low-level bit 6) regardless of other transmitter activity. The feature enables the CPU to alert a terminal in a computer communications system.

Bit 7: This bit is the Divisor Latch Access Bit (DLAB). It must be set high (logic 1) to access the Divisor Latches of the Baud Rate Generator during a Read or Write operation. It must be set low (logic 0) to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

Programmable Baud Rate Generator
The VL7C213's Baud Rate Generator can be programmed for one of six baud rates. The desired speed is selected by writing into the Divisor Latch (DLM). On reset, the rate will be 1200 baud.

DLM (Hex Code)	Baud Rate
00	1200
01	300
03	150
04	110
06	75
09	50

Line Status Register

This 8-bit register provides status information to the CPU concerning the data transfer. The contents of the Line Status Register are indicated in Table 2 and are described below:

Bit 0: This bit is the receiver Data Ready (DR) indicator. Bit 0 is set to a logic 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register. Bit 0 will reset to a logic 0 either by the CPU reading the data in the Receiver Buffer Register or by writing a logic 0 into it from the CPU.

Bit 1: This bit is the Overrun Error (OE) indicator. Bit 1 indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.

Bit 2: This bit is the Parity Error (PE) indicator. Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even parity select bit. The PE bit is set to a logic 1 upon detection of parity error and is reset to a logic 0 whenever the CPU reads the contents of the Line Status Register.

Bit 3: This bit is the Framing Error (FE) indicator. Bit 3 indicates that the received character did not have a valid Stop bit. Bit 3 is set to a logic 1 whenever the Stop bit following the last data bit or parity bit is detected as a zero (Spacing level).

Bit 4: This bit is the Break Interrupt (BI) indicator. Bit 4 is set to a logic 1

whenever the received data input is held in the Spacing (Logic 0) state for longer than a full word transmission time - the total time of Start bit + data bits + Parity + Stop bits.

Bit 5: This bit is the Transmitter Holding Register Empty (THRE) indicator. Bit 5 indicates that the VL7C213 is ready to accept a new character for transmission. In addition, this bit causes the VL7C213 to issue an interrupt to the CPU when the Transmit Holding Register Empty enable is set high. The THRE bit is set to a logic 0 concurrently with the loading of the Transmitter Holding Register by the CPU.

Bit 6: This bit is the Transmitter Shift Register Empty (TSRE) indicator. Bit 6 is set to a logic 1 whenever the Transmitter Shift Register is idle. It is reset to logic 0 upon a data transfer from the Transmitter Holding Register to the Transmitter Shift Register.

Bit 7: This bit is permanently set to logic 0.

Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected.

Interrupt Identification Register

The VL7C213 has an on-chip interrupt capability that allows for complete flexibility in interfacing to all popular microprocessors. To provide minimum software overhead during data character transfers, the VL7C213 prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows: Receiver Line Status (priority 1); Received Data Ready (priority 2); Transmitter Holding Register Empty (priority 3); and MODEM Status (priority 4).

Information indicating that a prioritized interrupt is pending the source of that interrupt are stored in the Interrupt Identification Register (refer to Table 7). The Interrupt Identification Register (IIR), when addressed during chip-select time, freezes the highest priority interrupt pending and no other interrupts are acknowledged until the particular interrupt is serviced by the CPU. The contents of the IIR are indicated in Table 2 and are described below.

Bit 0: This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When bit 0 is a logic 1, no interrupt is pending.

Bits 1 and 2: These two bits of the IIR are used to identify the highest priority interrupt pending as indicated in Table 7.

Bits 3 through 7: These five bits of the IIR are always logic 0.

Interrupt Enable Register

This 8-bit register enables the four interrupt sources of the VL7C213 to separately activate the Interrupt (INT) output signal. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the Interrupt Enable Register. Similarly, by setting the appropriate bits of this register and the active (high) INT output from the chip. All other system functions operate in their normal manner, including the setting of the Line Status and MODEM Status Register. The contents of the Interrupt Enable Register are indicated in Table 2 and are described below.

Bit 0: This bit enables the Received Data Available Interrupt when set to logic 1.

Bit 1: This bit enables the transmitter Holding Register Empty Interrupt when set to a logic 1.

Bit 2: This bit enables the Receiver Line Status Interrupt when set to logic 1.

Bit 3: This bit enables the MODEM Status Interrupt when set to logic 1.

Bit 4 through 7: These four bits are always logic 0.

MODEM Control Register

This 8-bit register controls the interface with the MODEM. The contents of the MODEM Control Register are indicated in Table 2 and are described below.

Bit 0: This bit controls Data Terminal Ready (DTR) signal. If the external switch on the -RD pin is set to VCC through an 18 k Ω resistor, setting the DTR low will force the VL7C213 into the command state and if on line, it will hang up.

Bit 1: This bit controls the Request to Send (RTS) signal. This signal is not used by the VL7C213.

Bit 2: This bit controls the Output 1 (OUT1) signal. This signal is not used by the VL7C213.

Bit 3: This bit controls the Output 2 (OUT2) signal. When OUT2 is a 0, the interrupt output is in high impedance state.

Bit 4: Not used.

Bits 5 through 7: These bits are permanently set to logic 0.

MODEM Status Register

This 8-bit register provides the current state of the control lines from the

MODEM (or peripheral device) to the CPU. In addition to this current-state information, two bits of the MODEM Status Register provide change information. These bits are set to a logic 1 whenever a control input from the MODEM changes state. They are reset to logic 0 whenever the CPU reads the MODEM Status Register.

The contents of the MODEM Status Register are indicated in Table 2 and are described below.

Bits 0 and 1: These bits are always 0.

Bit 2: This bit is the Trailing Edge of Ring Indicator (TERI) detector. Bit 2 indicates that the -RI input to the chip has changed from On (logic 1) to an Off (logic 0) condition.

Bit 3: This bit is the Delta Received Line Signal Detector (DRLSD) indicator. Bit 3 indicates that the carrier detector has changed state.

Bit 4: This bit is always 1.

Bit 5: This bit is always 1.

Bit 6: This bit is the complement of the Ring Indicator (-RI) input.

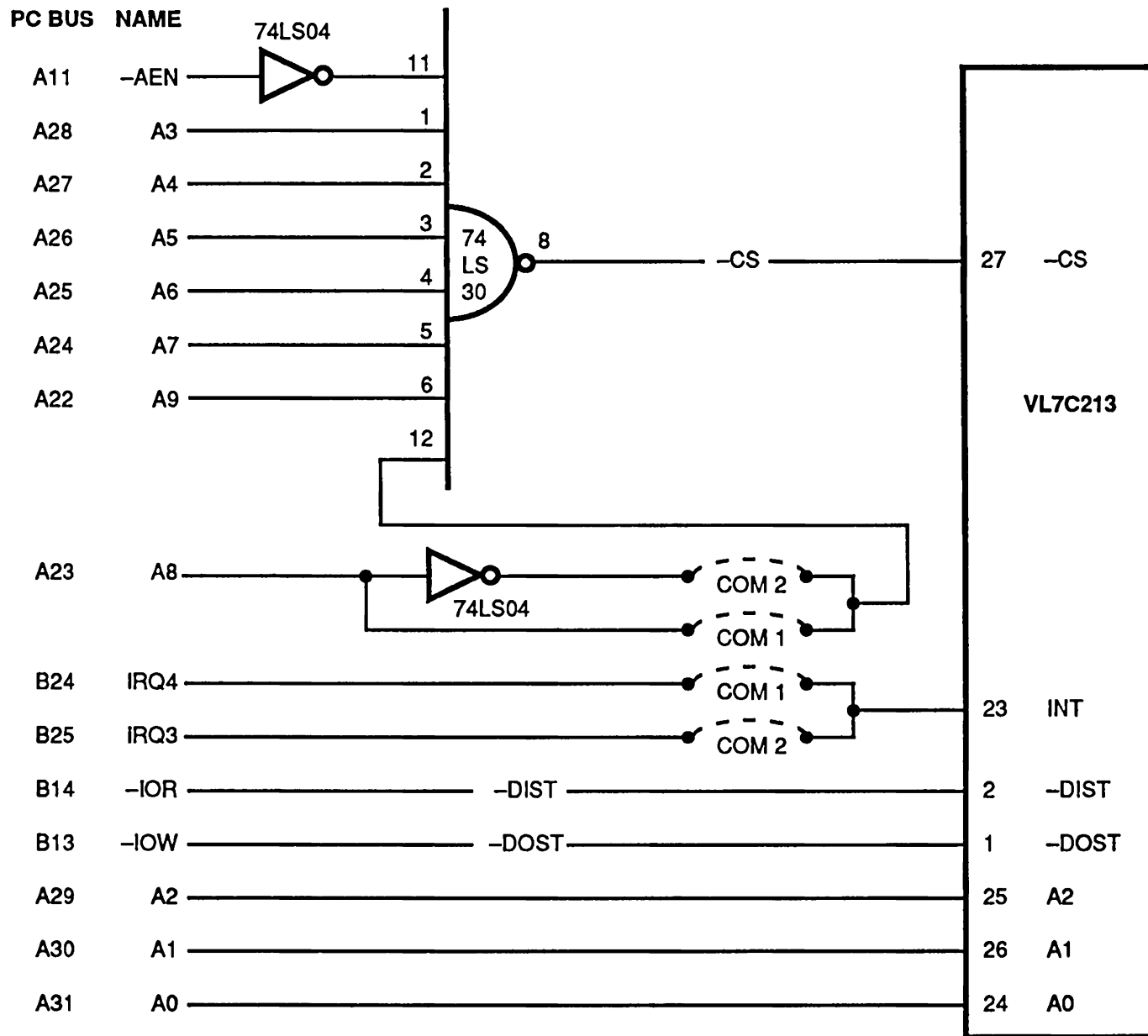
Bit 7: This bit is the Received Line Signal Detect (RLSD) signal.

Whenever bit 2 is set to logic 1, or bit 3 changes state, a MODEM Status Interrupt is generated if enabled.

TABLE 7. INTERRUPT CONTROL FUNCTIONS

Interrupt Identification Register			Interrupt Set and Reset Functions			
Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Flag	Interrupt Source	Interrupt Reset Control
0	0	1		None	None	
1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error or Framing Error or Break Interrupt	Reading the Line Status Register
1	0	0	Second	Received Data Available	Received Data Available	Reading the Receiver Buffer Register
0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR (if source of interrupt) or Writing into the Transmitter Holding Register
0	0	0	Fourth	MODEM Status	Ring Indicator or Received Line Signal Detect	Reading the MODEM Status Register

FIGURE 2. ADDRESS DECODER CIRCUIT



AC CHARACTERISTICS: TA = 0 TO 70°C, VCC = 5 V ±10%

Symbol	Parameter	Min	Max	Units	Conditions
tDIW	–DIST Strobe Width	300		ns	1TTL Load
tRC	Read Cycle Delay	300		ns	1TTL Load
RC	Read Cycle = tDIW + tRC + 20 ns	620		ns	1TTL Load
tDDD	Delay from –DIST to Data		300	ns	1TTL Load
tHZ	–DIST to Floating Data Delay	60		ns	1TTL Load
tDOW	–DOST Strobe Width	300		ns	1TTL Load
tWC	Write Cycle Delay	300		ns	1TTL Load
WC	Write Cycle = tDOW + tWC + 20 ns	620		ns	1TTL Load
tDS	Data Setup Time	60		ns	1TTL Load
tDH	Data Hold Time	60		ns	1TTL Load
tDIC	–DIST Delay from Select	150		ns	1TTL Load
tDOC	–DOST Delay from Select	150		ns	1TTL Load
tACR	Address and Chip Select Hold Time from –DIST	10		ns	1TTL Load
tACW	Address and Chip Select Hold Time from –DOST	10		ns	1TTL Load

Receiver

tRINT	Delay from –DIST (Read RBR) to Reset Interrupt		1	μs	100 pF Load
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Transmitter

tHR	Delay from –DOST (Write THR) to Reset Interrupt		1	μs	100 pF Load
tIRS	Delay from Initial INTR Reset to Transmit Start		1	Baud Cycle	
tSI	Delay from Initial Write to Interrupt		1	Baud Cycle	
tSS	Delay from Stop to Next Start		1	μs	
tSTI	Delay from Stop to Interrupt (THRE)		1	Baud Cycle	
tIR	Delay from –DIST (Read IIR) to Reset Interrupt (THRE)		1	μs	100 pF Load

Note: A TTL load is 40 μA sourced and -1.6 mA sinked current.

FIGURE 3. READ CYCLE TIMING

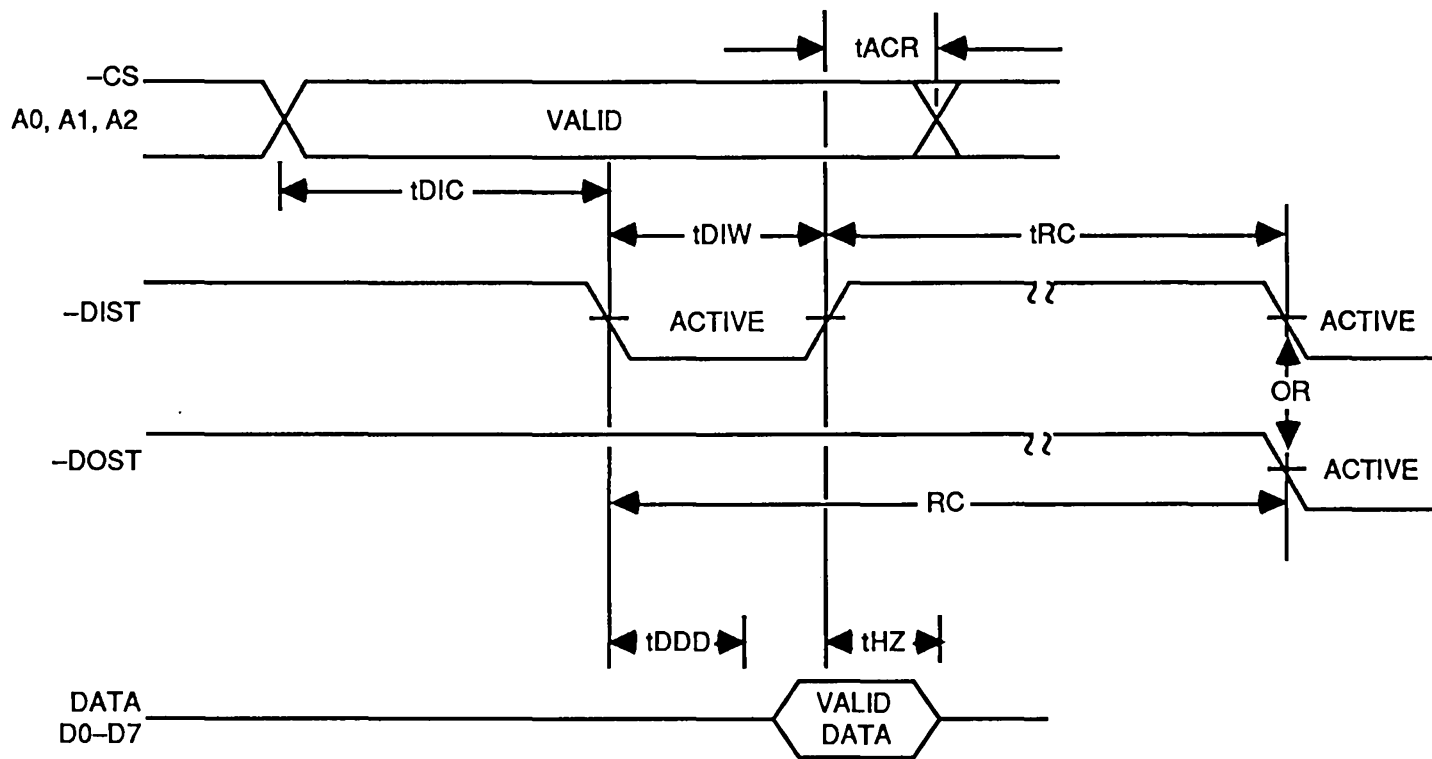


FIGURE 4. WRITE CYCLE TIMING

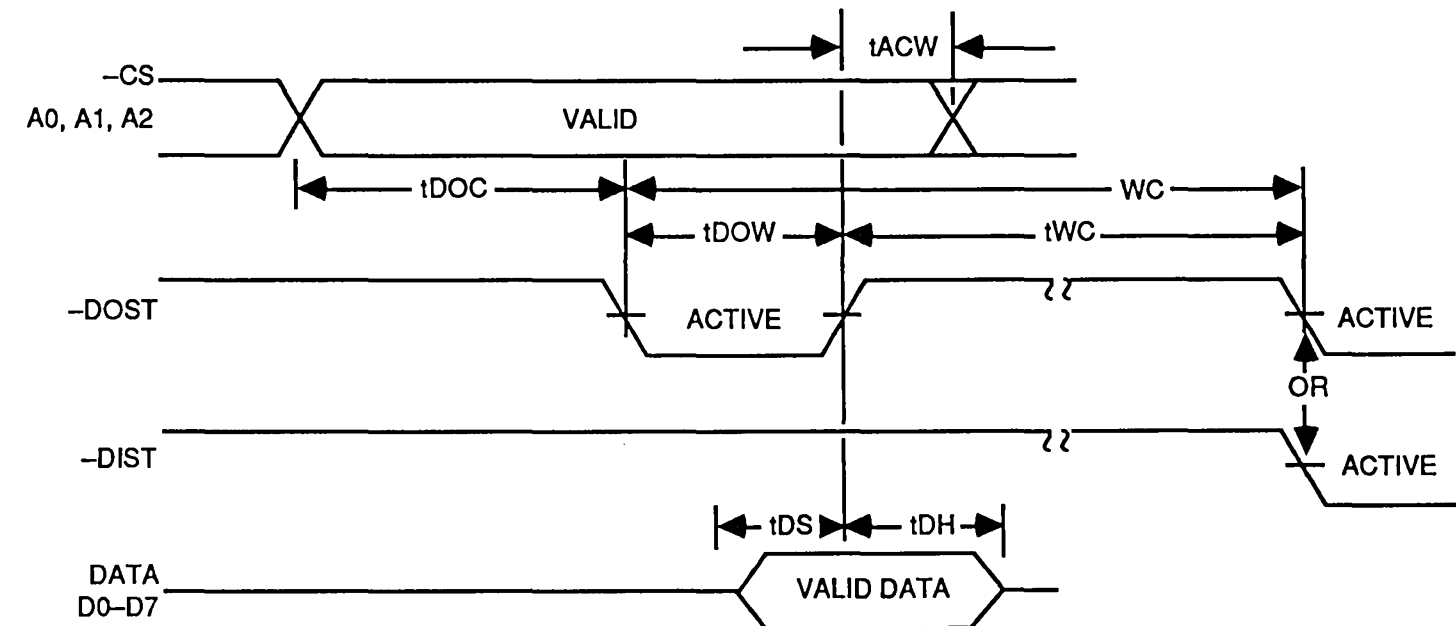




FIGURE 5. RECEIVER TIMING

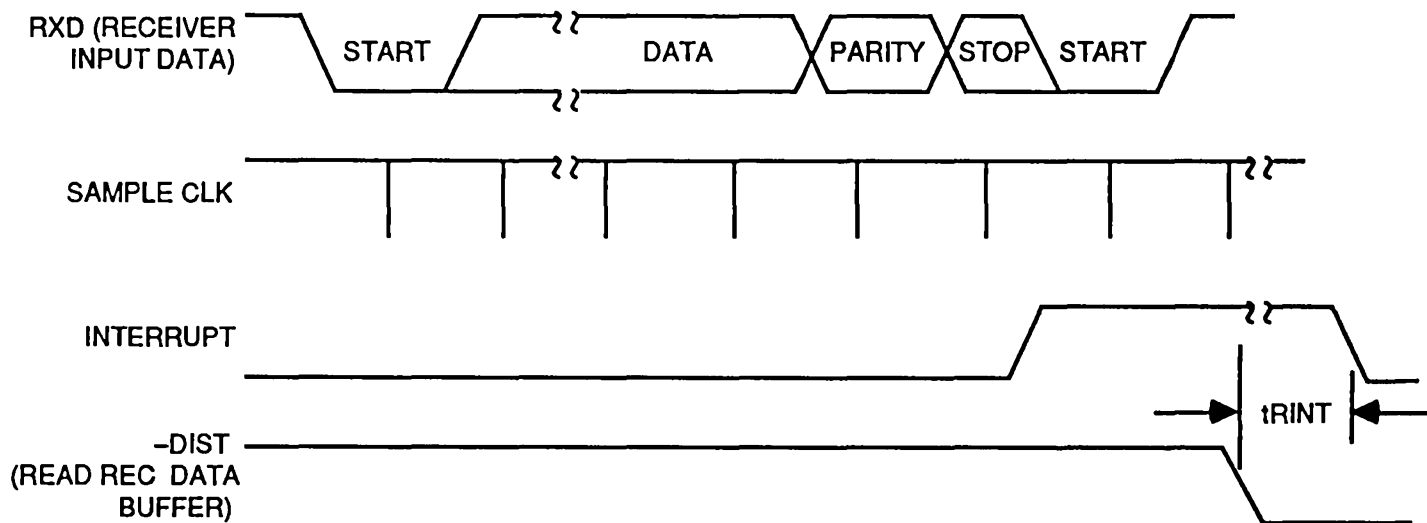
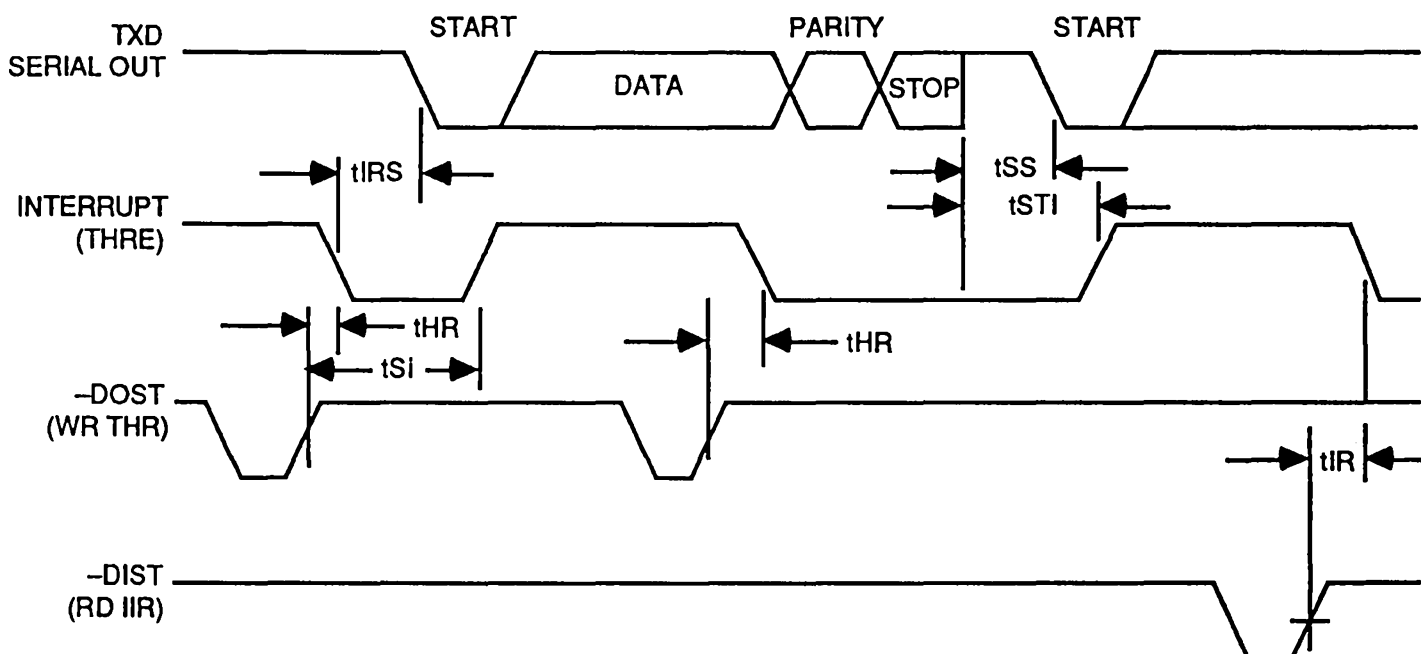


FIGURE 6. TRANSMITTER TIMING



ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	0°C to +70°C
Storage Temperature	-65°C to +150°C
Supply Voltage to Ground Potential	+6 V
Applied Input Voltage	-0.6 V to VCC +0.6 V
Power Dissipation	500 mW

Stresses above those listed may cause permanent damage to the device. These are stress ratings only, functional operation of this device at these or any other conditions above those indicated

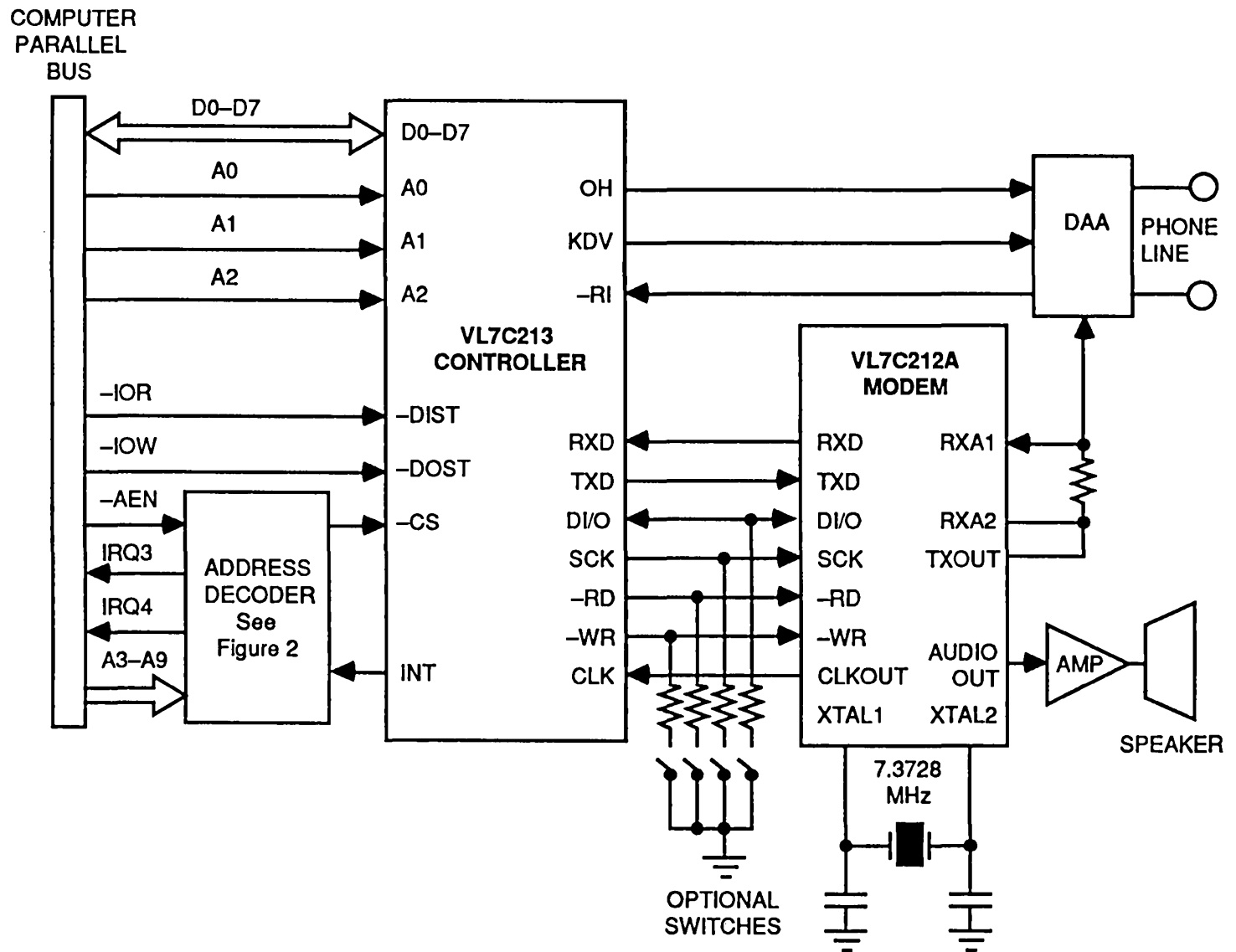
in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS: TA = 0 to +70 °C, VCC = 5 V ±10%

Symbol	Parameter	Min	Typ	Max	Units	Conditions
VCC	Positive Supply Voltage	4.5	5.0	5.5	V	
ICC	Operating Current		10.0		mA	@ VCC = 5 V
VIH	High Level Input Voltage	2.0			V	All pins except -RI
VIL	Low Level Input Voltage			0.8	V	All pins except -RI
VT+	Positive Hysteresis Threshold		2.5		V	-RI pin
VT-	Negative Hysteresis Threshold		1.8		V	-RI pin
VOH	High Level Output Voltage	VCC - 1.0			V	Digital signal pins D0 to D7 and INT @ IOH = -6 mA
		VCC - 1.0			V	All other output or I/O pins @ IOH = -2 mA
VOL	Low Level Output Voltage			0.4	V	Digital signal pins D0 to D7 and INT @ IOL = 6 mA
				0.4	V	All other output or I/O pins @ IOL = 2 mA
IL	Leakage Current (Note)		±1.0		µA	
FCLK	Clock Frequency	7.3721	7.3728	7.3735	MHz	

Note : This applies to all pins except TEST, which has an internal pull-down -WR, -RD, SCK, DI/O and switch input pins which have internal pull-ups.

FIGURE 7. INTEGRAL SMART MODEM CONFIGURATION FOR PC BUS APPLICATIONS



STAND-ALONE MODEM INTERFACE CONTROLLER

FEATURES

- Direct interface to VL7C212A single chip modems
- Complete Hayes AT command set in firmware
- Built-in UART for RS232C interface
- Two-micron CMOS process
- 28-pin DIP or PLCC package
- Complete intelligent modem in two ICs
- Compatible with industry-standard software
- Reduces board space and component count requirements
- Low power consumption
- Replacement for Sierra SC11008

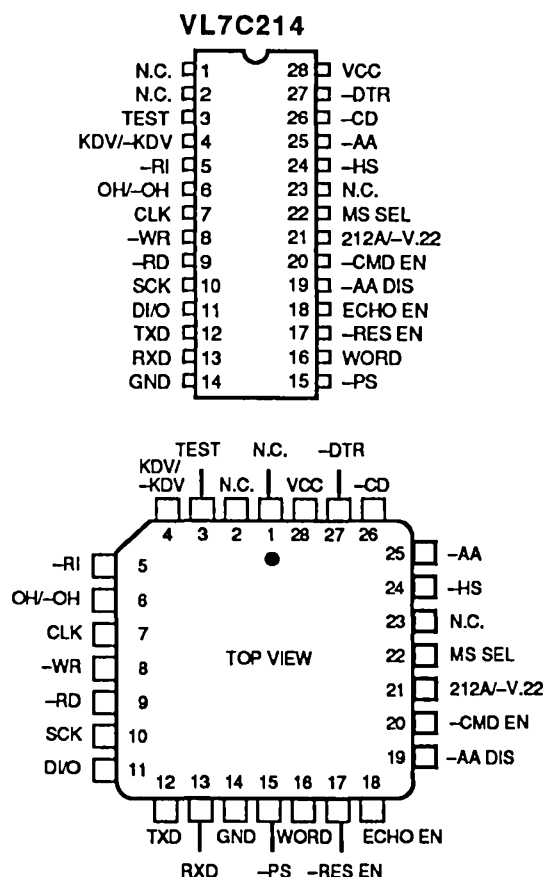
DESCRIPTION

The VL7C214 Stand-Alone Modem Interface Controller is specifically designed to control the VL7C21A single-chip, 300/1200 bit-per-second modem. Built with an advanced two-micron CMOS process, the VL7C214 provides a highly cost effective solution for interfacing a modem IC to a computer's RS232C port. When connected to the VL7C21A, with the addition of a data access arrangement (DAA), the VL7C214 implements a Hayes-type smart modem for stand-alone modem applications. All of the popular communications software written for the IBM PC will work with the VL7C214/VL7C21A chip set. The

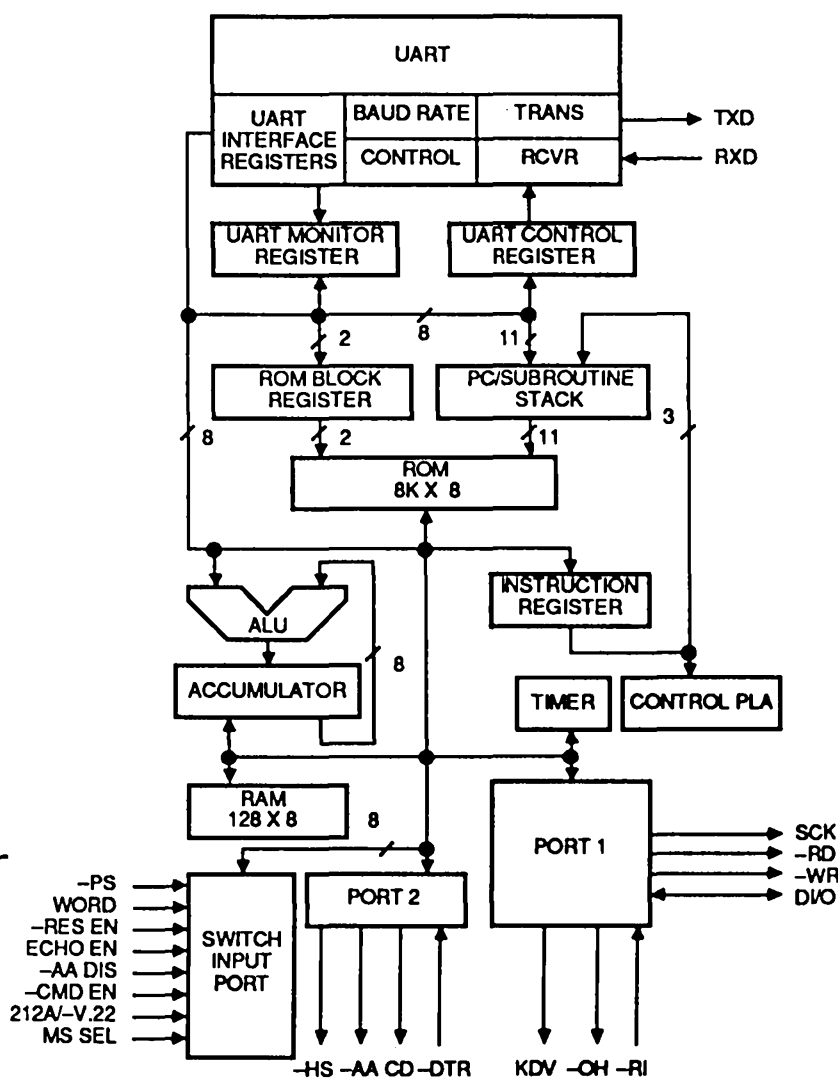
VL7C214 contains an 8-bit microprocessor, 8K by 8 bits of ROM and 128 by 8 bits of RAM. In order to support the stand-alone functionality of the device, an 8-bit switch input port allows immediate user access and manual control of the system. Either Bell 103 or CCITT V.22 may be selected in this manner.

For specific high volume applications, the control program can be modified by VLSI Technology, Inc. to include additional commands and functions.

PIN DIAGRAMS



BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Package
VL7C214-PC	Plastic DIP
VL7C214-QC	Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range is 0°C to +70°C.

SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Description
N.C.	1	No connection
N.C.	2	No connection
TEST	3	When the test input is high, the VL7C214 enters a test mode (used for factory testing only). For normal operation, this pin can be left open or connected to ground.
KDV/-KDV	4	This output controls the operation of the data/voice relay. The polarity of this output is selected by -PS pin. If -PS is connected to ground, this output is active high, i.e., it is low when modem is on hook, causing the data/voice relay to be off and the phone line is connected to the phone set. During a data call, this output goes high to operate the data/voice relay, disconnecting the phone set from the phone line. It may also be used to drive a relay for multi-line phone applications to close the A and A1 leads. If -PS pin is left open or connected to VCC, this output is active low, i.e., it is high when the modem is on hook and low when modem makes a data call.
-RI	5	The output of the ring detector in the DAA is connected to this input. A low level on this input indicates the "On" duration of the ring cycle. This is a Schmitt-trigger input, allowing for slow rising and falling signals on this pin.
OH/-OH	6	This output controls the operation of the hookswitch relay in the DAA. The polarity of this output is selected by -PS pin. If -PS pin is connected to ground, this output is active high, i.e., it is low when the modem is on hook. During a data call, it goes high to operate the hookswitch relay and seize the phone line. During rotary dialing, the VL7C214 pulses this output at a rate of 10 pulses per second with appropriate Mark/Space ratio depending on 212A or V.22 mode. If -PS pin is left open or connected to VCC, this output is active low, i.e., it is high when the modem is on hook and low during data call.
CLK	7	A 7.3728 MHz clock signal must be connected to this input. Normally, the CKOUT pin of the VL7C212A modem is connected to this pin. All internal timing is derived from this clock.
-WR	8	This pin is used to initiate writing of data to the VL7C212A modem.
-RD	9	This pin is used to initiate reading of data from the VL7C212A modem.
SCK	10	The VL7C214 supplies a shift clock on this pin to the VL7C212A modem for reading or writing data.
DI/O	11	The VL7C214 shifts data serially out of this pin to VL7C212A during a write operation and shifts data serially into this pin during a read operation from the VL7C212A.
TXD	12	The VL7C214 outputs serial data in asynchronous start/stop format at the data rate selected by the terminal. This data is either echo of commands received from the terminal or result codes generated by the controller during processing of the commands. This output is normally high and should be "AND"ed with the RXD output of the VL7C212A to form RXD data to the terminal.
RXD	13	The VL7C214 receives command data from the terminal on this pin. The UART in the controller connects the serial asynchronous start/stop data into a parallel byte for processing by the controller.
GND	14	Ground reference (0 V).
-PS	15	This input controls the polarity of KDV and OH outputs. When left open or connected to VCC, it forces the KDV and OH outputs to be active low. If this input is connected to ground, KDV and OH outputs are active high.
WORD	16	When the input is open or connected to VCC, the VL7C214 sends result codes as words. When this input is low, result codes are sent as digits. This setting can also be changed by entering the V command.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Description
-RES EN	17	When this input is low, the VL7C214 sends result codes. When this input is high or left open, commands received from the terminal are performed but result codes are not sent. This setting can also be changed by entering the Q command.
ECHO EN	18	When this input is high or left open, the VL7C214 echoes characters received from the terminal in the command state. When this input is low, the VL7C214 will not echo characters unless it is set for half duplex and it is on line. This setting can also be changed by entering the E command.
-AA DIS	19	When this input is low, the VL7C214 will not answer incoming calls. When this input is high or left open, the VL7C214 automatically answers incoming calls on the first ring. This function can also be enabled/disabled by writing to the S0 register.
-CMD EN	20	When this input is low, the VL7C214 recognizes command sent to it. For some applications such as unattended answering operation it is better to disable this function by leaving this input open or connecting it to VCC.
212A-V.22	21	When this input is open or connected to VCC, the VL7C214 supports Bell 103 and 212A modes. When this input is low, the VL7C214 supports the CCITT V.22 and V.21 modes. This setting can also be changed by entering the B command.
MS SEL	22	When this input is open or connected to VCC, the Mark/Space ratio is U.S. standard, 40/60 Make/Break. When it is low, the Mark/Space ratio is European standard, 33/67 Make/Break.
N.C.	23	No connection
-HS	24	This output, when low, indicates that the modem is in the high speed (1200 bps) mode. When high, it indicates that it is in the low speed (300 bps) mode. This output can be directly connected to a light emitting diode through a 330 Ω resistor.
-AA	25	This output is low when the VL7C214 is set for auto-answer mode, either by switch input -AA DIS (pin 19) or register S0. The output goes high during each ring. If the device is not set to answer the phone (pin 19 is low or S0 = 0), this output goes low each time the phone rings. A light emitting diode through a 330 Ω resistor can be directly connected to this output.
-CD	26	This output goes low when the VL7C214 detects a carrier signal from the remote modem. If the connection is broken or never established, it remains high. A light emitting diode can be directly connected to this output through a 330 Ω resistor.
-DTR	27	When this input is low, the VL7C214 executes data call commands. If during a data call, this input goes high, the VL7C214 terminates the data call, hangs up the phone line and returns to command state.
VCC	28	Positive supply (+5 V).

**TABLE 1. VL7C214 SOFTWARE REGISTERS**

Register	Range/Units	Description	Default
S0	0-255 Rings	Ring to answer telephone on	0
S1	0-255 Rings	Number of rings	0
S2	0-127 ASCII	Escape code character	43 (+)
S3	0-127 ASCII	Character recognized as carriage return	13 (CR)
S4	0-127 ASCII	Character recognized as line feedback	10 (LF)
S5	0-32, 127 ASCII	Character recognized as back space	8 (BS)
S6	2-255 sec.	Wait time for dial tone	2
S7	1-255 sec.	Wait time for carrier	30
S8	0-255 sec.	Pause time (caused by comma)	2
S9	1-255 1/10 sec.	Carrier detect response time	6
S10	1-255 1/10 sec.	Delay between loss of carrier and hang up	7
S11	50-255 millisec.	Duration and spacing of Touch-Tones	70
S12	20-255 1/50 sec.	Escape code guard time	50
S13	bit mapped	UART status register	-
S14	bit mapped	Option register	-
S15	bit mapped	Flag register	-
S16	0, 1, 2, 4	Test modes	0

TABLE 2. COMMAND SUMMARY
PREFIX, REPEAT AND ESCAPE COMMANDS

Command	Description (Notes 1 & 2)
AT	Attention prefix: precedes all command lines except + + + (escape) and A/(repeat) commands
A/	Repeat last command line (A/ is not followed by carriage return)
+ + +	Escape code: go from on-line state to command state (one second pause before and after escape code entry; ; + + + is not followed by carriage return)

DIALING COMMANDS

Command	Description (Notes 1 & 2)	Command	Description (Notes 1 & 2)
D	Dial	/	Wait for 1/8 second
P	Pulse*	@	Wait for silence
T	Touch-Tone	W	Wait for second dial tone
,	Pause	;	Return to command state after dialing
I	Flash	R	Reverse mode (to call originate-only modem)

OTHER COMMANDS

Commands	Description (Notes 1 & 2)	Commands	Description (Notes 1 & 2)
A	Answer call without waiting for ring	M1	Speaker on until carrier detected*
B/B0	CCITT V.22 mode (Note 3)	M2	Speaker always on
B1	Bell 103 and 212A mode*	O	Go to on-line state
C/C0	Transmit carrier off	O1	Remote digital loopback off*
C1	Carrier on*	O2	Remote digital loopback request
E/E0	Characters not echoed	Q/Q0	Result codes displayed*
E1	Characters echoed*	Q1	Result codes not displayed
F/F0	Half duplex	Sr?	Requests current value of register r
F1	Full duplex*	Sr = n	Sets register r to value of n
H/H0	On hook (hang up)	V/V0	Digit result codes
H1	Off hook; line and auxiliary relay	V1	Word result codes*
H2	Off hook; line relay only	X/X0	Compatible with Hayes-type 300 modems*
I/I0	Request product ID code (130)	X1	Result code CONNECT 1200 enabled
I1	Firmware revision number	X2	Enables dial tone detection
I2	Test internal memory	X3	Enables busy signal detection
L/L1	Low speaker volume	X4	Enables dial tone and busy signal detection
L2	Medium speaker volume	Y/Y0	Long space disconnect disabled*
L3	High speaker volume	Y1	Long space disconnect enabled
M/M0	Speaker always off	Z	Software reset: restores all default settings

Notes:

1. Default modes are indicated by *.
2. Commands entered with null parameters assume 0 - X is the same as X0.
3. When the ATB command is used in the answer mode, the VL7C212A is placed in either the V.21 or the V.22 mode, depending on the response from the remote modem. In the originate mode, the VL7C214 will sense if the baud rate is set at 300 or 1200 bits per second and will adjust the VL7C212A accordingly.

TABLE 3. RESULT CODES

Digit Code	Word Code	Description
0	OK	Command executed
1	Connect	Connected at 300 or 1200 bps Connected at 300 bps, if result of X1, X2, X3, or X4 command
2	Ring	Ringing signal detected (Note)
3	No Carrier	Carrier signal not detected or lost
4	Error	Illegal command Error in command line Command line exceeds buffer (40 characters, including punctuation) Invalid character format at 1200 bps
5	Connect 1200	Connected at 1200 bps. Results from X1, X2, X3, or X4 commands only
6	No Dialtone	Dialtone not detected and subsequent commands not processed Results from X2 or X4 commands only
7	Busy	Busy signal detected and subsequent commands not processed Results from X3 or X4 commands only
8	No Answer	Silence not detected and subsequent commands not processed Results from @ command only

Note : When the VL7C214 detects a ringing on the telephone line, it sends a RING result code. However, the VL7C214 will answer the call only if it is in auto-answer mode or is given an A command.

ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature 0°C to +70°C
 Storage Temperature -65°C to +150°C
 Supply Voltage to Ground Potential +6 V
 Applied Input Voltage -0.6 V to VCC + 6 V
 Power Dissipation 500 mW

Stresses above those listed may cause permanent damage to the device. These are stress ratings only, functional operation of this device at these or any other conditions above those indicated

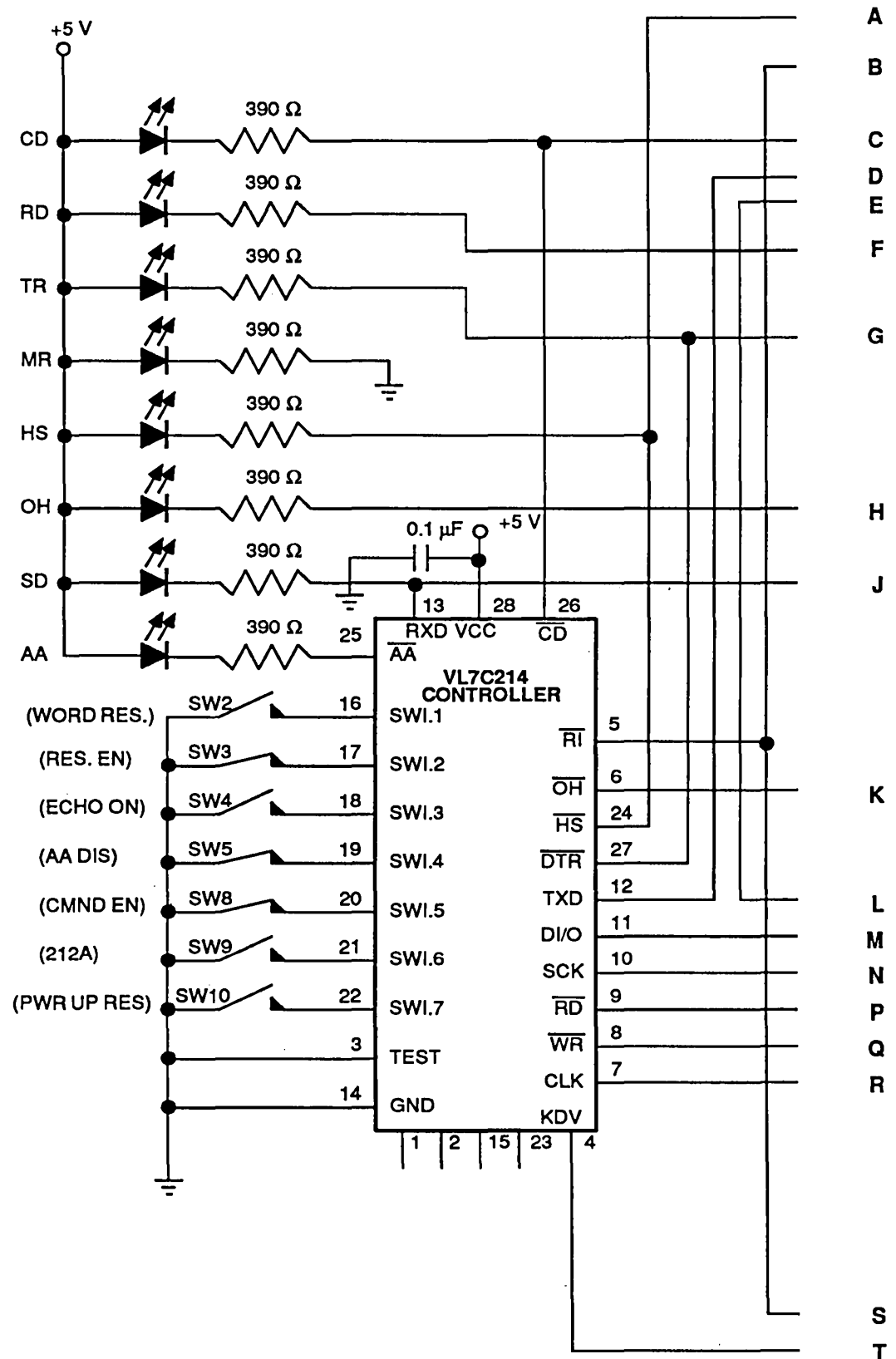
in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS: TA = 0 to +70 °C, VCC = 5 V ±10%

Symbol	Parameter	Min	Typ	Max	Units	Conditions
VCC	Positive Supply Voltage	4.5	5.0	5.5	V	
ICC	Operating Current		10.0		mA	@ VCC = 5 V, outputs unloaded
VIH	High Level Input Voltage	2.0			V	All pins except -RI
VIL	Low Level Input Voltage			0.8	V	All pins except -RI
VT+	Positive Hysteresis Threshold		2.5		V	-RI pin
VT-	Negative Hysteresis Threshold		1.8		V	-RI pin
VOH	High Level Output Voltage	VCC - 1.0			V	@ IOH = -2 mA
VOL	Low Level Output Voltage			0.4	V	@ IOL = 2 mA
IL	Leakage Current (Note)		±1.0		µA	
FCLK	Clock Frequency	7.3721	7.3728	7.3735	MHz	

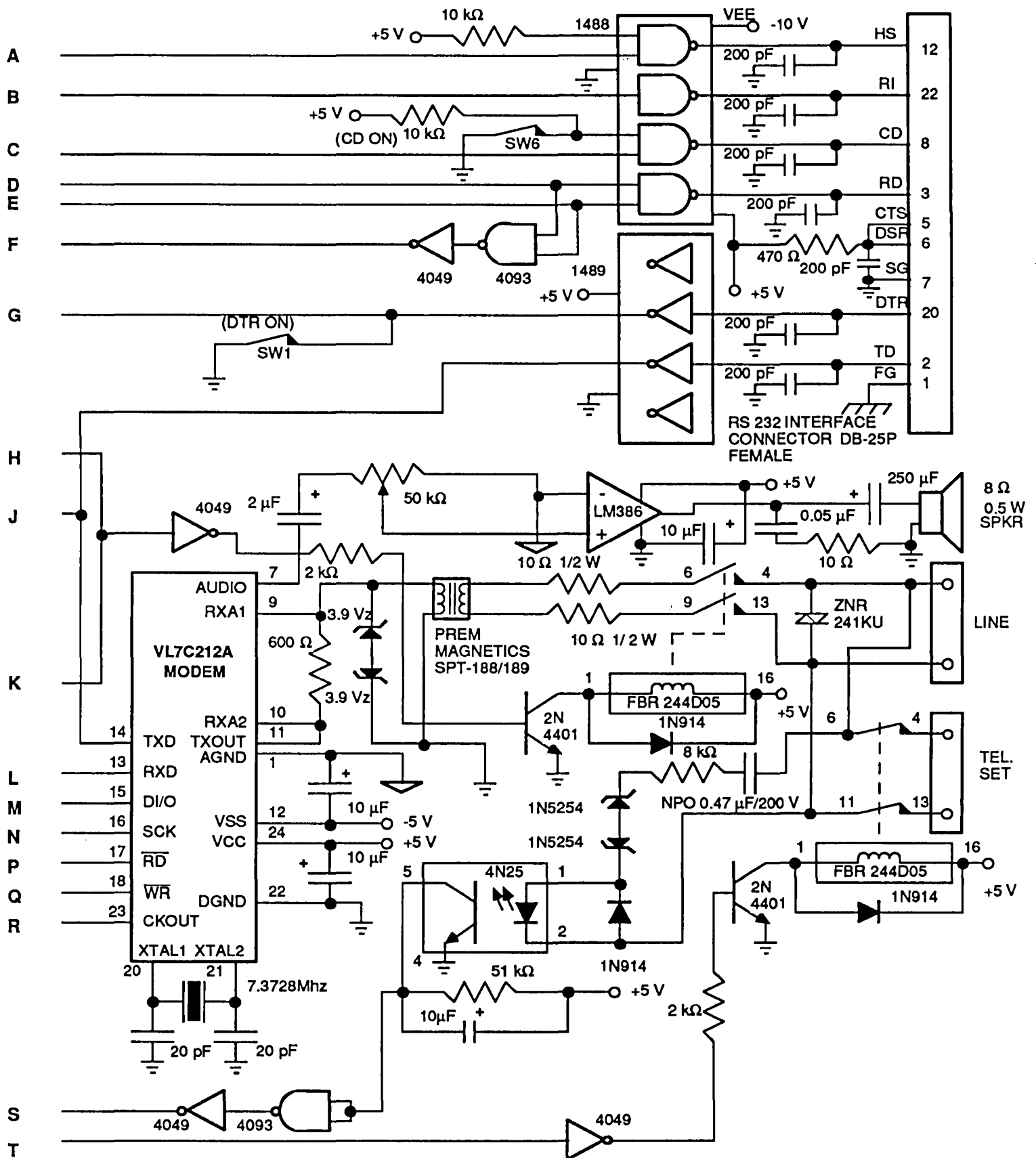
Note : This applies to all pins except TEST, which has an internal pull-down -WR, -RD, SCK, D/O, and switch input pins 15 thru 21 which have internal pull-ups.

FIGURE 1. 212A/V.22 STAND-ALONE INTELLIGENT MODEM USING THE VL7C212A MODEM IC AND THE VL7C214



Note: Schematics are for illustration purposes only. Operational systems may require modifications.

FIGURE 1. 212A/V.22 STAND-ALONE INTELLIGENT MODEM USING THE VL7C212A MODEM IC AND THE VL7C214 (Cont.)



HIGH SPEED PARALLEL BUS MODEM CONTROLLER

FEATURES

- Direct interface to VL7C212A single-chip modems
- Complete Hayes AT command set in firmware
- Built-in UART
- Direct IBM PC bus interface
- IORDY pin for use on high-speed buses
- Two-micron CMOS process
- Complete intelligent modem in two ICs
- Compatible with industry-standard software
- Replacement for Sierra SC11017
- Reduces board space and component count requirements

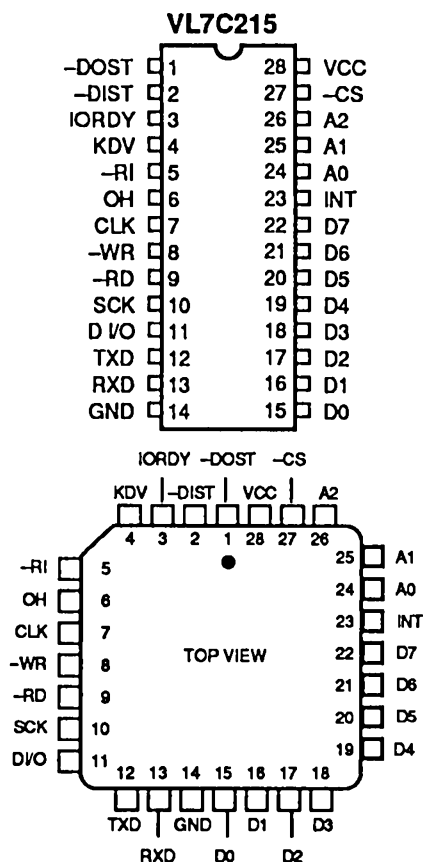
DESCRIPTION

The VL7C215 Parallel Bus Modem Controller is specifically designed to control the VL7C212A single-chip, 300/1200 bit-per-second modem. Built with an advanced two-micron CMOS process, the VL7C215 provides a highly cost effective solution for interfacing a modem IC to a system bus. When connected to the VL7C212A, with the addition of a data access arrangement (DAA), the VL7C215 implements a Hayes-type smart modem for board-level, integral-modem applications. Because the VL7C215 fully emulates the functionality of the VL82C50 UART and includes data bus transceivers, it can be directly interfaced to a computer's parallel data

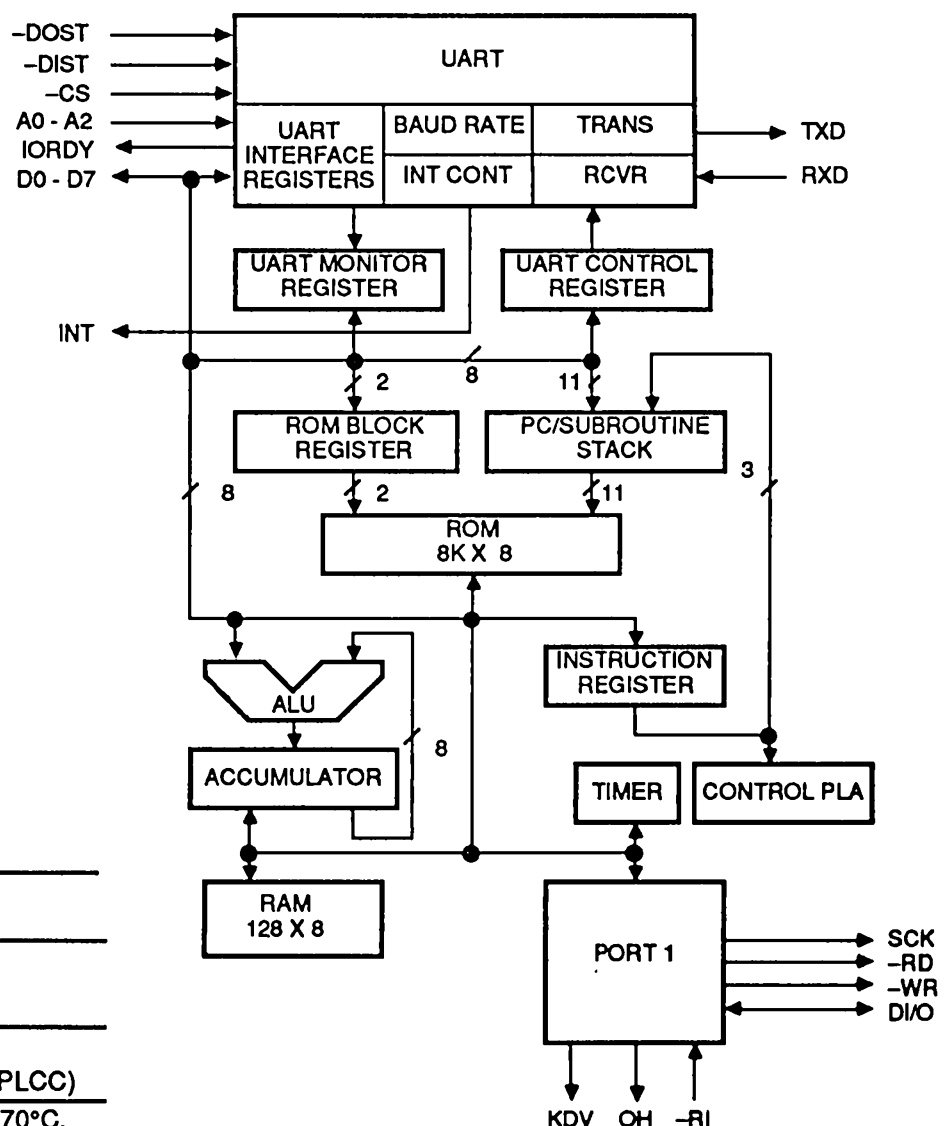
bus (in particular to the bus of the IBM PC, XT or AT). All of the popular communications software written for the PC will work with the VL7C215/VL7C212A chip set. In addition to including the functionality of the VL82C50 UART, the VL7C215 contains an 8-bit microprocessor, 8K by 8 bits of ROM and 128 by 8 bits of RAM.

For specific high-volume applications, the control program can be modified by VLSI to include additional command functions.

PIN DIAGRAMS



BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Package
VL7C215-PC	Plastic DIP
VL7C215-QC	Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range is 0°C to +70°C.

SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Description
-DOST	1	The CPU can write data or control words into a selected register of the VL7C215 when -DOST is low and the chip is selected. Data is latched on the rising edge of the signal.
-DIST	2	The CPU can read data or status information from a selected register of the VL7C215 when -DIST is low and the chip is selected.
IORDY	3	This open-drain output will go low upon a write or read operation, and remain low until internal data setup and hold times have been satisfied.
KDV	4	This output controls the operation of the data/voice relay. When low, the data/voice relay is off and the phone line is connected to the phone set. During a data call, the VL7C215 makes this output high to operate the data/voice relay, disconnecting the phone set from the phone line. It may also be used to drive a relay for multi-line phone applications to close the A and A1 leads.
-RI	5	The output of the ring detector in the DAA is connected to this input. A low level on this input indicates the "On" duration of the ring cycle. This is a Schmitt-trigger input, allowing for slow rising and falling signals on this pin.
OH	6	This output controls the operation of the hookswitch relay in the DAA. During a data call, this output is high. It operates the hookswitch relay which causes the phone line to be seized. During rotary dialing, the VL7C215 pulses this output at a rate of 10 pulses per second with appropriate Mark/Space ratio depending on 212A or V.22 mode.
CLK	7	A 7.3728 MHz clock signal must be connected to this input. Normally, the CKOUT pin of the VL7C212A modem is connected to this pin. All internal timing is derived from this clock. This clock must be adjusted to within 0.01%.
-WR	8	This pin is used to initiate writing of data to the VL7C212A modem. On power-up, it is an input for a brief time in which the VL7C215 reads the carrier status switch connected to this pin. If the switch is closed to ground through an 18 K Ω resistor, the VL7C215 sets the Received Line Signal Detect (RLSD) Bit in the Modem Status Register. If the switch is open, the VL7C215 resets this bit and writes the actual status of the carrier detector during a data call. If no switch is used, an internal pull-up sets the status during power-up to the default state (pull-up to VCC) which is to follow the remote modem's carrier.
-RD	9	This pin is used to initiate reading of data from the VL7C212A modem. On power-up, this pin is an input for a brief time in which the VL7C215 reads the DTR status switch connected to this pin. If this switch is open, the VL7C215 reacts to the status of the DTR bit in the UART Modem Control Register. If the switch is closed to ground through 18 k Ω , the VL7C215 ignores the state of the DTR bit. When the switch is open, writing a zero to the DTR bit in the Modem Control Register forces the VL7C215 into the command state and when on-line, causes it to hang up. If no switch is used, an internal pull-up to VCC sets the status during power-up to the default state (to follow the DTR status).
SCK	10	The VL7C215 supplies a shift clock on this pin to the VL7C212A modem for reading or writing data. On power-up, this pin is an input for a brief time in which the VL7C215 reads the Bell/CCITT select switch connected to this pin. If this switch is open, Bell protocol is selected. If this switch is closed to ground through 18 k Ω , CCITT V.22 protocol is selected. If no switch is used, an internal pull-up sets the status during power-up to the default state (212A mode).
DI/O	11	The VL7C215 shifts data serially out of this pin to VL7C212A during a write operation and shifts data serially into this pin during a read operation from the VL7C212A. On power-up this pin is an input for a brief time in which the VL7C215 reads the Make/Break ratio select switch connected to this pin for selecting the pulse dialing standard. With the switch open, the Bell standard 39% Make, 61% Break is selected. With the switch closed to ground through 18 k Ω , the CCITT standard 33% Make, 67% Break is selected. If no switch is used, an internal pull-up sets the status during power-up to the default state (Bell standard).

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Description
TXD	12	This pin is a serial output pin. During a data call, after the connection is established, the VL7C215 converts parallel data received from the computer bus and outputs it in a serial, asynchronous format to the VL7C212A modem for modulation. At all other times the VL7C215 holds this output in the Mark (high) condition.
RXD	13	Demodulated data from the VL7C212A modem is received on this pin during a data call. A high level is considered Mark and a low level is Space. The VL7C215 converts the serial data into a parallel data byte and stores it in the Receiver Buffer Register (RBR). The Data Ready bit in the Line Status Register (LSR) is then set, and an appropriate interrupt identification code is written in the Interrupt Identification Register (IIR) to signal to the computer, the reception of a new data byte.
GND	14	Ground reference (0 V).
D0-D7	15-22	This is the 8 bit data bus comprising of three-state input/output lines. This bus provides bidirectional communication between the VL7C215 and the CPU. Data control words and status information are transferred via the D0 - D7 data bus.
INT	23	This output goes high whenever any one of the following interrupt types has an active condition and is enabled via the IER: Receiver Line Status flag, Received Data Available, Transmitter Holding Register Empty, and Modem Status. It is reset low upon the appropriate interrupt servicing. The INT pin is forced to a high impedance state when the OUT2 bit of the Modem Control Register (MCR) is low (power on state).
A0-A2	24-26	These three address inputs are used during read or write operation to select a UART register in the VL7C215 as shown in Table 1. The Divisor Latch Access Bit (DLAB) must be set high by the system software to access the bit rate divisor latches as shown in Table 2.
-CS	27	The VL7C215 is selected when this input is low. When high, the VL7C215 forces the Data bus lines into a high impedance state.
VCC	28	Positive supply (+5 V).

TABLE 1. VL7C215 UART REGISTERS

DLAB	A2	A1	A0	Mnemonic	Register
0	0	0	0	RBR	Receiver Buffer Register (read only)
0	0	0	0	THR	Transmitter Holding Register (write only)
0	0	0	1	IER	Interrupt Enable Register
X	0	1	0	IIR	Interrupt Identification Register (read only)
X	0	1	1	LCR	Line Control Register
X	1	0	0	MCR	Modem Control Register
X	1	0	1	LSR	Line Status Register
X	1	1	0	MSR	Modem Status (read only) Register
X	1	1	1	STR	Speed
1	0	0	0	DLL	Divisor Latch (LSB) (write only)
1	0	0	1	DLM	Divisor Latch (MSB) (write only)

X = "Don't Care" 0 = Logic Low 1 = Logic High

FIGURE 1. UART BLOCK DIAGRAM

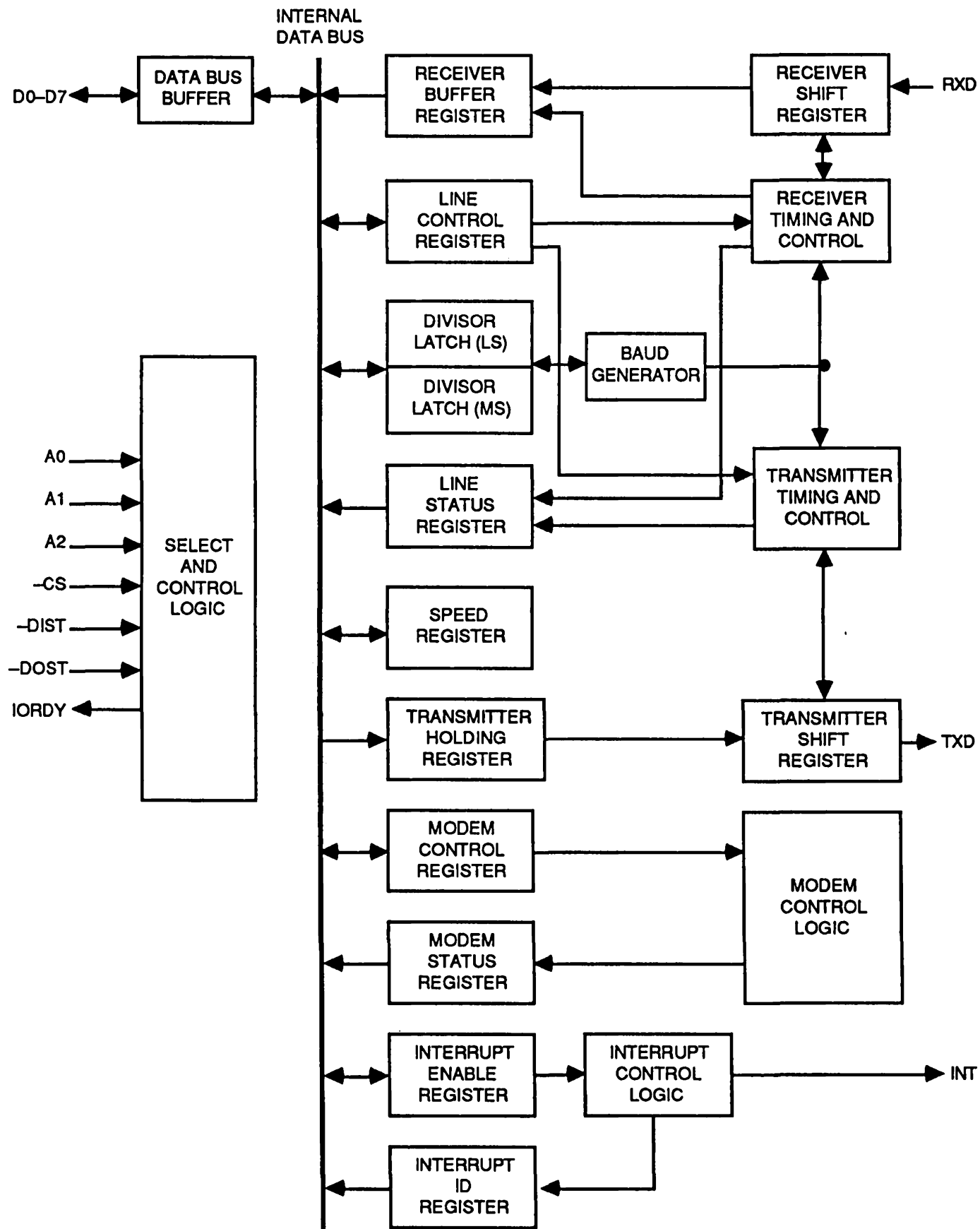


TABLE 2. VL7C215 UART REGISTER FUNCTION SUMMARY

Register Mnemonic	Register Bit Number							
	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
RBR	Data	Data	Data	Data	Data	Data	Data	Data
THR	Data	Data	Data	Data	Data	Data	Data	Data
IER	Receive Data Available Interrupt Enable	THRE Interrupt Enable	Receive Line Status Interrupt Enable	Modem Status Interrupt Enable	0	0	0	0
IIR	0 If Interrupt Pending	Interrupt ID Bit 0	Interrupt ID Bit 1	0	0	0	0	0
LCR	0 = 7 Bit Data 1 = 8 Bit Data	1	0 = 1 Stop Bit 1 = 2 Stop Bits	1 = Parity Enable	1 = Even Parity	1 = Stick Parity	1 = Set Break	DLAB
MCR	Data Terminal Ready	Request to Send	OUT1	OUT2 0 = INT Output to HI-Z	No Function	0	0	0
LSR	Data Ready	Overrun Error	Parity Error	Framing Error	Break Interrupt	THRE	TSRE	0
MSR	0	0	Trailing Edge Ring	Delta RLSD	1 (CTS)	1 (DSR)	RING	RLSD
DLM	Data	Data	Data	Data	Data	Data	Data	Data
DLL	Data	Data	Data	Data	Data	Data	Data	Data
STR	Data	Data	Data	Data	Data	Data	Data	Data

TABLE 3. VL7C215 SOFTWARE REGISTERS

Register	Range/Units	Description	Default
S0	0-255 Rings	Ring to answer telephone on	0
S1	0-255 Rings	Number of rings	0
S2	0-127 ASCII	Escape code character	43 (+)
S3	0-127 ASCII	Character recognized as carriage return	13 (CR)
S4	0-127 ASCII	Character recognized as line feedback	10 (LF)
S5	0-32, 127 ASCII	Character recognized as back space	8 (BS)
S6	2-255 sec.	Wait time for dial tone	2
S7	1-255 sec.	Wait time for carrier	30
S8	0-255 sec.	Pause time (caused by comma)	2
S9	1-255 1/10 sec.	Carrier detect response time	6
S10	1-255 1/10 sec.	Delay between loss of carrier and hang up	7
S11	50-255 millise.	Duration and spacing of Touch-Tones	70
S12	20-255 1/50 sec.	Escape code guard time	50
S13	bit mapped	UART status register	-
S14	bit mapped	Option register	-
S15	bit mapped	Flag register	-
S16	0, 1, 2, 4	Test modes	0

TABLE 4. COMMAND SUMMARY
PREFIX, REPEAT AND ESCAPE COMMANDS

Command	Description (Notes 1 & 2)
AT	Attention prefix: precedes all command lines except + + + (escape) and A/(repeat) commands
A/	Repeat last command line (A/ is not followed by carriage return)
+ + +	Escape code: go from on-line state to command state (one second pause before and after escape code entry; ; + + + is not followed by carriage return)

DIALING COMMANDS

Command	Description (Notes 1 & 2)	Command	Description (Notes 1 & 2)
D	Dial	/	Wait for 1/8 second
P	Pulse*	@	Wait for silence
T	Touch-Tone	W	Wait for second dial tone
,	Pause	;	Return to command state after dialing
!	Flash	R	Reverse mode (to call originate-only modem)

OTHER COMMANDS

Commands	Description (Notes 1 & 2)	Commands	Description (Notes 1 & 2)
A	Answer call without waiting for ring	M1	Speaker on until carrier detected*
B/B0	CCITT V.22 mode (Note 3)	M2	Speaker always on
B1	Bell 103 and 212A mode*	O	Go to on-line state
C/C0	Transmit carrier off	O1	Remote digital loopback off*
C1	Carrier on*	O2	Remote digital loopback request
E/E0	Characters not echoed	Q/Q0	Result codes displayed*
E1	Characters echoed*	Q1	Result codes not displayed
F/F0	Half duplex	Sr?	Requests current value of register r
F1	Full duplex*	Sr = n	Sets register r to value of n
H/H0	On hook (hang up)	V/V0	Digit result codes
H1	Off hook; line and auxiliary relay	V1	Word result codes*
H2	Off hook; line relay only	X/X0	Compatible with Hayes-type 300 modems*
I/I0	Request product ID code (130)	X1	Result code CONNECT 1200 enabled
I1	Firmware revision number	X2	Enables dial tone detection
I2	Test internal memory	X3	Enables busy signal detection
L/L1	Low speaker volume	X4	Enables dial tone and busy signal detection
L2	Medium speaker volume	Y/Y0	Long space disconnect disabled*
L3	High speaker volume	Y1	Long space disconnect enabled
M/M0	Speaker always off	Z	Software reset: restores all default settings

Notes:

1. Default modes are indicated by *.
2. Commands entered with null parameters assume 0 - X is the same as X0.
3. When the ATB command is used in the answer mode, the VL7C212A is placed in either the V.21 or the V.22 mode, depending on the response from the remote modem. In the originate mode, the VL7C215 will sense if the baud rate is set at 300 or 1200 bits per second and will adjust the VL7C212A accordingly.

TABLE 5. RESULT CODES

Digit Code	Word Code	Description
0	OK	Command executed
1	Connect	Connected at 300 or 1200 bps Connected at 300 bps, if result of X1, X2, X3, or X4 command
2	Ring	Ringing signal detected (Note)
3	No Carrier	Carrier signal not detected or lost
4	Error	Illegal command Error in command line Command line exceeds buffer (40 characters, including punctuation) Invalid character format at 1200 bps
5	Connect 1200	Connected at 1200 bps. Results from X1, X2, X3, or X4 commands only
6	No Dialtone	Dialtone not detected and subsequent commands not processed Results from X2 or X4 commands only
7	Busy	Busy signal detected and subsequent commands not processed Results from X3 or X4 commands only
8	No Answer	Silence not detected and subsequent commands not processed Results from @ command only

Note: When the VL7C215 detects a ringing on the telephone line, it sends a RING result code. However, the VL7C215 will answer the call only if it is in auto-answer mode or is given an A command.

TABLE 6. RESET CONTROL OF REGISTERS AND PINOUT SIGNALS

Register/Signal	Reset Control	Reset State
Receiver Buffer Register	First word received	Data
Transmitter Holding Register	Writing into the Transmitter Holding Register	Data
Interrupt Enable Register	Power on reset	All bits low
Interrupt Identification Register	Power on reset	Bit 0 high; bits 1–7 low
Line Control Register	Writing into the LCR	Data
MODEM Control Register	Power on reset	All bits low
Line Status Register	Power on reset	Bits 0–4, 7 low; bits 5–6 high
Modem Status Register	Power on reset	Bits 0–3, 6–7 low; bits 4–5 high
Divisor Latch (high order bits)	Power on reset	1200 bps
TXD	Master reset	High
INT	Power on reset	Low (high impedance)

UART REGISTERS

Line Control Registers

This register controls the format of the asynchronous data communications.

Bit 0 and 1: Bit 1 is always high. Bit 0 specifies the number of bits in each transmitted or received serial character.

The encoding of bit 0 is as follows:

Bit 1	Bit 0	Word Length
1	0	7 Bits
1	1	8 Bits

Bit 2: This bit specifies the number of Stop bits in each transmitted or received serial character. If bit 2 is a logic 0, one Stop bit is generated or checked in the transmit or receive data, respectively. If bit 2 is a logic 1, when 7-bit word length with no Parity is selected, two Stop bits are generated or checked.

Bit 3: This bit is the Parity Enable bit. When bit 0 is a logic 0 and bit 3 is a logic 1, a Parity bit is generated (transmit data) or checked (receive data) between the last data word bit and the Stop bit of the serial data. (The Parity bit is used to produce an even or odd number of 1s when the data word bits and the Parity bit are summed.)

Bit 4: This bit is the Even Parity Select bit. When bit 3 is a logic 1 and bit 4 is logic 0, and odd number of logic 1s is transmitted or checked in the data word bits and Parity bit. When bit 3 is logic 1 and bit 4 is a logic 1, an even number of bits is transmitted or checked.

Bit 5: This bit is the Stick Parity bit. When bit 3 is logic 1 and bit 5 is logic 1, the Parity bit is transmitted and then detected by the receiver in the opposite state indicated by bit 4.

Bit 6: This bit is the Set Break Control bit. When bit 6 is a logic 1, the serial output (TXD) is forced to the Spacing state (logic 0) and remains there (until reset by a low-level bit 6) regardless of other transmitter activity. The feature enables the CPU to alert a terminal in a computer communications system.

Bit 7: This bit is the Divisor Latch Access Bit (DLAB). It must be set high (logic 1) to access the Divisor Latches of the Baud Rate Generator during a Read or Write operation. It must be set low (logic 0) to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

Programmable Baud Rate Generator

The VL7C215's Baud Rate Generator can be programmed for one of six baud rates. The desired speed is selected by writing into the Divisor Latch (DLM). On reset, the rate will be 1200 baud.

DLM (Hex Code)	Baud Rate
00	1200
01	300
03	150
04	110
06	75
09	50

Line Status Register

This 8-bit register provides status information to the CPU concerning the data transfer. The contents of the Line Status Register are indicated in Table 2 and are described below:

Bit 0: This bit is the receiver Data Ready (DR) indicator. Bit 0 is set to a logic 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register. Bit 0 will reset to a logic 0 either by the CPU reading the data in the Receiver Buffer Register or by writing a logic 0 into it from the CPU.

Bit 1: This bit is the Overrun Error (OE) indicator. Bit 1 indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.

Bit 2: This bit is the Parity Error (PE) indicator. Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even parity select bit. The PE bit is set to a logic 1 upon detection of parity error and is reset to a logic 0 whenever the CPU reads the contents of the Line Status Register.

Bit 3: This bit is the Framing Error (FE) indicator. Bit 3 indicates that the received character did not have a valid Stop bit. Bit 3 is set to a logic 1 whenever the Stop bit following the last data bit or parity bit is detected as a zero (Spacing level).

Bit 4: This bit is the Break Interrupt (BI) indicator. Bit 4 is set to a logic 1

whenever the received data input is held in the Spacing (Logic 0) state for longer than a full word transmission time - the total time of Start bit + data bits + Parity + Stop bits.

Bit 5: This bit is the Transmitter Holding Register Empty (THRE) indicator. Bit 5 indicates that the VL7C215 is ready to accept a new character for transmission. In addition, this bit causes the VL7C215 to issue an interrupt to the CPU when the Transmit Holding Register Empty enable is set high. The THRE bit is set to a logic 0 concurrently with the loading of the Transmitter Holding Register by the CPU.

Bit 6: This bit is the Transmitter Shift Register Empty (TSRE) indicator. Bit 6 is set to a logic 1 whenever the Transmitter Shift Register is idle. It is reset to logic 0 upon a data transfer from the Transmitter Holding Register to the Transmitter Shift Register.

Bit 7: This bit is permanently set to logic 0.

Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected.

Interrupt Identification Register

The VL7C215 has an on-chip interrupt capability that allows for complete flexibility in interfacing to all popular microprocessors. To provide minimum software overhead during data character transfers, the VL7C215 prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows: Receiver Line Status (priority 1); Received Data Ready (priority 2); Transmitter Holding Register Empty (priority 3); and MODEM Status (priority 4).

Information indicating that a prioritized interrupt is pending the source of that interrupt are stored in the Interrupt Identification Register (refer to Table 7). The Interrupt Identification Register (IIR), when addressed during chip-select time, freezes the highest priority interrupt pending and no other interrupts are acknowledged until the particular interrupt is serviced by the CPU. The contents of the IIR are indicated in Table 2 and are described below.

Bit 0: This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When bit 0 is a logic, no interrupt is pending.

Bits 1 and 2: These two bits of the IIR are used to identify the highest priority interrupt pending as indicated in Table 7.

Bits 3 through 7: These five bits of the IIR are always logic 0.

Interrupt Enable Register

This 8-bit register enables the four interrupt sources of the VL7C215 to separately activate the Interrupt (INT) output signal. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the Interrupt Enable Register. Similarly, by setting the appropriate bits of this register and the active (high) INT output from the chip. All other system functions operate in their normal manner, including the setting of the Line Status and MODEM Status Register. The contents of the Interrupt Enable Register are indicated in Table 2 and are described below.

Bit 0: This bit enables the Received Data Available Interrupt when set to logic 1.

Bit 1: This bit enables the transmitter Holding Register Empty Interrupt when set to a logic 1.

Bit 2: This bit enables the Receiver Line Status Interrupt when set to logic 1.

Bit 3: This bit enables the MODEM Status Interrupt when set to logic 1.

Bit 4 through 7: These four bits are always logic 0.

MODEM Control Register

This 8-bit register controls the interface with the MODEM. The contents of the MODEM Control Register are indicated in Table 2 and are described below.

Bit 0: This bit controls Data Terminal Ready (DTR) signal. If the external switch on the -RD pin is set to VCC through an 18 kΩ resistor, setting the DTR low will force the VL7C215 into the command state and if on line, it will hang up.

Bit 1: This bit controls the Request to Send (RTS) signal. This signal is not used by the VL7C215.

Bit 2: This bit controls the Output 1 (OUT1) signal. This signal is not used by the VL7C215.

Bit 3: This bit controls the Output 2 (OUT2) signal. When OUT2 is a 0, the interrupt output is in high impedance state.

Bit 4: Not used.

Bits 5 through 7: These bits are permanently set to logic 0.

MODEM Status Register

This 8-bit register provides the current state of the control lines from the

MODEM (or peripheral device) to the CPU. In addition to this current-state information, two bits of the MODEM Status Register provide change information. These bits are set to a logic 1 whenever a control input from the MODEM changes state. They are reset to logic 0 whenever the CPU reads the MODEM Status Register.

The contents of the MODEM Status Register are indicated in Table 2 and are described below.

Bits 0 and 1: These bits are always 0.

Bit 2: This bit is the Trailing Edge of Ring Indicator (TERI) detector. Bit 2 indicates that the -RI input to the chip has changed from On (logic 1) to an Off (logic 0) condition.

Bit 3: This bit is the Delta Received Line Signal Detector (DRLSD) indicator. Bit 3 indicates that the carrier detector has changed state.

Bit 4: This bit is always 1.

Bit 5: This bit is always 1.

Bit 6: This bit is the complement of the Ring Indicator (-RI) input.

Bit 7: This bit is the Received Line Signal Detect (RLSD) signal.

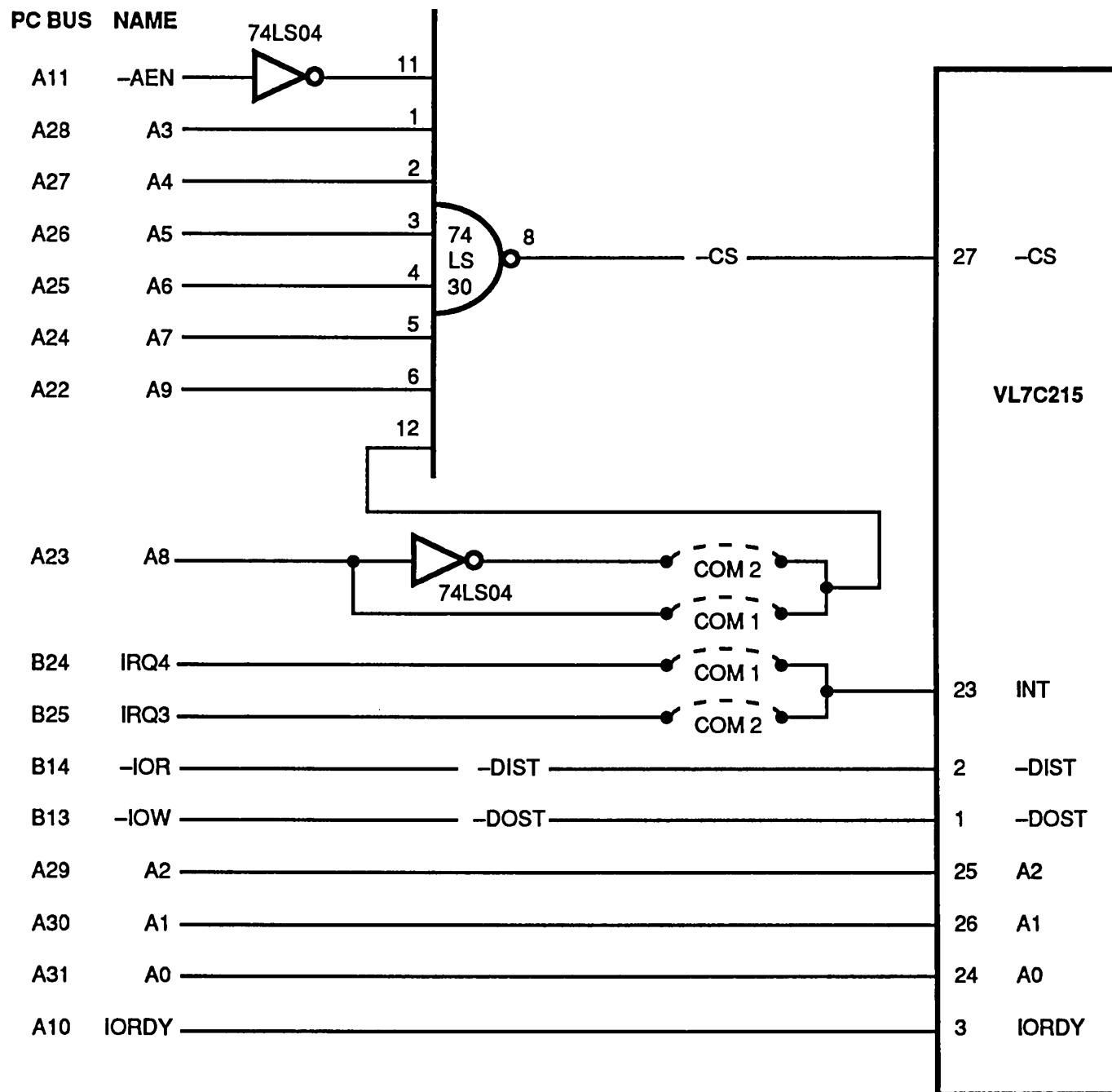
Whenever bit 2 is set to logic 1, or bit 3 changes state, a MODEM Status Interrupt is generated if enabled.

TABLE 7. INTERRUPT CONTROL FUNCTIONS

Interrupt Identification Register			Interrupt Set and Reset Functions			
Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Flag	Interrupt Source	Interrupt Reset Control
0	0	1		None	None	
1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error or Framing Error or Break Interrupt	Reading the Line Status Register
1	0	0	Second	Received Data Available	Received Data Available	Reading the Receiver Buffer Register
0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR (if source of interrupt) or Writing into the Transmitter Holding Register
0	0	0	Fourth	MODEM Status	Ring Indicator or Received Line Signal Detect	Reading the MODEM Status Register



FIGURE 2. ADDRESS DECODER CIRCUIT



AC CHARACTERISTICS: TA = 0 TO 70°C, VCC = 5 V ±10%

Symbol	Parameter	Min	Max	Units	Conditions
tDIW	–DIST Strobe Width	300		ns	1TTL Load
tRC	Read Cycle Delay	300		ns	1TTL Load
RC	Read Cycle = tDIW + tRC + 20 ns	620		ns	1TTL Load
tDDD	Delay from –DIST to Data		300	ns	1TTL Load
tHZ	–DIST to Floating Data Delay	60		ns	1TTL Load
tDOW	–DOST Strobe Width	300		ns	1TTL Load
tWC	Write Cycle Delay	300		ns	1TTL Load
WC	Write Cycle = tDOW + tWC + 20 ns	620		ns	1TTL Load
tDS	Data Setup Time	60		ns	1TTL Load
tDH	Data Hold Time	60		ns	1TTL Load
tDIC	–DIST Delay from Select	150		ns	1TTL Load
tDOC	–DOST Delay from Select	150		ns	1TTL Load
tACR	Address and Chip Select Hold Time from –DIST	10		ns	1TTL Load
tACW	Address and Chip Select Hold Time from –DOST	1		ns	1TTL Load
tDIOR	–DIST/–DOST to IORDY Delay		TBD	ns	1TTL Load
tWIOR	IORDY Pulse Width	TBD		ns	1TTL Load
Receiver					
tRINT	Delay from –DIST (Read RBR) to Reset Interrupt		1	μs	100 pF Load
Transmitter					
tHR	Delay from –DOST (Write THR) to Reset Interrupt		1	μs	100 pF Load
tIRS	Delay from Initial INTR Reset to Transmit Start		1	Baud Cycle	
tSI	Delay from Initial Write to Interrupt		1	Baud Cycle	
tSS	Delay from Stop to Next Start		1	μs	
tSTI	Delay from Stop to Interrupt (THRE)		1	Baud Cycle	
tIR	Delay from –DIST (Read IIR) to Reset Interrupt (THRE)		1	μs	100 pF Load

Note: A TTL load is 40 μA sourced and -1.6 mA sinked current.

FIGURE 3. READ CYCLE TIMING

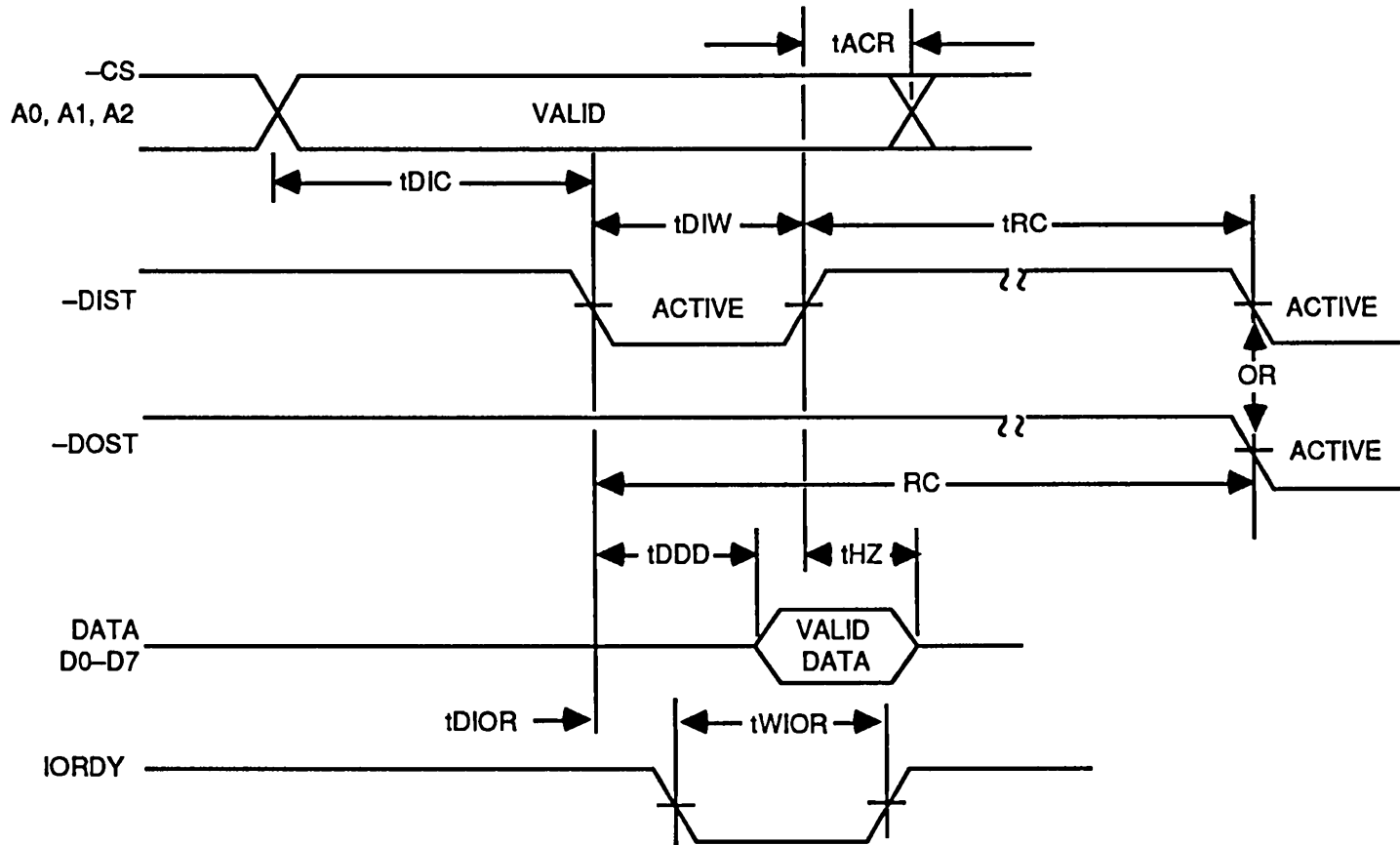


FIGURE 4. WRITE CYCLE TIMING

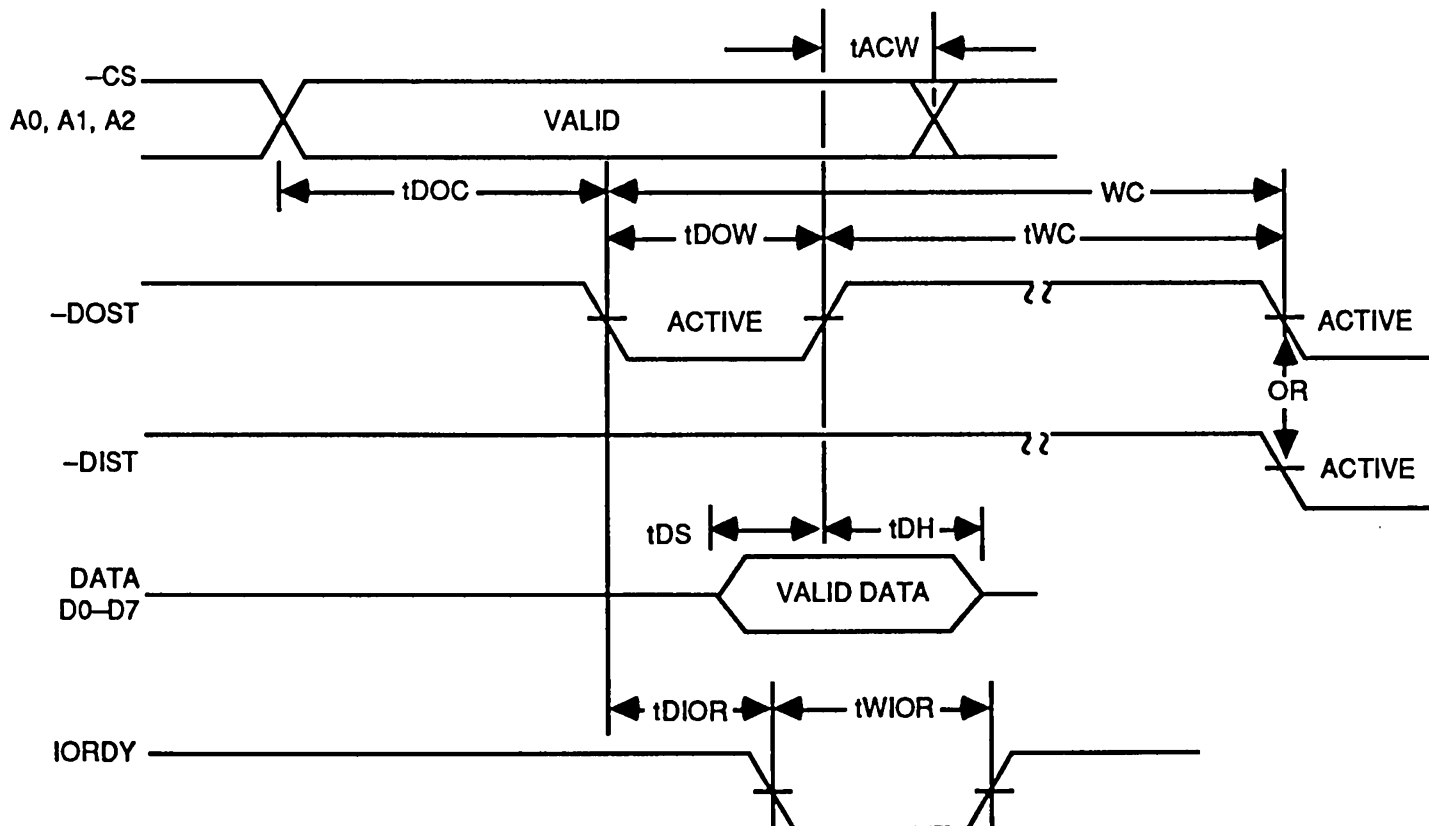


FIGURE 5. RECEIVER TIMING

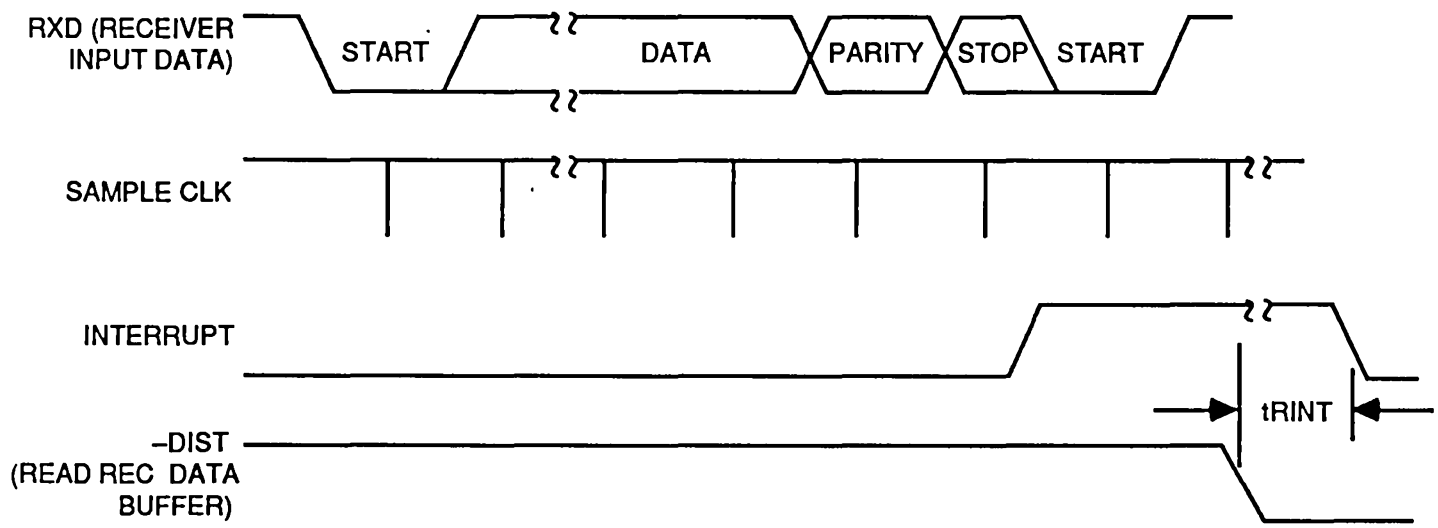
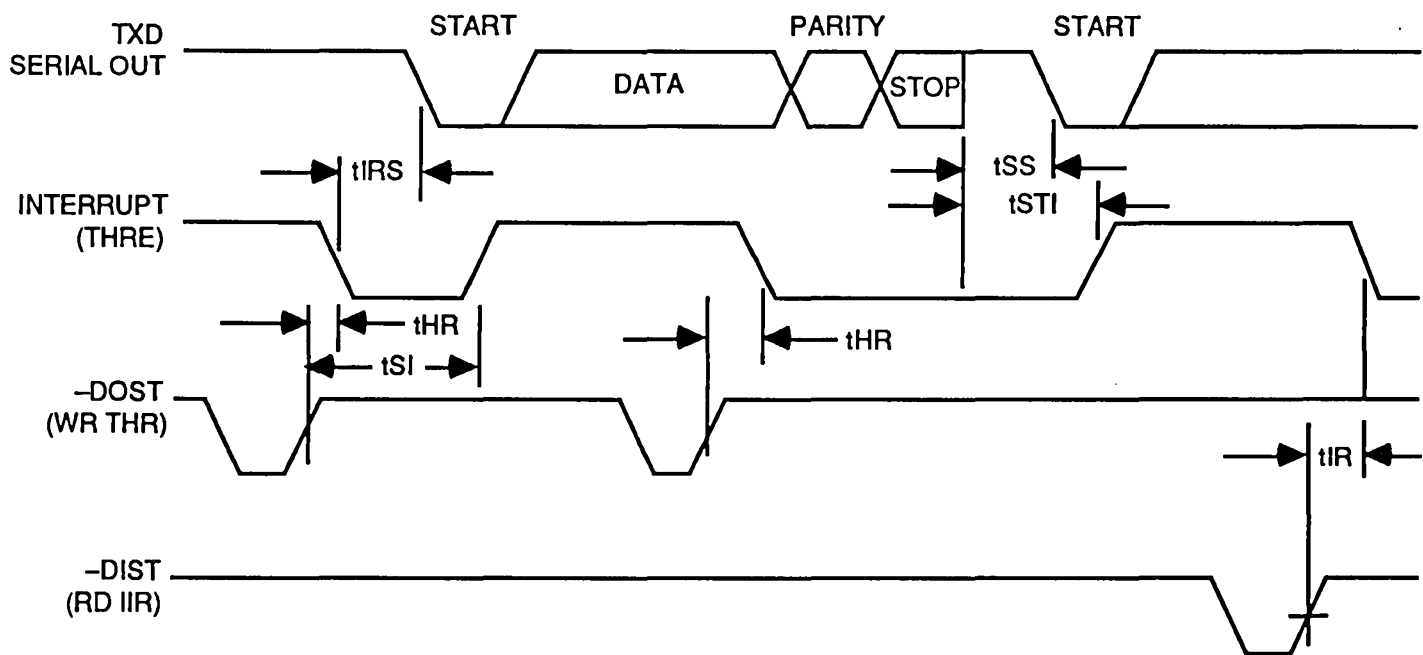


FIGURE 6. TRANSMITTER TIMING



ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature 0°C to +70°C
 Storage Temperature -65°C to +150°C
 Supply Voltage to Ground Potential +6 V
 Applied Input Voltage -0.6 V to VCC +0.6 V
 Power Dissipation 500 mW

Stresses above those listed may cause permanent damage to the device.
 These are stress ratings only, functional operation of this device at these or any other conditions above those indicated

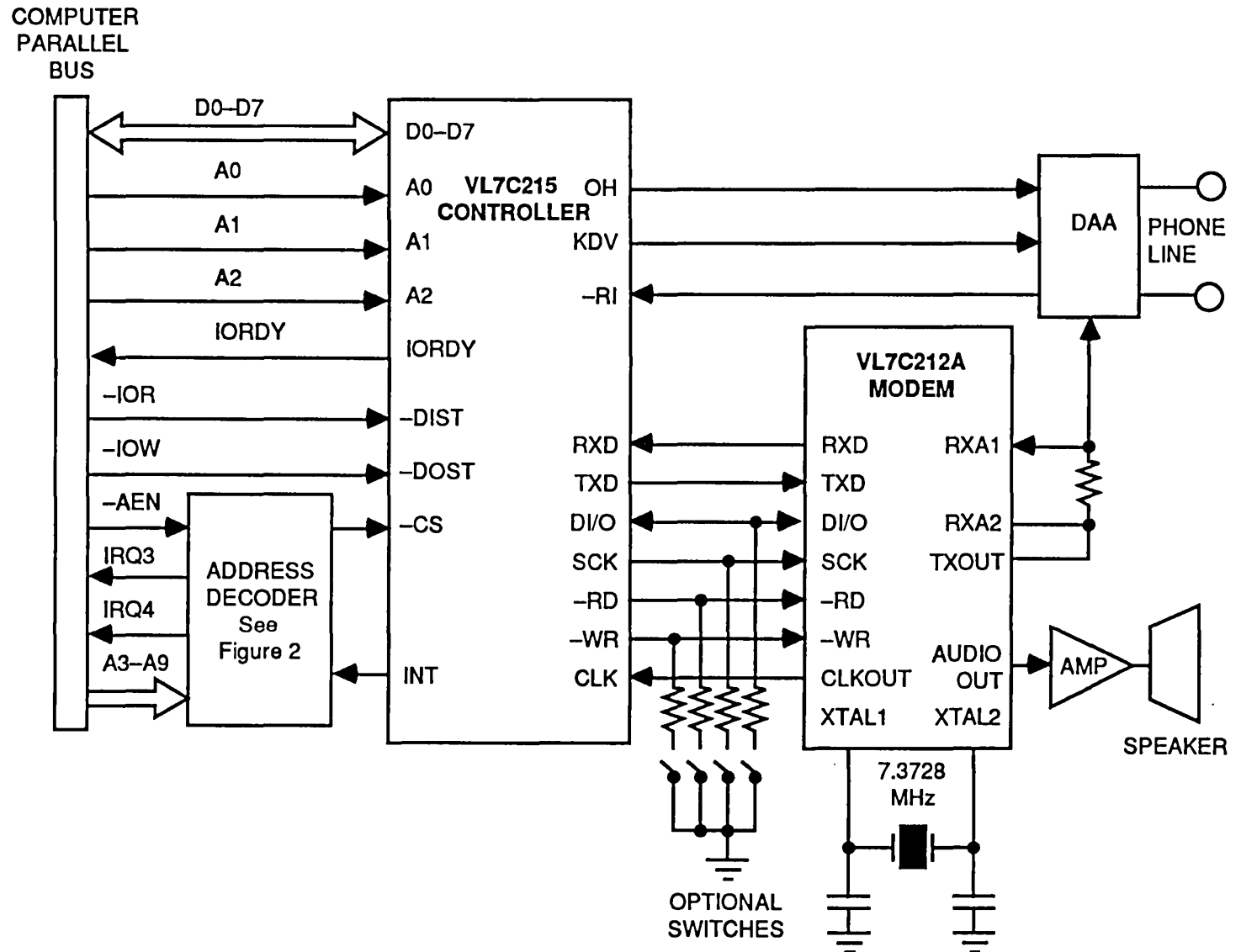
in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS: TA = 0 to +70 °C, VCC = 5 V ±10%

Symbol	Parameter	Min	Typ	Max	Units	Conditions
VCC	Positive Supply Voltage	4.5	5.0	5.5	V	
ICC	Operating Current		10.0		mA	@ VCC = 5 V
VIH	High Level Input Voltage	2.0			V	All pins except -RI
VIL	Low Level Input Voltage			0.8	V	All pins except -RI
VT+	Positive Hysteresis Threshold		2.5		V	-RI pin
VT-	Negative Hysteresis Threshold		1.8		V	-RI pin
VOH	High Level Output Voltage	VCC - 1.0			V	Digital signal pins D0 to D7 and INT @ IOH = -6 mA
		VCC - 1.0			V	All other output or I/O pins @ IOH = -2 mA
VOL	Low Level Output Voltage			0.4	V	Digital signal pins D0 to D7 and INT @ IOL = 6 mA
				0.4	V	All other output or I/O pins @ IOL = 2 mA
IL	Leakage Current (Note)		±1.0		µA	
FCLK	Clock Frequency	7.3721	7.3728	7.3735	MHz	

Note : This applies to all pins except TEST, which has an internal pull-down -WR, -RD, SCK, D/I/O and switch input pins which have internal pull-ups.

FIGURE 7. INTEGRAL SMART MODEM CONFIGURATION FOR PC BUS APPLICATIONS



VL7C224A

2400 BIT-PER-SECOND MODEM

FEATURES

- Complete 2400 bit-per-second modem conforming to V.22 bis specifications
- Compatible with CCITT V.22 bis, V.22, V.21 and BELL 212A and 103 standards
- Integrated DTMF/GUARD TONE GENERATOR, call progress monitor and contains an on-chip hybrid
- Analog, digital and remote digital loopback
- Programmable audio output port
- Three-micron CMOS technology
- DIP or PLCC package
- High-level of integration provides for economical 2400 bit-per-second modem solution

- Broadly adaptable to established worldwide standards at 2400, 1200 and 300 bits-per-second
- Minimizes need for external components simplifying design of intelligent modems
- Testable signal path diagnostics
- Audio interface for phone line monitoring
- Low power consumption

DESCRIPTION

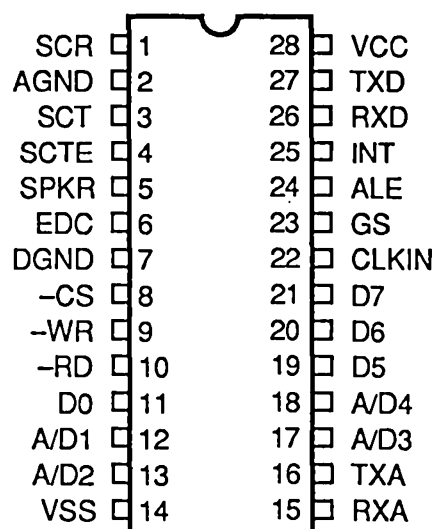
The VL7C224A is a complete 2400 bit-per-second modem IC containing all modem functions except the adaptive equalizer. It is used in conjunction with an external controller such as the VL7C235 (for parallel bus applications), the VL7C245 (for RS-232 applications) or a general purpose microcontroller such as 8096, to implement

a 2400 bps full duplex modem, compatible with the CCITT V.22 bis recommendation. The controller performs all modem control and handshaking functions as well as the adaptive equalization.

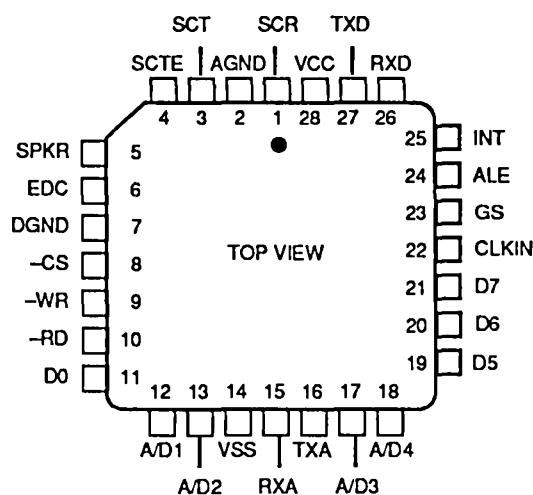
The VL7C224A operates in 2400 bps QPSK/QAM and 1200 bps PSK as well as 0 to 300 baud FSK modes, compatible with Bell 103 and 212A as well as CCITT V.21, V.22 and V.22 bis standards. When used with the VL7C225, VL7C235, or VL7C245 controllers, the VL7C224A becomes an intelligent modem controlled by the industry standard "AT" command set. The interface between the VL7C224A modem and the controller (either the 8096 or the VL7C225/235/245) is a standard microcontroller interface that easily connects to an EEPROM for permanent storage of configuration settings and phone numbers.

PIN DIAGRAMS

VL7C224A-PC



VL7C224A-QC

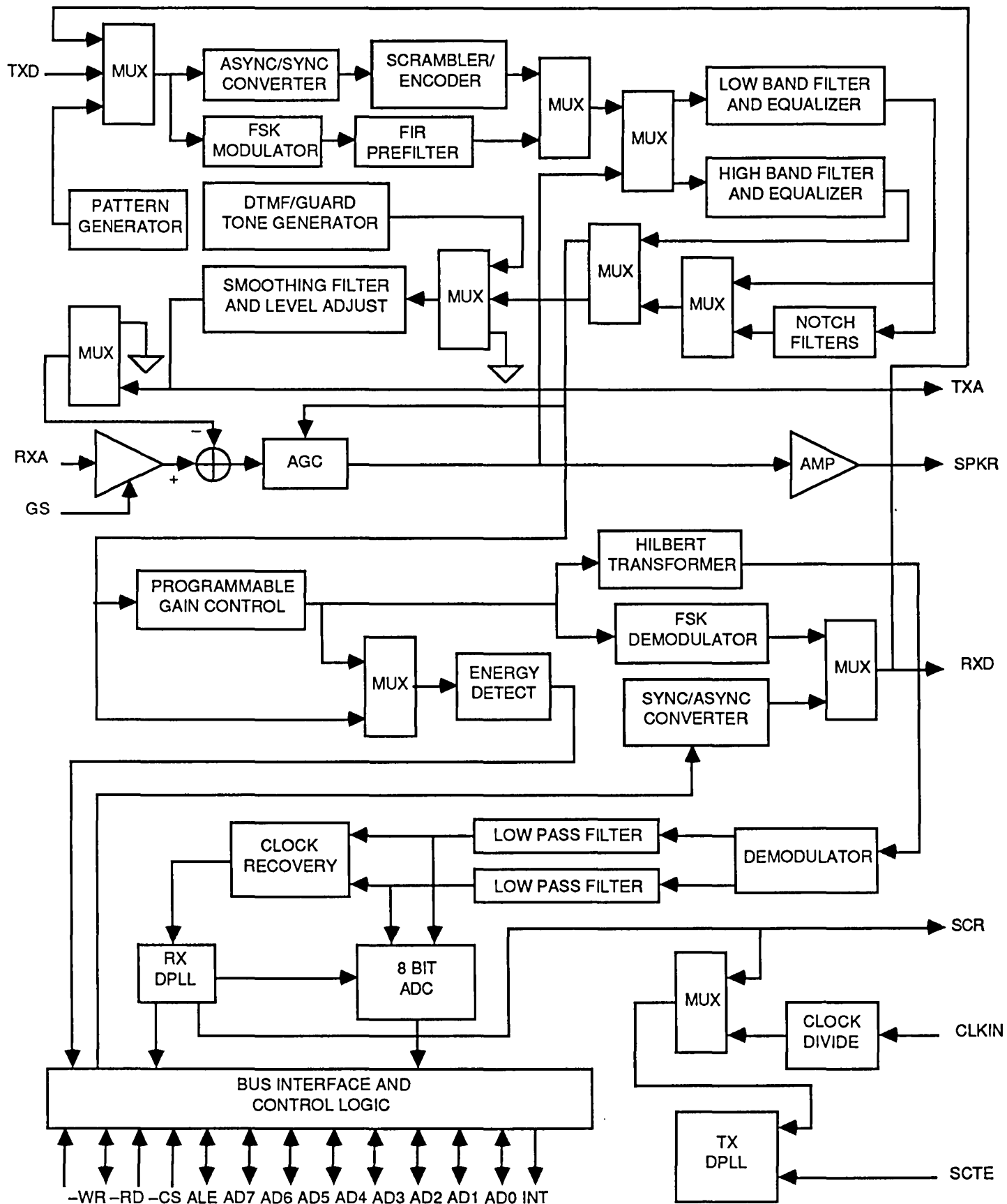


ORDER INFORMATION

Part Number	Package
VL7C224A-PC	Plastic DIP
VL7C224A-QC	Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range is 0°C to +70°C.

FIGURE 1. BLOCK DIAGRAM



SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Description
SCR	1	Synchronous Clock Receive (Data set source) - A TTL output that is used only in bit synchronous mode. It's recovered by the receiver phase locked loop from the far end modem. Data on RX is valid at the rising edge of this clock.
AGND	2	Analog Ground
SCT	3	Synchronous Clock Transmit (Data set source) - This TTL output is used only in bit synchronous mode and is generated internally by the VL7C224A clock generator. Rate = 1200 Hz \pm 0.01% or 2400 Hz \pm 0.01%.
SCTE	4	Synchronous Clock Transmit Element (DTE source) - TTL input used only in bit synchronous locked mode and data on TXD line is latched by the VL7C224A at the rising edge of this clock. Clock rate = 1200 Hz \pm 0.01% or 2400 Hz \pm 0.01%.
SPKR	5	Speaker - The hybrid output is passed through a programmable attenuator and fed to this analog pin. Four different levels can be attained by controlling bit 0 and bit 1 of the SPKR register as specified under SPKR register description.
EDC	6	Capacitor for Energy Detect - A 1.0 μ F capacitor should be connected between this pin and AGND.
DGND	7	Digital Ground
-CS	8	Chip Select - An active low TTL input.
-WR	9	Write - This TTL input is normally high. Data on AD0-AD7 is written into the VL7C224A registers at the rising edge of this pulse.
-RD	10	Read - A normally high TTL input. Data on AD0-AD7 is read from the VL7C224A registers at the rising edge of this pulse.
A/D1-A/D4	12,13, 17, 18	Multiplexed Address/Data Bus (8-bits) - These four TTL I/O bits are used for multiplexed addressing and data I/O of internal registers.
VSS	14	Negative Power Supply - -5 V
RXA	15	Receive Analog - Input.
TXA	16	Transmit Analog - Output.
D0, D5-D7	11, 19-21	Data Bus Bits 0, 5, 6, and 7 - They are don't cares as far as the address is concerned.
CLKIN	22	Clock Input - 9.8304 MHz or 12.288 MHz clock input from the VL7C225/235/245, or external controller.
GS	23	Gain Select - To compensate for loss in line coupling transformer. When left open or tied to VSS, the compensation is 0 dB. Connected to ground, +2 dB compensation is provided, and when tied to VDD, the compensation is +3 dB.
ALE	24	Address Latch Enable - The address on A/D4-A/D1 is latched into the VL7C224A address decoder at the falling edge of a positive pulse on this normally low TTL input.
INT	25	Interrupt - A normally low TTL output. A short (13 μ s typical) positive pulse is generated after all A to D conversions are completed.
RXD	26	Received Data - A TTL output.
TXD	27	Transmit Data - A TTL input.
VCC	28	Positive Power Supply - +5 V

FUNCTIONAL DESCRIPTION

- Full transmitter consisting of
 - Async to sync converter
 - Scrambler
 - Data encoder
 - 75% square root of raised cosine pulse shaper
 - Quadrature modulator
 - FSK (Bell 103 and CCITT V.21) modulator
 - Hybrid
- High-band and low-band filters
- High-band and low-band compromise equalizers
- V.22 Notch filter (selectable at 550 or 1800 Hz)
- Transmit smoothing filter
- Programmable attenuator for transmit level adjust
- DTMF, 550 Hz, 1800 Hz, 1300 Hz, and 2100 Hz tone generators
- Transmit clock circuit for synchronous operation (slave, external, and internal modes)
- Pattern generator for generating fixed digital patterns in handshaking mode
- Receive section consisting of
 - 64-step programmable gain controller (PGC)
 - Energy detector at the output of the PCG
 - Hilbert transformer
 - Quadrature demodulator (free running carrier) with low pass filters
 - Baud timing recovery circuit (sampling clock of 600 Hz)
 - FSK demodulator
 - Sync to Async converter
- 8-bit analog to digital converter (ADC)
- Control and status register
- 8-bit microprocessor interface with interrupt and multiplexed address/data lines
- Audio output with level adjust

TRANSMITTER

Since data terminals and computers may not have the timing accuracy required for 2400/1200 bps transmis-

sion (0.01%), timing correction on the incoming data stream must be made. The async/sync convertor accepts asynchronous serial data clocked at a rate between 2400/1200 Hz + 2.3%, - 2.5%. It outputs serial data at a fixed rate of 2400/1200 Hz \pm 0.01% derived from the master clock oscillator. To compensate for the input and output rate differences, a stop bit is either deleted or inserted when necessary. If the input data rate is slower than the output rate, a stop bit is inserted. If the input data rate is faster than the output data rate, a stop bit is deleted. The output of the async/sync convertor is applied to the scrambler.

The scrambler is a 17 bit shift register clocked at 2400/1200 Hz. Outputs from the 14th and 17th stages are exclusive OR'd and further exclusive OR'd with the input data. The resultant data is applied to the D input of the shift register. Outputs from the first four/two stages of the shift register form the quad/dibit that is applied to the QAM/QPSK modulator. The purpose of the scrambler is to randomize data so that the energy of the modulated carrier is spread over the band of interest - either the high-band centered at 2400 Hz or the low-band, centered at 1200 Hz. In the 2400 bps mode, the modem actually sends four bits at a time, called a quadbit; quadbits are sent at 600 baud, the actual rate of transmission; 600 baud is the optimum rate that can be transmitted over the general switched telephone network for a full duplex FDM (frequency division multiplexing) modem because band limit filters in the central office cut off at about 3000 Hz.

In the 2400 bps data rate, the data to be transmitted is divided into groups of four consecutive bits (quadbits). The first two bits of the quadbit is encoded as a phase quadrant change relative to the quadrant occupied by the preceding signal element. The last two bits define one of the four signaling elements associated with the new quadrant.

In the 1200 bps data rate, the data stream is divided into groups of two consecutive bits (dibits), the dibits are used to determine the phase quadrant change relative to the quadrant

occupied by the preceding signal element. The resulting signaling elements from the inphase (I) and quadrature (Q) channels are passed through base-band filters with a square root of raised-cosine shape. The filtered signals subsequently modulate sine and cosine carriers and add to form the QAM/QPSK signal. The wave shaped signal is then passed through either the low-band or high-band filter depending upon originate or answer mode selection.

For low speed operation the FSK modulator is used. It produces one of four precision frequencies depending on originate or answer mode and the 1 (mark) or 0 (space) level of the transmit data. Different frequencies are used for V.21 and 103 modes. The frequencies are produced from the master clock oscillator using programmable dividers. The dividers respond quickly to data changes, introducing negligible bit jitter while maintaining phase coherence. The output of the FSK modulator is applied to the appropriate filter when the low speed mode of the operation is selected.

The filter section consists of low-band (1200 Hz) and high-band (2400 Hz) filters, half-channel compromise amplitude and group delay equalizers for both bands, smoothing filters for both bands and multiplexers for routing of the transmit and receive signals through the appropriate band filters. For CCITT V.22 bis applications, a notch filter is included that can be programmed for either 550 Hz or 1800 Hz. In the call progress monitor mode, the low-band filter is scaled down by a factor of 2.5 to center it over a frequency range of 300 to 660 Hz. Thus, during call establishment in the originate mode, call progress tones can be monitored through the scaled low-band filter and the modem answer tone or voice can be monitored through the unscaled high-band filter.

The low-band filter is a tenth order switched-capacitor band-pass filter with a center frequency of 1200 Hz. In the originate mode, this filter is used in the transmit direction; in the answer mode it is used in the receive direction. When

analog loopback is used in the originate mode, this filter, together with the low-band delay equalizer, is in the test loop. In the call progress monitoring mode, the filter response is scaled down by 2.5, moving the center frequency to 480 Hz.

The low-band delay equalizer is a tenth order switched-capacitor all-pass filter that compensates for the group delay variation of the low-band filter and half of the compromise line characteristics, producing a flat delay response within the pass-band.

The high-band filter is a tenth order switched-capacitor band-pass filter with center frequency of 2400 Hz. In the answer mode, this filter is used in the transmit direction; in the originate mode, it is used in the receive direction. When analog loopback is used in the answer mode, this filter, together with the high-band delay equalizer, will be in the test loop.

The high-band delay equalizer is a tenth order switched-capacitor all-pass filter that compensates for the group delay variation of the high-band filter and half of the compromise line characteristics, producing a flat delay response within the pass-band. The transmit smoothing filter is a second order low-pass switched-capacitor filter that adds the modem transmit signal to the DTMF or V.22 guard tones. It also provides a 2 dB per step programmable gain function to set the output level.

RECEIVER

The receiver section consists of an energy detector, programmable gain control (PGC), part of the QAM/QPSK demodulator, FSK demodulator, 8 bit ADC and sync/async convertor.

The received signal is routed through the appropriate band-pass filter and applied to the energy detector and PGC circuit. The energy detector provides a detection within 17 to 24 msec. It is set to turn on when the signal exceeds -43 dBm and turn off when the signal falls below -48 dBm measured at the chip. A 2 dB minimum hysteresis is provided between the turn on and turn off levels. In call progress mode the energy detector is connected to the output of PGC to allow detection level adjustment.

The output of the filter is applied to the programmable gain control (PGC). This circuit has a wide overall range of 47.25 dB and provides 64 steps of 0.75 dB/step. The PGC gain is controlled by the external processor. It also includes autozeroing to minimize the output DC offset voltage.

The QAM/QPSK demodulator uses a coherent demodulation technique. Output of the programmable gain control (PGC) is applied to a hilbert transformer that produces an in-phase and 90° out of phase component. These components are then demodulated to base-band in a mixer stage where individual components are multiplied by a free running carrier. The base-band components are low-pass filtered to produce I and Q channel outputs. (In phase and quadrature.) The I and Q channel outputs are both filtered by 300 Hz band-pass filters. Then they are rectified, summed and passed through a band-pass filter giving a 600 Hz signal. This signal is applied to a digital phase lock loop (DPLL) to produce a baud rate clock. Using the recovered clock signal, the I and Q channels are sampled and digitized into 8-bit samples by the ADC. Each channel (I and Q) is sampled twice during a baud period, once at the middle and once at the end of the baud period allowing T/2 or T sampling operation. The external processor is interrupted once every baud period (1.667 msec). The processor should read the I and Q samples (within 100 µsec from the time interrupt is issued), and perform adaptive equalization, carrier phase tracking, data decoding, and data descrambling. One quad/dibit is then transferred to the VL7C224A during each baud period.

In the asynchronous mode, data received from the external processor is applied to the sync/async convertor to reconstruct the originally transmitted asynchronous data. For data which had stop bits deleted at the transmitter (overspeed data), these stop bits are reinserted. Underspeed data is passed essentially unchanged. The sync/async convertor has two modes of operation. In the basic signaling mode the buffer can accept an overspeed which corresponds to one missing stop bit in

eight characters. The length of the start and data bits will be the same and the stop bit will be reduced by 12.5%. In the extended signalling range, the buffer can accept one missing stop bit in four characters and the stop bits will be reduced by 25% to allow for overspeed in the transmitting terminal. Output of the sync/async convertor along with the output of the FSK demodulator is applied to a multiplexer. The multiplexer selects the appropriate output, depending on the operating speed, and outputs received data on the RXD pin.

For low speed operation, the FSK demodulator is used. the output of the PGC amplifier is passed through a zero crossing detector and applied to a counter that is reset on zero crossings. The counter is designed to cycle at a rate four times faster than the carrier signal. The counter output is low-pass filtered and hard limited to generate FSK data.

To improve performance of receiver at low signal levels, while maintaining a wide amplitude range, a 1-bit AGC circuit is placed prior to band-pass filter. The decision thresholds of this AGC are controlled by AGCVT bit. When AGCVT = 1, the thresholds will be 6 dB farther apart than when AGCVT = 0, so that probability of gain change will be reduced. The status of the AGC gain is available through AGC0 bit. AGC will have 8 dB more gain when AGC0 = 1. Status of AGC0 should be monitored every baud timing and when it makes a transition (causing gain-hit). PGC's gain should be modified by the external processor accordingly to prevent divergence of the adaptive equalization.

HYBRID

The signal on the phone line is the sum of the transmit and receive signals. The hybrid subtracts the transmitted signal from the signal on the line to form the received signal. It is important to match the hybrid impedance as closely as possible to the telephone line to produce only the received signal. When the internal hybrid is used, by setting the "HYBRID" bit in the control register, this matching is provided by an external resistor connected between the TXA and RXA pins on the VL7C224A. The

filter section provides sufficient attenuation of the out of band signals to eliminate leftover transmit signals from the received signal. The hybrid also acts as a first order low-pass anti-aliasing filter. The hybrid can be deactivated by the external controller.

The VL7C224A internal hybrid is intended to simplify the phone line interface. The internal hybrid can compensate for the loss in the line coupling transformer used in the DAA. Depending upon the transformer selected, the loss can be as little as 1 dB or as high as 3 dB. Internal hybrid can make up for this loss from 0 to 3 dB, using the GS pin.

With higher loss transformers, some degradation in performance at lower signal levels will occur. Specifically, the bit error rate, when operating at receive signal levels below -40 dBm in the presence of noise, will be higher. The energy detect on/off levels measured at the line will also be different from those specified at the chip. An external hybrid circuit, shown in Figure 2, can be used to overcome these losses and achieve maximum performance. In this case the internal hybrid must be turned off.

The external hybrid circuit uses two operational amplifiers, one in the transmit path and the other in the receive path. The VL7C224A internal transmit stage provides a gain of 6 dB over the transmit signal level desired at the line. Under ideal conditions, with no loss in the transformer and perfect line matching, the signal level at the line will then be desired value. In practice, however, there is impedance mismatch and a loss in the coupling transformer. Therefore it may be desired to provide a gain in the transmit and receive paths to overcome the loss. The receive gain GR and transmit gain GT are set by the ratios of resistors R2, R1 and R6, R5, respectively (Figure 2).

The circuit can be analyzed as follows:

$$VR = -(R2/R1) (VTR) + (1 + R2/R1) [R4/(R3 + R4)] VY$$

$$VY = -(R6/R5) VX$$

If R6/R5 is chosen to equal the loss in the transformer, it can be assumed that VY is twice as high as VX (transmit portion of the total line signal). Since

$$VTR = VX + VRX \text{ and } VY = 2 (VX),$$

$$VR = -(R2/R1) (VX + VRX) + (1 + R2/R1) [R4/(R3 + R4)] 2 (VX)$$

$$= -(R2/R1) VRX + \{(1 + R2/R1) [2R4/(R3 + R4)] - (R2/R1)\} (VX)$$

To eliminate any transmit signal from appearing at the received signal input, the second term in the above equation must be set to zero, giving:

$$(1 + R2/R1) [2R4/(R3 + R4)] = R2/R1$$

$$R3/R4 = 1 + (2R1/R2)$$

Additionally,

$$GR = R2/R1 \text{ and } GT = R6/R5$$

These equations can be solved to select component values that meet the desired requirements. For example, if the transmit and receive loss in the coupling transformer is 2.5 dB, then:

$$R2/R1 = \text{INV Log } (GR_{dB}/20) = \text{INV Log } (2.5/20) = 1.333$$

Similarly,

$$R6/R5 = 1.333 \text{ and } R3/R4 = 2.5$$

Some typical values are:

$$R1 = 20k \Omega, R2 = 27k \Omega, R3 = 13k \Omega, R4 = 5.1k \Omega, R5 = 20k \Omega \text{ and } R6 = 27k \Omega.$$

It should be noted that the transmit amplifier is only needed to overcome the loss in line coupling. It can be eliminated since the transmit signal level specification is typically stated as a maximum. Amplifier B, resistors R5 and R6, and capacitor C1 can be eliminated and point VX connected to point VY in the circuit of Figure 2 to achieve a more cost effective external hybrid arrangement.

The VL7C224A with the internal hybrid may also be used on a four-wire system where the transmit and receive signals are kept separate. In this mode, the Hybrid bit in TXCR must be turned off. The transmit signal is connected to a

600 Ω line transformer through a 600 Ω resistor.

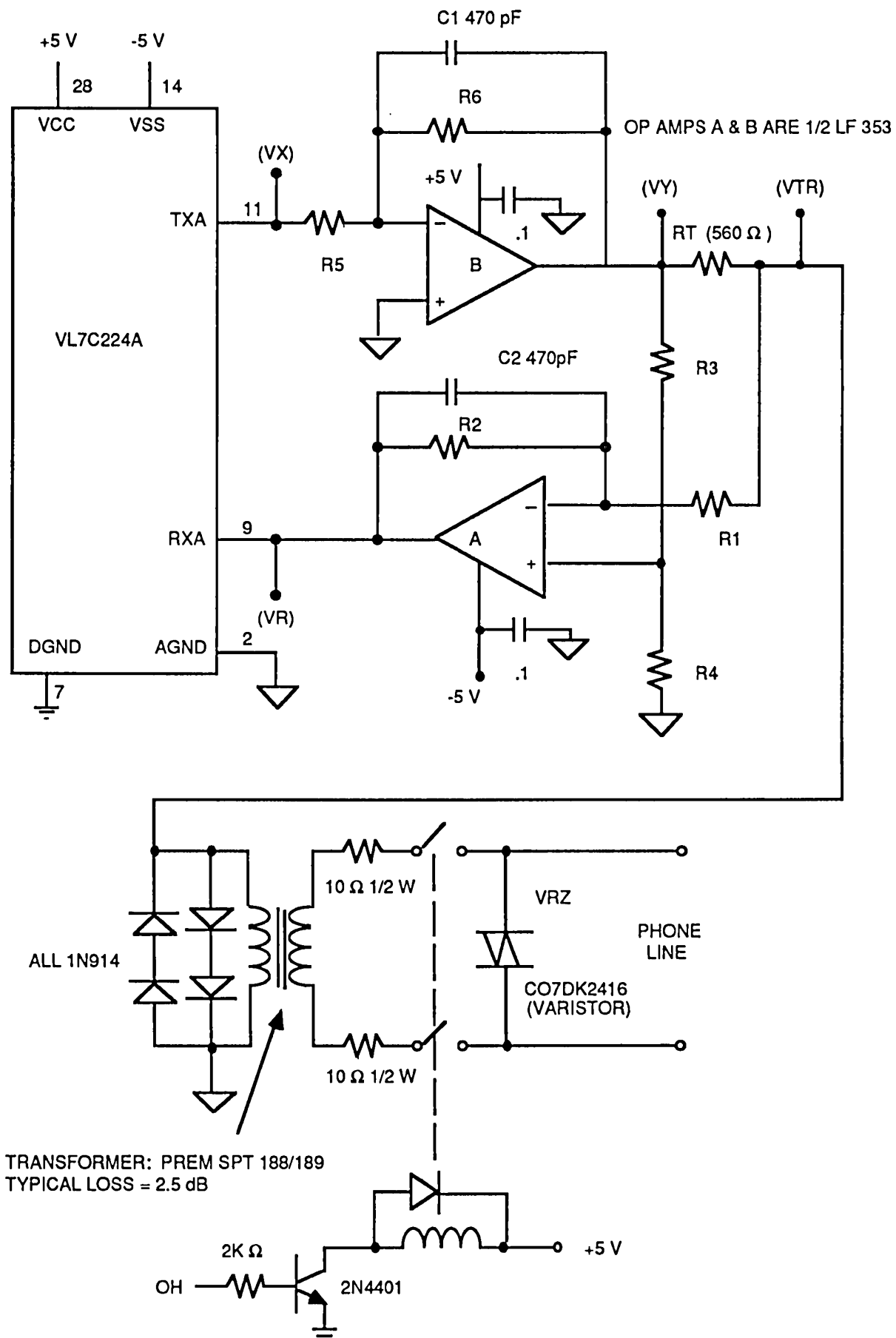
tone generator

The tone generator section consists of a DTMF generator, V.22 guard tone, 1300 and 2100 Hz tone generator. The DTMF generator produces all of the tones corresponding to digits zero through 9 and A, B, C, D, *, and # keys. The V.22 guard tone generator produces either 550 Hz or 1800 Hz tone. Selection of either tone will cascade the corresponding notch filter with the low-band filter. The tones are selected by applying appropriate codes through the Data I/O pin. Before a tone can be generated, tone mode must be selected. Facility is also provided to generate single tones corresponding to 1300 and 2100 Hz and the individual rows or columns of the DTMF signal.

audio output stage

A programmable attenuator that can drive a load impedance of 50k Ω is provided to allow monitoring of the received line signal through an external speaker. The attenuator is connected to the output of the hybrid. Four levels of attenuation - no attenuation, 6 dB attenuation, 12 dB attenuation, and squelch are provided through the ALC1, ALC0 audio output level control codes. Output of the attenuator is available on the audio output pin where an external audio amplifier (LM386 type) can be connected to drive a low impedance speaker. The output can directly drive a high impedance transducer, but the volume level will be low.

FIGURE 2. USING AN EXTERNAL HYBRID WITH THE VL7C224A.



FUNCTIONAL DESCRIPTION OF THE VL7C225, VL7C235, AND VL7C245

The VL7C235 modem controller, implemented in VLSI's two-micron CMOS process, was designed specifically to handle all of the modem control functions, as well as the interface to a system bus. Besides including a 16-bit microprocessor, 8K by 8 bytes of ROM and 304 by 8 bytes of RAM, it also contains the functionality of an 8250B UART, greatly simplifying the interface to a parallel system bus, such as the one used in IBM's PC. In fact, a complete Hayes-type compatible modem for the PC consists of the VL7C235 controller, the VL7C224A modem and the DAA. All of the popular communications software written for the PC will work with the VL7C224A/VL7C225 set.

Another version of the controller, the VL7C245, is intended for RS-232 applications. It contains the same processor, memory and UART as the VL7C224A and has the same interface to the modem chip. The difference is that the UART is turned around so that serial data from the RS-232 port is converted to parallel data handled by the internal processor. Pins are provided for connecting the familiar switches and indicator lamps found on most stand-alone modems, although the switches and lamps are not needed for operation - all of the switch settings can be done through software. A third version, the VL7C225 uses external EPROM memory instead of internal ROM for full customization to specific applications. The internal UART can be software configured (for either parallel bus or serial RS-232 data applications).

The controller receives 8-bit signal sample from VL7C224A and performs adaptive equalization, carrier phase recovery, data decode, and descrambling. VL7C225, VL7C235, and VL7C245 have identical hardware. Each controller can be configured as a VL7C235 or VL7C245 by the software. The controller is designed by using a 16 bit 2900 processor to perform the digital signal processing and the control functions. Its instruction set is a subset of the Intel 8096 instruction set but operates faster than the 8096.

The VL7C245 provides a standard five volt logic level interface. RS-232 drivers are required to interface to the serial port. Like the VL7C235, the VL7C245 comes preprogrammed with the Hayes "AT" command set, and when used with the VL7C224A modem, emulates a Hayes-type stand-alone modem. The VL7C235 and VL7C224A emulate a Hayes-type IBM PC plug-in card modem.

But the chip set is by no means limited to implementing a Hayes-type smart modem. VLSI is in the custom IC business and both chips were designed with this in mind. And since the controller is ROM programmable, any command set, not just the Hayes "AT" set, can be implemented.

Both the VL7C235 and VL7C245 are available in two different pinout options. They are 44-pin and 40-pin. The VL7C225 is available in a 68-pin package. (The 68-pin package allows the controller to access external ROM for up to 32K bytes and external RAM for up to 16K bytes. This allow users to customize their own software. And provides a mean for software development.) The 44-pin and 40-pin packaged VL7C235 and VL7C245 do not provide external ROM access. All three pinouts allow the controller to talk to both the VL7C224A and a SC22102-1 (EEPROM).

The interface to the VL7C224A is via an 8-bit address/data bus and the control lines for read and write. The same interface is used for access to an electrical erasable random access memory (SC22102-1). They operate on six clock multiplexed address/data bus cycles. For the 44-pin option an I/O ready signal is provided for interface to high speed PC/AT type bus cycle. For the VL7C225 there are 15 extra address lines and chip selects for external ROM and external RAM interfaces.

Besides the interface for the VL7C224A modem, the VL7C235 controller has an 8-bit data port, three address lines, a chip select input, an interrupt line, and the DOST and DIST control lines found in the 8250B UART. It also has control

lines for ring indication, the off-hook relay and a data/voice relay; these lines connect to the DAA.

In the VL7C245, the 8-bit port becomes the switch input lines and the address, chip select, INTO, DIST, and DOST lines become the lines for the RS-232 interface, and modem status. These lines are also used to drive the LEDs. Internally, all of these lines are treated as programmable I/O ports under software control - so the main difference between the VL7C235 and VL7C245 is the ROM code. It also contains the same modem and DAA interface lines as the VL7C225A.

The VL7C235 and VL7C245 are designed to control a modem or other peripheral that operates at a moderately slow data rate up to 2400 bits per second. The VL7C235 allows a slow peripheral, such as the modem, to interface to a high speed bus, without making the main processor slow down.

This is done through the UART interface and the on-chip registers which look somewhat like dual port registers. The main processor can write to and read from them at will, while the on-chip controller can do the same. The controller was designed this way because most communications software has to have unrestrained access to the UART registers. To make the VL7C235 compatible with this software, these registers were included.

The actual processor contains a 16-bit data path and can execute 54 instructions with three different addressing modes: direct, indirect, immediate. There is 8K by 8 of ROM on-chip for program storage.

To the system bus, the VL7C235 looks and acts just like an 8250B UART. Communications software written for the UART will work with the VL7C235 and VL7C245. The VLSI chip set is a completely compatible Hayes-type modem in two chips.

In operation, the VL7C235 or VL7C245 monitor the registers to determine the mode of operation - command mode or data mode; at power-up it is automatically put in the command mode and it

looks for instructions. Once carrier is detected, it goes into the data mode, and stays there until an escape

sequence is entered, just like in a Hayes-type modem. The escape sequence is three + signs (+++) in the

default mode, but it can be changed in software.

REGISTERS

There are 12 8-bit registers interfacing to the microprocessor bus. Five of these registers can only be read by the processor (called READ registers) and the remaining seven can be read from or written into by the processor (called CONTROL registers). Table 1 shows the address and bit assignments for these registers.

A chip select pin is provided for multi-peripheral addressing by the processor.

READ REGISTERS

Q1 Register:	Stores Midbaud Quadrature Sample Output of ADC
I1 Register:	Stores Midbaud Inphase Sample Output of ADC
Q2 Register:	Stores Endbaud Quadrature Sample Output of ADC
I2 Register:	Stores Endbaud Inphase Sample Output of ADC
Status Register:	Status information

Note: All samples are represented in two's complement form.

TABLE 1. READ REGISTERS

Address Bits				Name	Bit Number								MSB	LSB
A4	A3	A2	A1		7	6	5	4	3	2	1	0		
0	0	0	1	Q1	Q17	Q16	Q15	Q14	Q13	Q12	Q11	Q10		
0	0	0	0	I1	I17	I16	I15	I14	I13	I12	I11	I10		
0	0	1	1	Q2	Q27	Q26	Q25	Q24	Q23	Q22	Q21	Q20		
0	0	1	0	I2	I27	I26	I25	I24	I23	I22	I21	I20		
0	1	0	0	Status	X	X	X	ACG0	PA	PR	FSKD	ED		
0	1	X	1	Unused										
0	1	1	X	Unused										

TABLE 2. STATUS REGISTER ADDRESS (A4-A1) = 0100

Bit Number	Bit Name	Description
Bit 7-5	Unused	Note 2
Bit 4	AGCO	When this bit is set, RXA signal is being amplified by 8 dB before entering the band-pass filters by the AGC circuit.
Bit 3	PA	This bit is set whenever the DPLL advances one step (skips a count) to lock. It is cleared only when STATUS register is read.
Bit 2	PR	This bit is set whenever the clock recovery DPLL retards one step (adds a count) to lock. It is cleared only when STATUS register is read.
Bit 1	FSKD	Received FSK data. FSKD = 1 when a mark is received.
Bit 0	ED	Energy detect circuit output. ED = 1 when energy is detected.

Notes: 1. When DPLL neither advances nor retards, then PA = PR = 0.

2. When reading unused bits, the corresponding bus lines will not be driven by the VL7C224A and will be floating.

TABLE 3. CONTROL REGISTERS

Address Bits				Name	Bit Number							
A4	A3	A2	A1		7	6	5	4	3	2	1	0
1	0	0	0	TXCR	X	HYBRID	TXSEL2	TXSEL1	TXSEL0	SQT	BR1	BR0
1	0	0	1	MCRA	X	LOCK/-INT	RNGX	SYNC	WLS1	WLS0	A/-O	RXMRK
1	0	1	0	MCRB	X	X	CLKSEL	CPM	ALB	TL2	TL1	TL0
1	0	1	1	TONE	X	HNDSK	TONEON	DTMF	D3	D2	D1	D0
1	1	0	0	PGCR	X	AGCVT	G5	G4	G3	G2	G1	G0
1	1	0	1	DATA	X	PLLJAM	PLLFRZ	PLLFAS	RD3	RD2	RD1	RD0
1	1	1	0	AUDIO	X	DISS	PGCZ	TST2	TST1	TST0	ALC1	ALC2
1	1	1	1	Unused								

TABLE 4. TRANSMIT CONTROL REGISTER (TXCR): ADDRESS (A4-A1) = 1000

Bit Number	Bit Name	Description
Bit 7	Unused	
Bit 6	HYBRID	When set, the transmitter output (TXA) is connected to the inverting input of the receive buffer to allow the use of the on-chip hybrid circuit for 2-to-4 wire conversion
Bit 5	TXSEL2	Transmit Select bit 2. Determines the data transmitted by the transmitter according to Table 5.
Bit 4	TXSEL1	Transmit Select bit 1. Determines the data transmitted by the transmitter according to Table 5.
Bit 3	TXSEL0	Transmit Select bit 0. Determines the data transmitted by the transmitter according to Table 5.
Bit 2	SQT	When this bit is set, the transmitter is squelched by connecting the output of MUX1 (see block diagram) to analog ground.
Bit 1	BR1	Bit Rate Selection bit1. See Table 6.
Bit 0	BR0	Bit Rate Selection bit 0. See Table 6.

Note: When writing into these registers, the bus lines corresponding to the unused bits are ignored by the VL7C224A.

TABLE 5. TRANSMIT SELECTION BITS

TXSEL2	TXSEL1	TXSEL0	Transmitted Data
0	0	0	External data sent by DTE.
0	0	1	Unscrambled S1 (Note 1).
0	1	0	Unscrambled Space.
0	1	1	Unscrambled Mark.
1	0	0	Scrambled RX. Digital loopback mode (Note 2).
1	0	1	Scrambled Reversals (Notes 3 and 4).
1	1	0	Scrambled Space (Note 4).
1	1	1	Scrambled Mark (Note 4).

Notes: 1. S1 is a pattern of 0011 transmitted at 1200 bps rate regardless of BR1. If in FSK mode (BR0 = 1), then reversals are sent. This pattern cannot be sent at 2400 bps rate.
2. In this mode the received data, after being descrambled, is sent back to the scrambler. The modem will automatically go to the synchronous mode with slave timing.
3. Reversals are continuous streams of 01.
4. When in FSK mode (BR0 = 1), TXSEL2 is ignored since scrambling is not applicable.

TABLE 6. BIT RATE SELECTION BITS

BR1	BR0	Bit Rate
0	0	2400 bps V.22 bis
1	0	1200 bps V.22/212A
0	1	0-300 bps Bell 103
1	1	0-300 bps CCITT V.21

TABLE 7. MODE CONTROL REGISTER A (MCRA): ADDRESS (A4-A1) = 1001

Bit Number	Bit Name	Description
Bit 7	Unused	
Bit 6	LCK/-INT	Determines the clock source for the transmitter. When this bit is set clock source is externally provided on SCTE (pin 4), and when cleared it is internally generated (SCT). This bit can select the clock source independent of sync/async mode selection (see below). When in digital loopback mode, the clock source will be forced to the slave mode.
Bit 5	RNGX	Range extender for the receiver sync/async converter. When set, the receiver sync/async can insert up to one stop bit per four (8, 9, 10, or 11-bit) characters to compensate for a far end DTE being up to 2.3% overspeed. The transmitter async/sync always handles this overspeed condition regardless of this bit's condition.
Bit 4	SYNC	When set, operate in bit synchronous mode; when clear, operate in character asynchronous mode. When in digital loopback mode, the VL7C224A will be forced to the synchronous mode.
Bit 3	WLS1	Word Length Select bit in asynchronous mode, see Table 8.
Bit 2	WLS0	Word Length Select bit in asynchronous mode, see Table 8.
Bit 1	A/-O	When set, operate in answer mode. When clear, operate in originate mode.
Bit 0	RXMARK	When set, the RXD pin is clamped to the high logical level.

TABLE 8. WORD LENGTH SELECTION BITS

WLS1	WLS0	Number of Bits Per Character
1	0	8
1	1	9
0	0	10
0	1	11

TABLE 9. MODE CONTROL REGISTER B (MCRB): ADDRESS (A4-A1) = 1010

Bit Number	Bit Name	Description
Bit 7, 6	Unused	
Bit 5	CLKSEL	This bit must be set when CLKIN = 12.288 MHz, and clear when CLKIN = 9.8304 MHz.
Bit 4	CPM	Call progress monitor mode. When set, the receive path can be connected to the high-band filter to detect answer tone (ALB = 0) or to the low-band filter scaled down 2.5 times (ALB = 1) to listen for the call progress tones during auto dialing.
Bit 3	ALB	Auto loopback mode. When set and CPM = 0, the transmitter output (TXA) is connected to the receive path, bypassing the receive filter.
Bit 2	TL2	Transmit level adjust bit based on Table 10.
Bit 1	TL1	Transmit level adjust bit based on Table 10.
Bit 0	TL0	Transmit level adjust bit based on Table 10.

TABLE 10. TRANSMIT LEVEL SELECTION BITS

TL2	TL1	TL0	Transmit Level at TXA Pin
0	0	0	0 dBm
0	0	1	-2 dBm
0	1	0	-4 dBm
0	1	1	-6 dBm
1	0	0	-8 dBm
1	0	1	-10 dBm
1	1	0	-12 dBm
1	1	1	-14 dBm

TABLE 11. TONE REGISTER: ADDRESS (A4-A1) = 1011

Bit Number	Bit Name	Description
Bit 7	Unused	
Bit 6	HNDSHK	This bit is set only during handshaking sequence. When set, both FSK and PSK/QAM demodulators are enabled. When cleared, the FSK demodulator is disabled when in high speed mode.
Bit 5	TONEON	When set, the output of the tone generator appears at TXA. When cleared, the output of the tone generator is squelched.
Bit 4	DTMF	When set and TONEON = 1, the DTMF generator is turned on. When cleared, the DTMF generator is turned off but other tones can be generated.
Bit 3-0	D3-D0	Specify the desired tone (see Table 12).

TABLE 12. TONE GENERATION DATA BITS

DTMF	D3	D2	D1	D0	Digit Dialed	Tone Output Frequencies (Hz)
1	0	0	0	0	0	941/1336
1	0	0	0	1	1	697/1209
1	0	0	1	0	2	697/1336
1	0	0	1	1	3	697/1477
1	0	1	0	0	4	770/1209
1	0	1	0	1	5	770/1336
1	0	1	1	0	6	770/1477
1	0	1	1	1	7	852/1477
1	1	0	0	0	8	852/1477
1	1	0	0	1	9	852/1477
1	1	0	1	0	*	941/1477
1	1	0	1	1	(A)	697/1477
1	1	1	0	0	(B)	770/1477
1	1	1	0	1	(C)	852/1477
1	1	1	1	0	#	941/1477
1	1	1	1	1	(D)	941/1477
0	0	0	0	0	No Tone; Tone Generator Turned Off	
0	0	0	0	1		550
0	0	0	1	0		1800
0	0	0	1	1		2100
0	0	1	0	0		1300
0	0	1	0	1	No Tone; Tone Generator Turned Off	
0	0	1	1	X	No Tone; Tone Generator Turned Off	
0	1	X	X	X	No Tone; Tone Generator Turned Off	

TABLE 13. PROGRAMMABLE GAIN CONTROL REGISTER (PGCR): ADDRESS (A4-A1) = 1100

Bit Number	Bit Name	Description
Bit 7	Unused	
Bit 6	AGCVT	When set, prevents gain hit due to AGC's gain step. This bit must be set during the handshaking after detecting the four point constellation and before switching to 16 way decision making.
Bit 5-0	G5-G0	Control the gain of the PGC (see Table 14.)

TABLE 14. PROGRAMMABLE GAIN CONTROL BITS

G5	G4	G3	G2	G1	G0	PGC Gain (dB)
0	0	0	0	0	0	-6
0	0	0	0	0	1	-5.25
0	0	0	0	1	0	-4.5
0	0	0	1	0	0	-3
0	0	1	0	0	0	0
0	1	0	0	0	0	+6
1	0	0	0	0	0	+18
1	1	1	1	1	1	+41.25

Note: Signal level is adjusted (before entering the filter) by the internal AGC with +8 dB or 0 dB gain.

TABLE 15. DATA REGISTER: ADDRESS (A4-A1) = 1101

Bit Number	Bit Name	Description
Bit 7	Unused	
Bit 6	PLLJAM	When set, the DPLL will be reset by the next rising edge of the received baud clock. It must remain high for at least one baud period. It should be cleared by the processor to end the jamming mode. PLLFRZ overrides PLLJAM when both are enabled.
Bit 5	PLLFRZ	Phase locked loop freeze. When set, the DPLL begins to run freely regardless of the received baud clock. To re-enable the DPLL locking, the bit must be cleared by the processor. PLLFRZ overrides PLLJAM when both are enabled.
Bit 4	PLLFAS	When set, the DPLL operates in a "fast" locking mode. In this mode, the DPLL is updated every baud period in 13 μ s steps. When clear, the DPLL operates in "normal" mode and is updated once every eight baud periods in 6.5 μ s steps.
Bit 3-0	RD3-RD0	4-bit Received Data. Used only in high speed (1200 or 2400 bps) mode, they are descrambled by the processor and shifted out by the VL7C224A. Sync to async is also done by the VL7C224A, when in the asynchronous mode. RD0 is the first bit appearing on the RXD pin, followed by RD1, RD2, and RD3. In the 1200 bps mode, only RD0 and RD1 are shifted out during one baud period.

TABLE 16. AUDIO REGISTER: ADDRESS (A4-A1) = 1110

Bit Number	Bit Name	Description
Bit 7	Unused	
Bit 6	DISS	When this bit is set scrambler is disabled, when cleared it is enabled. Transmit select bits (TXSEL0-2) override this bit when in "transmit internal mode".
Bit 5	PGCZ	When set, the output of the PGC is grounded. DC offset of the demodulator can be stored and cancelled by the controller.
Bit 4-2	TEST	Test bits used for factory testing. For normal chip operation these bits must be cleared.
Bit 1	ALC1	Audio level control bit 1. Used to control audio level at SPKR pin, see Table 17.
Bit 0	ALC0	Audio level control bit 0. Used to control audio level at SPKR pin, see Table 17.

TABLE 17. AUDIO LEVEL SELECTION BITS

ALC1	ALC0	Audio Attenuation (dB)
0	0	Audio Off
0	1	12
1	0	6
1	1	0 (No Attenuation)

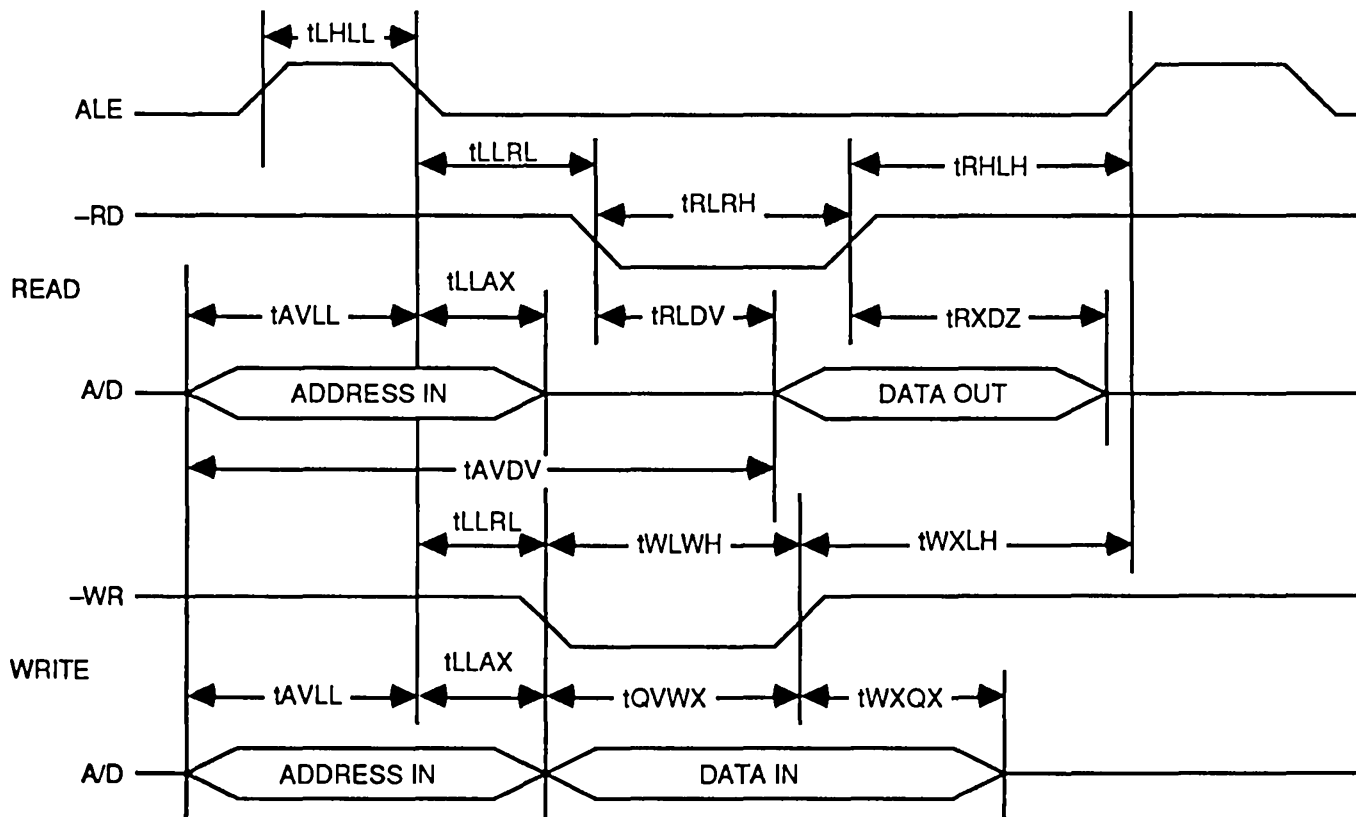
Note: The audio signal may be amplified by +8 dB by the AGC circuit.

AC CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit	Condition
tAVLL	Address Valid to end of ALE	41			ns	
tLLAX	Address Hold after end of ALE	61			ns	
tAVDV	Address Valid to Output Data Valid			336	ns	
tRLDV	–RD Active Low to Output Data Valid			194	ns	
tRXDZ	End of –RD to Output Data Hi Z			61	ns	
tLHLL	ALE Pulse Width	71			ns	
tRLRH	–RD Pulse Width	214			ns	
tWLWH	–WR Pulse Width	148			ns	
tQVWX	Data Valid to end of –WR Active	132			ns	
tWXQX	Data Hold after end of –WR	56			ns	
tLLRL	End of ALE to –RD or –WR Active	60			ns	
tRHLH	End of –RD to next ALE	55			ns	
tWXLH	End of –WR to next ALE	120			ns	
tXL	Transmit Level Measured at TXA		0		dBm	Load = 1200 Ω
				–50	dBm	TL2 = TL1 = TL0 = 0 Squelched

Note: Processor Bus Interface: see Figure 3.

FIGURE 3. BUS TIMING WAVEFORMS



SYNCHRONOUS OPERATION

Transmitter Timing

Case 1 - VL7C224A provides the timing to the Data Terminal Equipment (DTE). See Figure 4.

If the DTE can lock to an external clock, then all that needs to be done is to put the VL7C224A in the synchronous mode. This provides a 1200 Hz clock on the SCT pin that can be used as a clock source for the DTE to synchronize

its TXD to. The DTE must then synchronize its TXD to a 1200 Hz clock provided on the SCT pin. The transmit phase locked loop (TXPLL) of the VL7C224A will be in free running mode.

Case 2 - VL7C224A should lock its transmit timing to the clock source provided by the DTE.

In this case, after selecting synchronous mode, also select "locked" mode via the

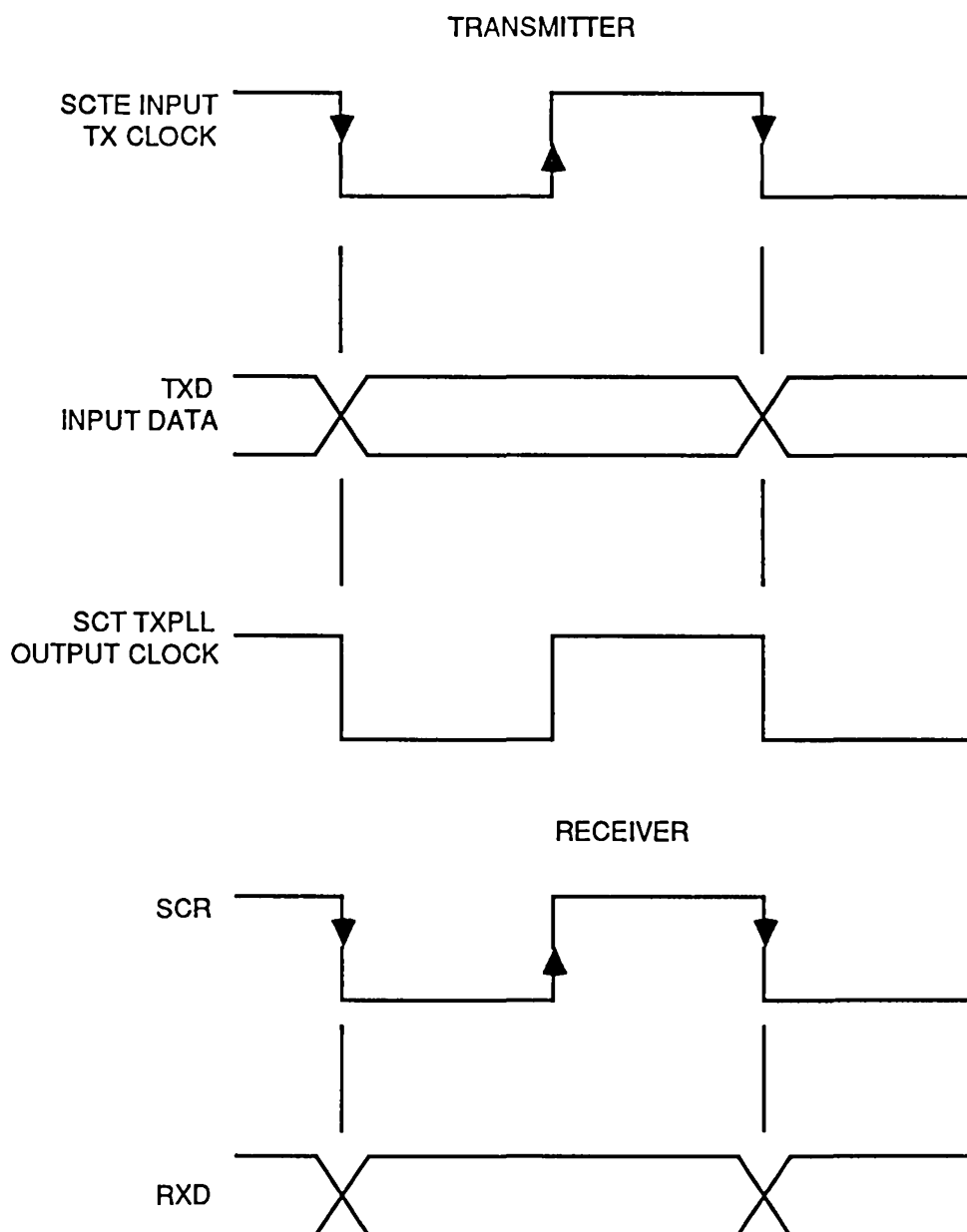
LCK bit of the MCRA register..

The VL7C224A will then synchronize itself to the clock provided on its SCTE pin.

Receiver Timing

In synchronous mode, the recovered clock will be provided on the SCR pin and the transitions of RXD will be on the falling edges of this clock as shown in Figure 4.

FIGURE 4. SYNCHRONOUS MODE CLOCK ALIGNMENT



MODEM TRANSMIT SIGNALS: ASSUME 9.8304 MHz CRYSTAL
FSK MODULATOR/DEMODULATOR FREQUENCIES: BELL 103

Parameter	Nominal	Actual	Unit	Condition
Answer Mark	2225	2226	Hz	
Answer Space	2025	2024.4	Hz	
Originate Mark	1270	1269.4	Hz	
Originate Space	1070	1070.4	Hz	

FSK MODULATOR/DEMODULATOR FREQUENCIES: CCITT V.21

Parameter	Nominal	Actual	Unit	Condition
Answer Mark	1650	1649.4	Hz	
Answer Space	1850	1850.6	Hz	
Originate Mark	980	978.34	Hz	
Originate Space	1180	1181.53	Hz	

CALL PROGRESS MONITOR MODE

Parameter	Min	Typ	Max	Unit	Condition
Center Frequency		480		Hz	ALB = 1
Detect Level (ED High) Measured at RXA	-43			dBm	
Reject Level (ED Low) Measured at RXA			-48	dBm	
Hysteresis	2			dB	
Delay Time (ED Low to High)	10	15	24	ms	EDC = 1.0 μ F
Hold Time (ED High to Low)	10	15	24	ms	EDC = 1.0 μ F

DTMF GENERATOR

Parameter	Nominal Frequency	Allowable Error	Actual Error
Row 1	697 Hz	$\pm 1\%$	-0.23%
Row 2	770 Hz	$\pm 1\%$	-0.01%
Row 3	852 Hz	$\pm 1\%$	-0.12%
Row 4	941 Hz	$\pm 1\%$	-0.39%
Column 1	1209 Hz	$\pm 1\%$	-0.35%
Column 2	1336 Hz	$\pm 1\%$	-0.93%
Column 3	1477 Hz	$\pm 1\%$	-0.48%
Guard Tones	550 Hz	± 20 Hz	-2 Hz
	1800 Hz	± 20 Hz	-2 Hz
Calling Tone	1300 Hz		-6 Hz
Answer Tone	2100 Hz		-12 Hz

MODEM TRANSMIT SIGNALS: ASSUME 9.8304 MHz CRYSTAL (Cont.)
DTMF GENERATOR

Parameter	Min	Typ	Max	Unit	Condition
Second Harmonic Distortion		-40		dB	
Row Output level		0		dBm	VCC = +5 V VSS = -5 V TL2 = TL1 = TL0 = 0 Measured at TXA Pin, 1200Ω Load
Column Output Level		2		dBm	
550 Hz Guard Tone		-3		dB (Note)	
1800 Hz Guard Tone		-6		dB (Note)	
1300 Hz Calling Tone		0		dB	
2100 Hz Answer Tone		0		dB	

Note: These levels are referenced to the TX signal level. When guard tones are added, the TXA level is automatically adjusted to maintain a constant level on the line. For 1800 Hz, the adjustment is -0.97 dB; for 550 Hz, the adjustment is -1.76 dB, per the CCITT specification.

Data Mode (Note)

Parameter	Min	Typ	Max	Unit	Condition
Energy Detect Level (ED Low to High)			-43	dBm	
Loss of Energy Detect Level (ED Low to High)	-48			dBm	
Hysteresis	2	3		dB	

Programmable Gain Controller (PGC)

Gain Step Size		0.75		dB	
Dynamic Range		47.25		dB	
Response Time (from Change In PGC Register to Output of A to D Converter)		1.0		ms	

Filter Characteristics

Crosstalk Rejection		70		dB	
Power Supply Rejection		0		dB	
DPLL Response times JAM or FRZ		20		μ s	
DPLL Response times Fast		200		μ s	

Note: EDC = 1.0 μF; measured at RXA. PGC = 0.

ABSOLUTE MAXIMUM RATINGS

Ambient Operating
Temperature 0°C to +70°C

Storage Temperature -65°C to +150°C

Positive Supply Voltage
to Ground Potential +6 V

Negative Supply Voltage
to Ground Potential -6 V

Applied Input
Voltage VSS -0.6 V to VCC +0.6 V

Power Dissipation 500 mW

Stresses above those listed may cause
permanent damage to the device.

These are stress ratings only, functional
operation of this device at these or any
other conditions above those indicated

in this data sheet is not implied.
Exposure to absolute maximum rating
conditions for extended periods may
affect device reliability.

DC CHARACTERISTICS: TA = 0°C to +70°C, VCC 5 V ±10%, VSS

Symbol	Parameter	Min	Typ	Max	Unit	Condition
ICC	Quiescent Current		18	35	mA	
ISS	Quiescent Current		18	35	mA	
VIH	High Level Input Voltage; Digital Pins	2.0			V	
VIL	Low Level Input Voltage; Digital Pins			0.8	V	
VOH	High Level Output	2.4			V	IOH = 0.5 mA
VOH	Low Level Output			0.6	V	IOL = 1.6 mA
VXTA	Maximum Peak Output Level on TXA Pin	± 3			V	VCC = + 5 V VSS = - 5 V

CLOCK CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit	Condition
FC	Clock Frequency	9.8295	9.8304	9.8313	MHz	CLKSEL = 0
		12.2868	12.2880	12.2872	MHz	CLKSEL = 1
TR, TF	Input Rise or Fall Time			500	ns	All Digital Inputs except CLKIN
TR, TF	Input Rise or Fall Time			500	ns	CLKIN

APPLICATIONS INFORMATION

WHY A MODEM/WHAT'S A MODEM

The voice frequency channels of the general switched telephone network have been used extensively for the transmission of digital data. To use these channels, the data must be put in a form that can be sent over a limited bandwidth line. In voice grade telephone networks, transformers, carrier systems and loaded lines attenuate all signals below 300 Hz and above 3400 Hz.

While the bandwidth from 300 Hz to 3400 Hz is fine for voice transmission, it is not suitable for the transmission of digital data because the data has many frequency components outside this range. To transmit data over phone lines, it is necessary to convert the digital data into a signal that is totally within the voice frequency range. This conversion is performed by a MODEM (MODulator DEModulator).

In full duplex data transmission - the simultaneous sending and receiving of data - Frequency Division Multiplexing (FDM) can be used for data rates up to 2400 bits per second. In FDM, the voice channel is divided into upper and lower bands (called the high-band and the low-band); one is used for sending and the other for receiving data. The originating terminal transmits in the low-band and receives in the high-band, while the answering terminal transmits in the high-band and receives in the low-band.

In low speed modems (300 bit per second transmission rate), the modulation technique commonly employed is called Frequency Shift Keying (FSK). In FSK modems, four separate frequencies are used; 1070 Hz for a zero (also called a space) in the low-band, 1270 Hz for a one (a mark) in the low-band, 2025 Hz for a zero in the high-band and 2225 Hz for a one in the high-band. The transmitting modem takes the digital ones and zeros from the terminal and converts them into the proper tones which are then sent over the phone line. The receiving modem takes the tones and converts them back to ones and zeros and sends them to the receiving terminal. Since four frequencies are

used, simultaneous transmitting and receiving of data can be accomplished.

Because of limited bandwidth of the phone line, FSK modems only work up to 600 bits per second for full duplex transmission. This is due to the fact that when the modem shifts between the two frequencies (for mark and space) it generates a spectrum of frequencies (it is a type of FM - frequency modulation - transmission). The faster the data rate, the wider the spectrum. The limit for full duplex FSK transmission is 600 bits per second, before the available audio spectrum is used up and allowing for enough separation between the frequency bands to reliably decode or demodulate the data. There are 1200 BPS FSK modems, but these are half duplex, they can send or receive data at 1200 bps, but not simultaneously.

In high speed, full duplex modems (1200/2400 bit per second transmission rate) a different modulation technique is employed. Called PSK (for Phase Shift Keying), this technique uses one carrier frequency for the high-band, 2400 Hz, and one for the low-band, 1200 Hz, for sending and receiving data. For each carrier frequency (one for transmitting and one for receiving), one of 16 phase and amplitude signalling levels is used. The data is sent four bits at a time, or in quadbits. Since there are 16 ways to send four bits at a time, each of the 16 signalling elements represents one unique quadbit. While the data rate is 2400 bits per second, the baud rate (the rate at which information packets are sent) is 600 because four bits are sent in each packet. Again, 600 packets per second (600 baud and, in this case, 2400 bps) is the limit for transmitting full duplex data over the general switched telephone network using FDM.

V.22 bis is a CCITT specification that specifies 2400 bit per second, full or half duplex data transmission. V.22 bis specifies a fallback mode of 1200 bps which is defined by the V.22 specification. Neither V.22 bis nor V.22 call for a 300 bps fallback; however, there is a CCITT standard for 300, V.21 and this mode is also provided by the chip set. In addition the chip set provides for Bell

212A capability for the U.S. 1200 bps and 300 bps modes of operation.

V.22 and V.22 bis also call for guard tones to be sent along with the data. In most of Europe the tone is 1800 Hz except in Sweden where 550 Hz is used. The VL7C224A has the 500 Hz and 1800 Hz tone generators built in, as well as the 550 and 1800 Hz notch filters to remove the guard tone when in the receive mode.

Power Supply Decoupling and Circuit Layout Consideration

For optimum performance and to obtain the best possible performance at low received signal levels with low s/n ratio, it is important to use the recommended power supply decoupling circuit as shown in Figure 5.

Small inductors in series with the positive and negative supplies help suppress RFI as well as improve the power supply noise rejection capability of the VL7C224A when used with the decoupling capacitors. The 10 μ F capacitors should be tantalum type while the 0.1 μ F capacitors should have a good high frequency rejection characteristic, monolithic ceramic types are recommended.

It is important to locate the decoupling capacitors as close to the actual power supply pins of the VL7C224A as possible. It is also recommended that the analog ground and digital ground buses be routed separately and connected at the common ground point of the power supply.

VL7C224A and DAA

As shown in Figure 5 the only external components required by the VL7C224A, U1, for its operation are the 600 Ω line matching resistor and a 1.0 μ F capacitor from the EDC pin to ground. If it is desired to drive a speaker to monitor the line, an external amplifier can be added, but the output provided on the VL7C224A can directly drive a high impedance (50 k Ω) earphone-type transducer. In Figure 5, U15 provides this amplifier. R12 will provide control of the maximum output level to the speaker. Note that the VL7C224A has an internal attenuator which allows software control of the audio level also.

All modems require a DAA. A DAA (data access arrangement) is a piece of equipment required by the FCC to connect anything to the general switched telephone network. In Figure 5, it consists of an isolation transformer, typically 600 Ω to 600 Ω (T1); a relay for disconnecting the modem from the line (K1); a ring detector, typically an opto-isolator (U15); and high voltage surge protectors (VS1). Relay K1 also provides a means to pulse dial if that mode is desired. Tone dialling capability is provided internally in the VL7C224A. Also required is a hybrid function which separates the transmit and receive signals from the combined signal on the two wire telephone line. This function is provided internally to the VL7C224A although an external hybrid may be constructed (refer to previous section of this data sheet for more information). Diodes CR5 to CR8 provide a clamp to limit the maximum signal applied to the VL7C224A. The other relay in Figure 5, K2, and its related circuitry is normally used to control a telephone set connected to the modem. This circuitry is optional. The DAA must be FCC registered and this can be done by any of many consultants and labs around the country. Another alternative is to buy a certified DAA, supplied by several manufacturers.

Two jumper selected options are shown in Figure 5. J1 is connected if an external synchronous transmit clock source is to be used. J2 has three positions and controls the receiver gain of the VL7C224A to compensate for any transformer losses in T1: unconnected, no gain adjustment; to + 5 V, gain will be increased by + 3 dB; if tied to ground, gain will be increased + 2 dB.

Also shown in Figure 5 is an optional 128 byte EEPROM, U13, which can be used by the modem controller for

storing configuration data and telephone numbers when the modem is turned off.

CONTROLLER OPTIONS

The VL7C224A is usually used with some form of controller. The controller does the tasks of programming the various modes of the VL7C224A and provides the equalization and PSK/QAM detection as well as controlling the handshaking sequences required for connection establishment. Usually a command language is used to communicate with the modem controller from external systems and this must be included in the controller functions also. A well established standard for this command language is the 'AT' command set used by Hayes in their modem products.

Three controllers are available which provide all these capabilities as well as providing a built-in UART function: the VL7C225, VL7C235, and VL7C245 Modem Advanced Coprocessors. The VL7C225 is the core device of this family and utilizes external EPROM or ROM for its program memory. It is also capable of using external RAM for temporary data storage. The VL7C225 is capable of being used either in stand-alone serial modem applications or in bus-oriented applications, such as the IBM PC. The pin functions of the device may be reconfigured by the firmware to either application. Figure 6 shows the VL7C225, U2, in a circuit which is applicable to either application. U3 provides the external program memory. A parallel resonant crystal, Y1, is used by the VL7C225 to generate its clocks. The specifications of this crystal are very important: 19,6608 MHz \pm .001%, parallel resonant with an 18 pF load capacitance (Saronix NP196-18). Also shown in Figure 6 is an optional bus buffer for the AD0-AD7 bus, U5.

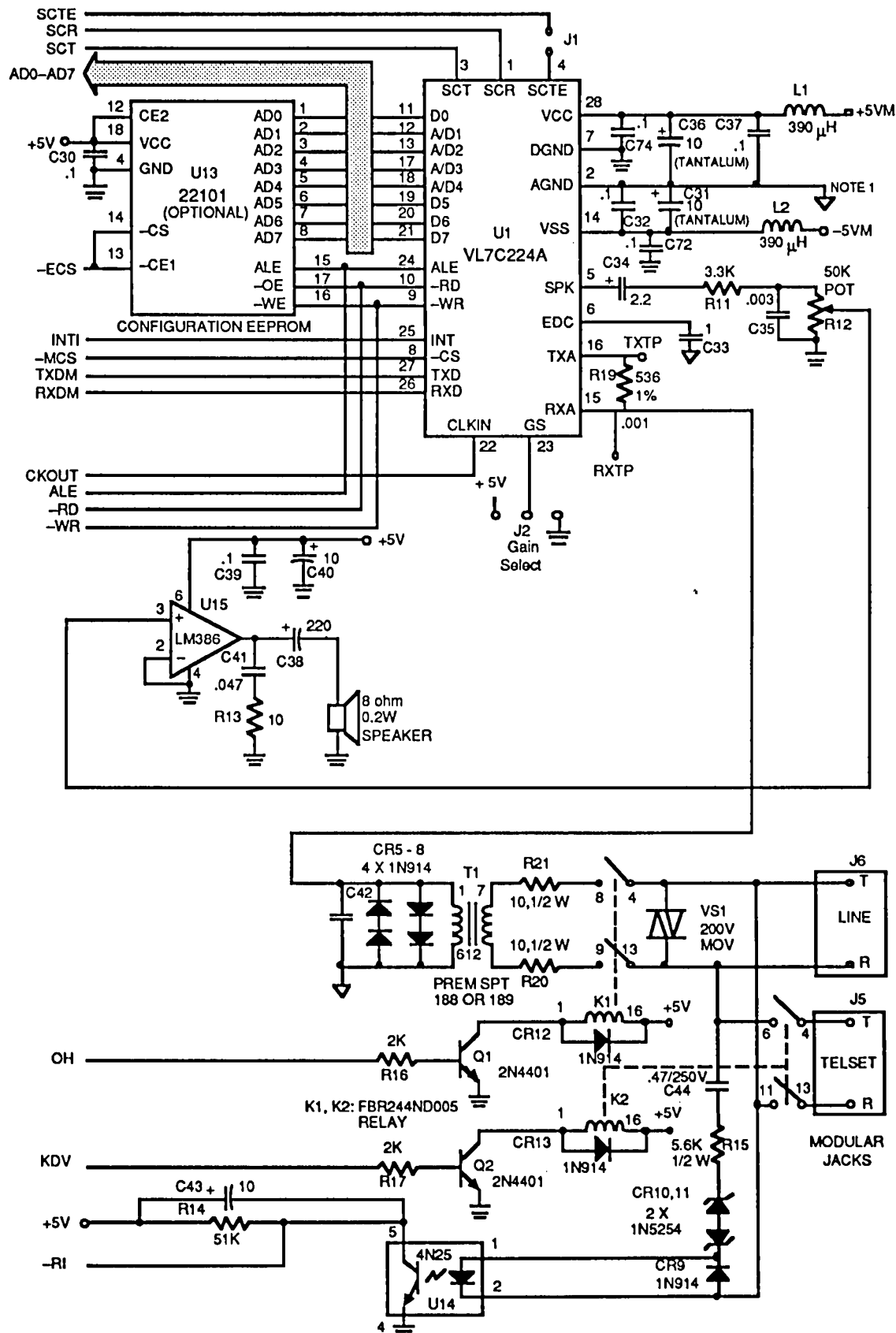
While not required for proper operation, this buffer improves the signal to noise performance of the modem. A future version of the VL7C224A is planned which will incorporate this buffer, at which time U5 may be omitted or bridged. Since the VL7C225 may be used for either serial or bus applications, designations for the signals may have dual names.

If a serial stand-alone modem is desired, Figures 5 and 6 may be combined with Figures 7 and 8 to form a complete modem. Figure 7 illustrates the circuitry required for the RS-232 interface, indicator LEDs, and optional configuration switches which may be read by the controller at power-up to set configuration defaults. Figure 8 provides a power supply circuit for converting the output of a 12 volt ac wall transformer into the voltages required by the rest of the circuitry.

Figure 7 may be combined with Figures 1 and 2 to form a IBM PC compatible plug-in modem card. U4 provides bus buffering, while U5 provides address decoding. Two I/O address options are provided: COM1 and COM2. In addition, either IRQ3 or IRQ4 may be selected by the appropriate jumpers.

Two other controllers are offered that use internal ROM for the program memory. This eliminates the need for an external EPROM. Figure 10 shows the VL7C245 which is intended for stand-alone applications. The VL7C235 is used for bus oriented applications and is shown in Figure 11. Both controllers contain the Hayes compatible 'AT' command set. These controllers can be substituted in Figure 6 for U2 and U3.

FIGURE 5. COMMON MODEM CIRCUITRY



Unless otherwise noted, resistance is given in ohms, capacitance in microfarads.

Note 1: Connect analog ground directly to common of the power supply filter capacitor.

FIGURE 6. MODEM CONTROLLER

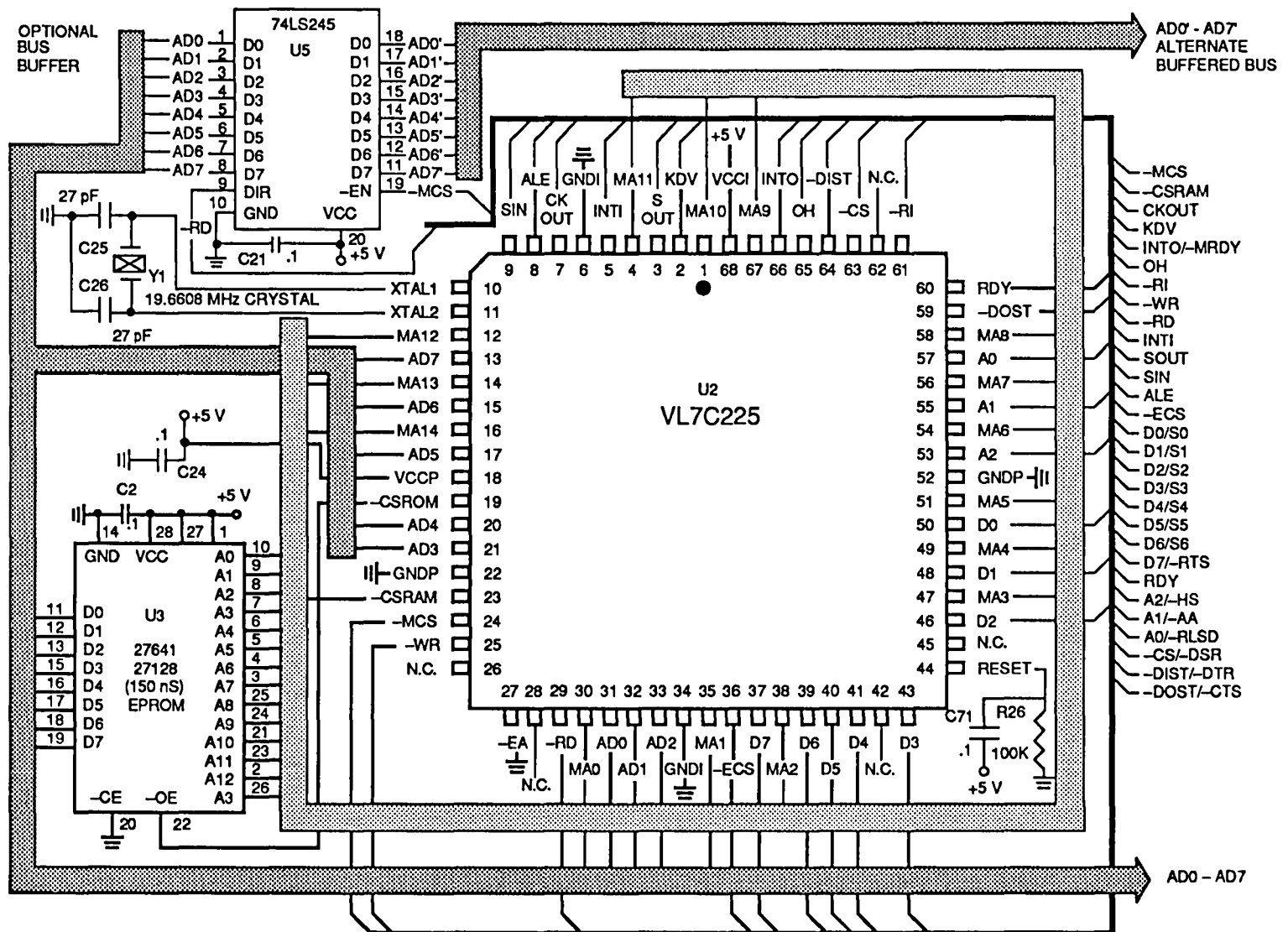


FIGURE 7. RS232 AND LED INTERFACE FOR STAND-ALONE MODEM

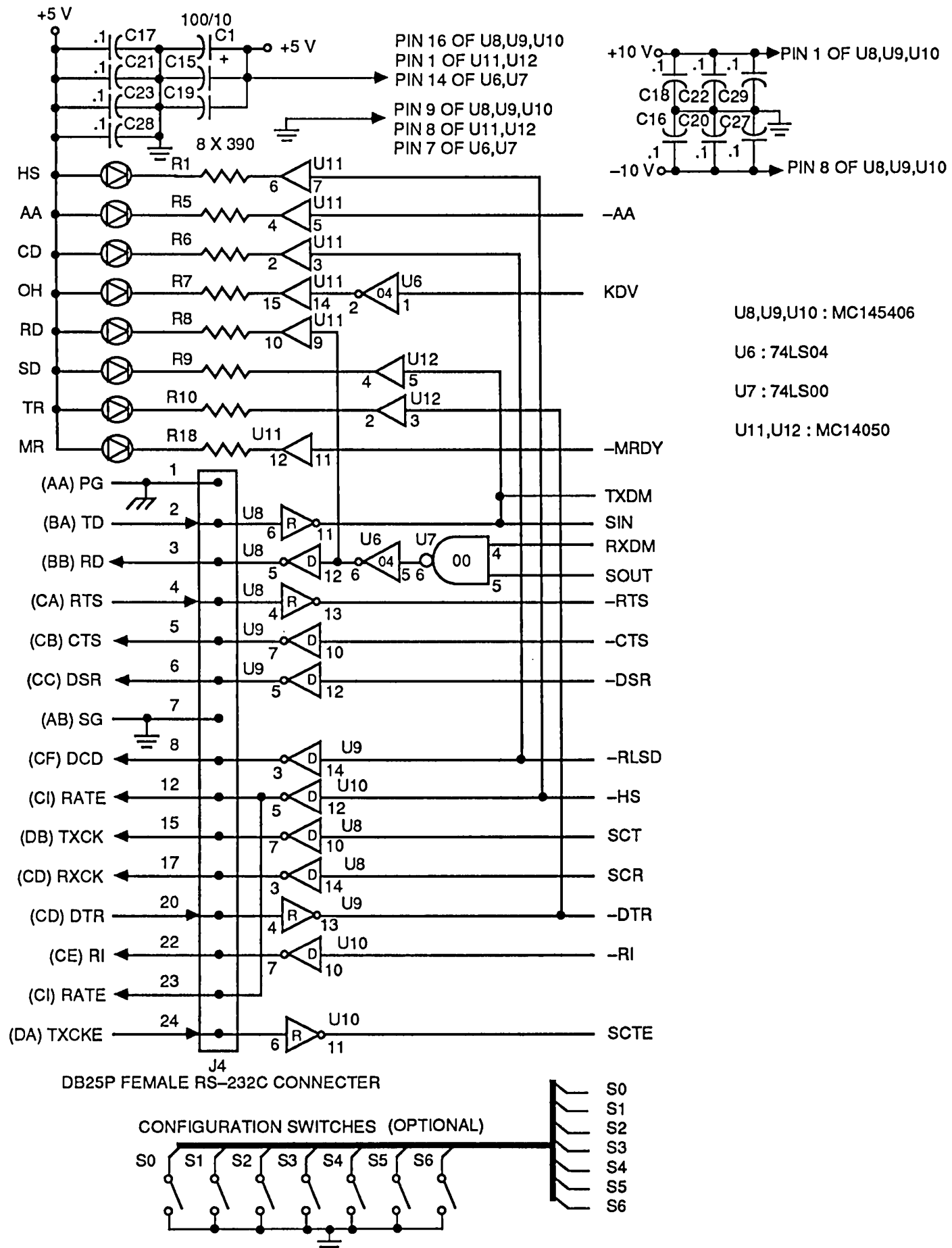


FIGURE 8. POWER SUPPLY FOR STAND-ALONE MODEM

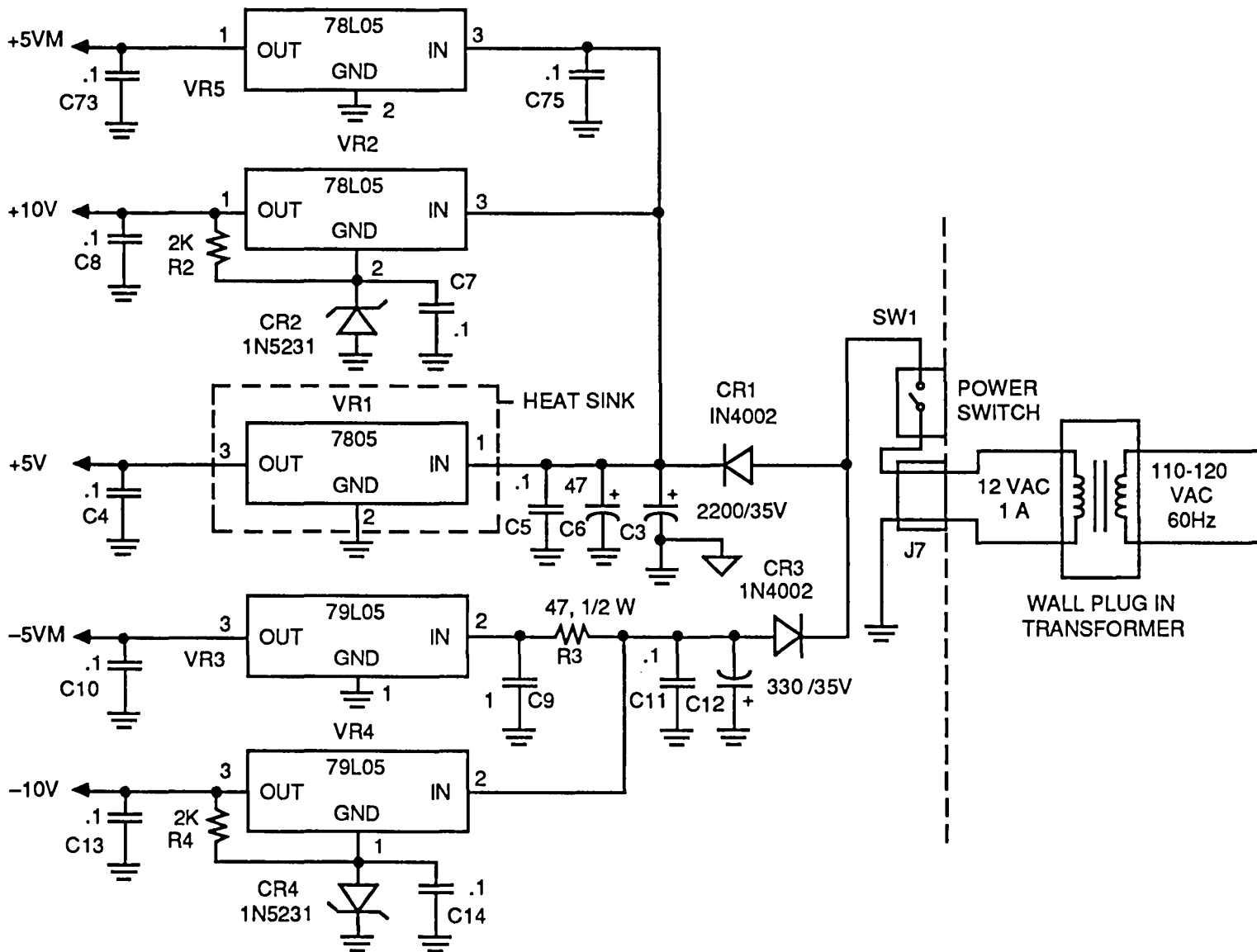


FIGURE 9. INTERFACE FOR PC BUS MODEM

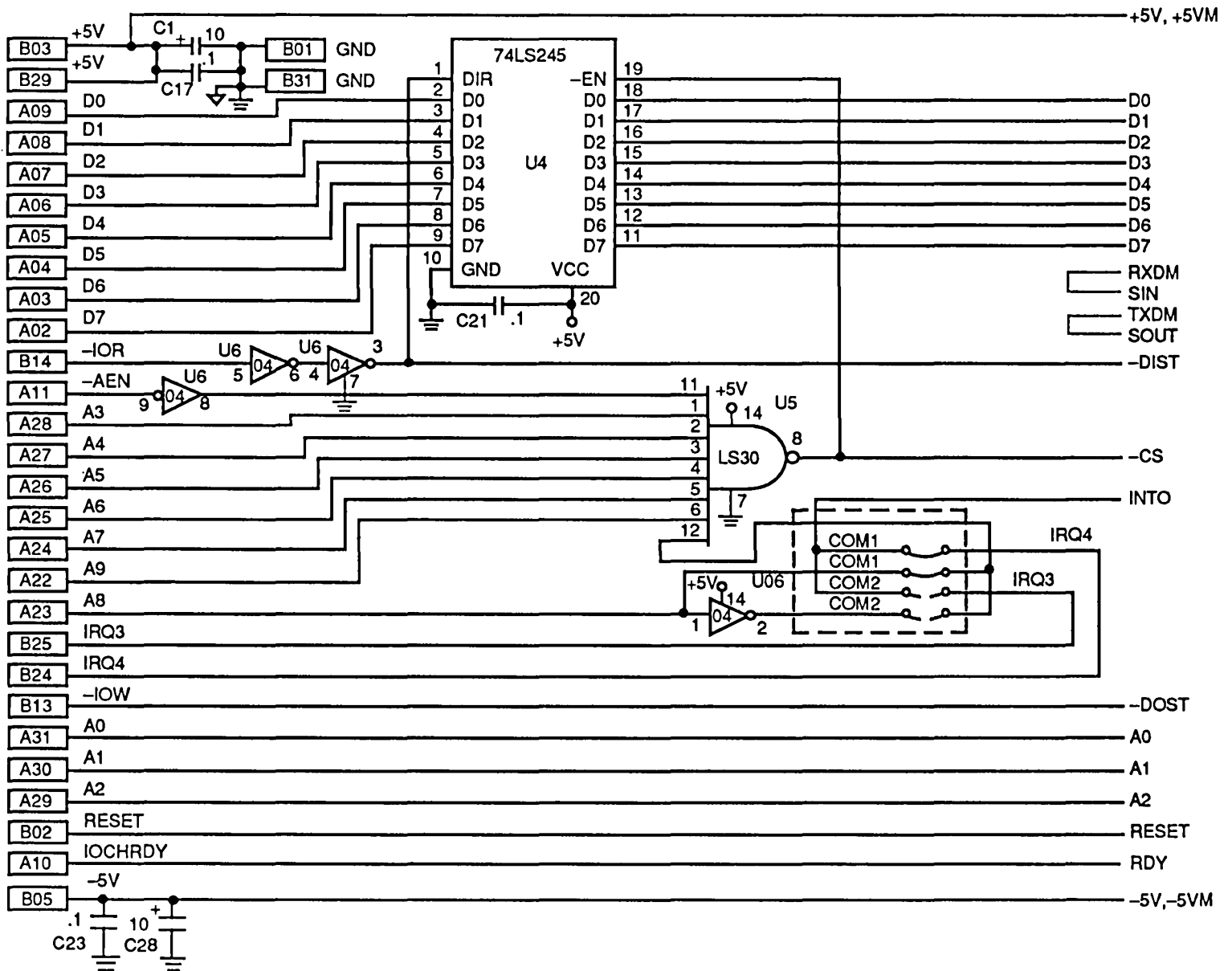


FIGURE 10. ALTERNATE STAND-ALONE MODEM CONTROLLER

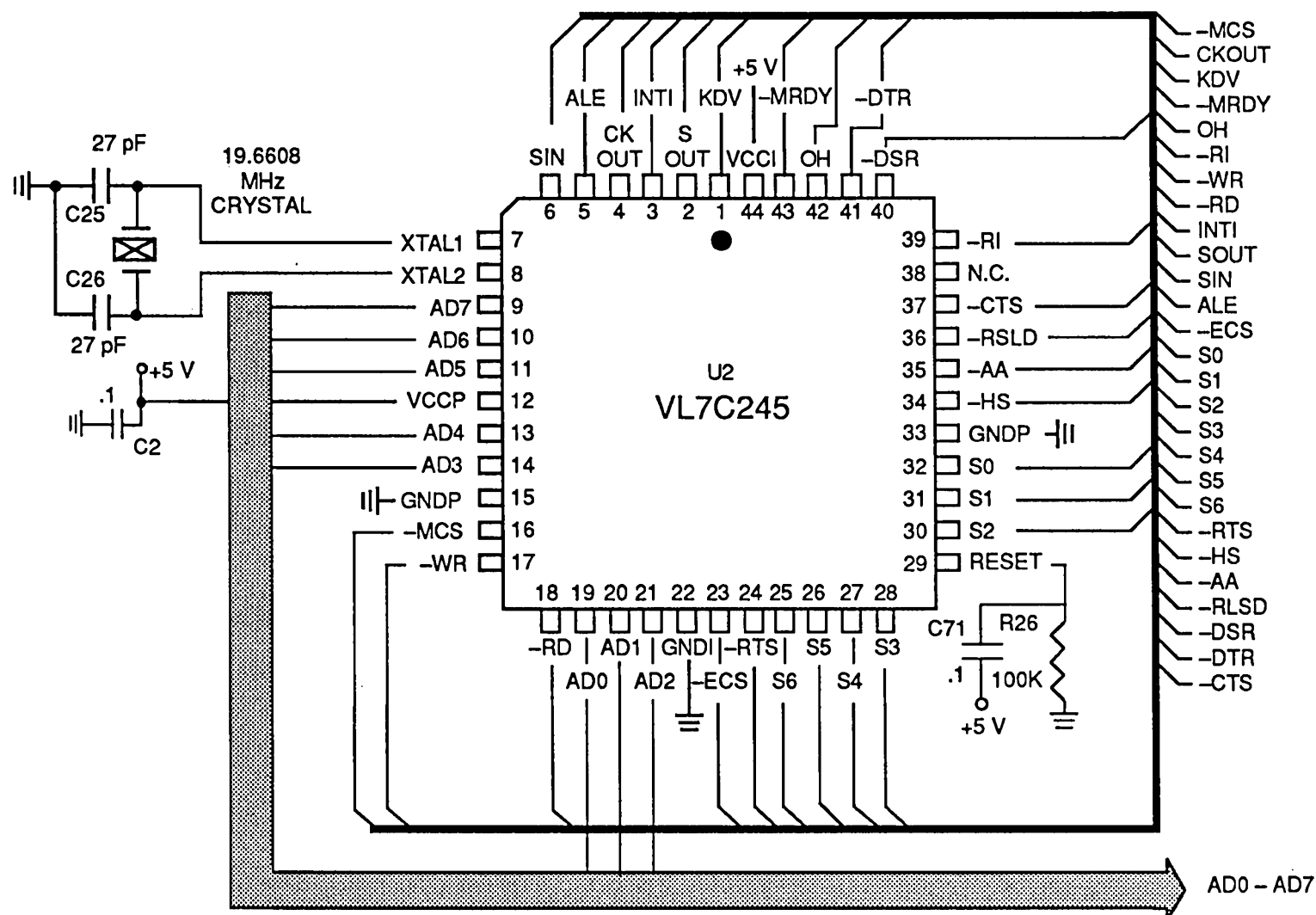
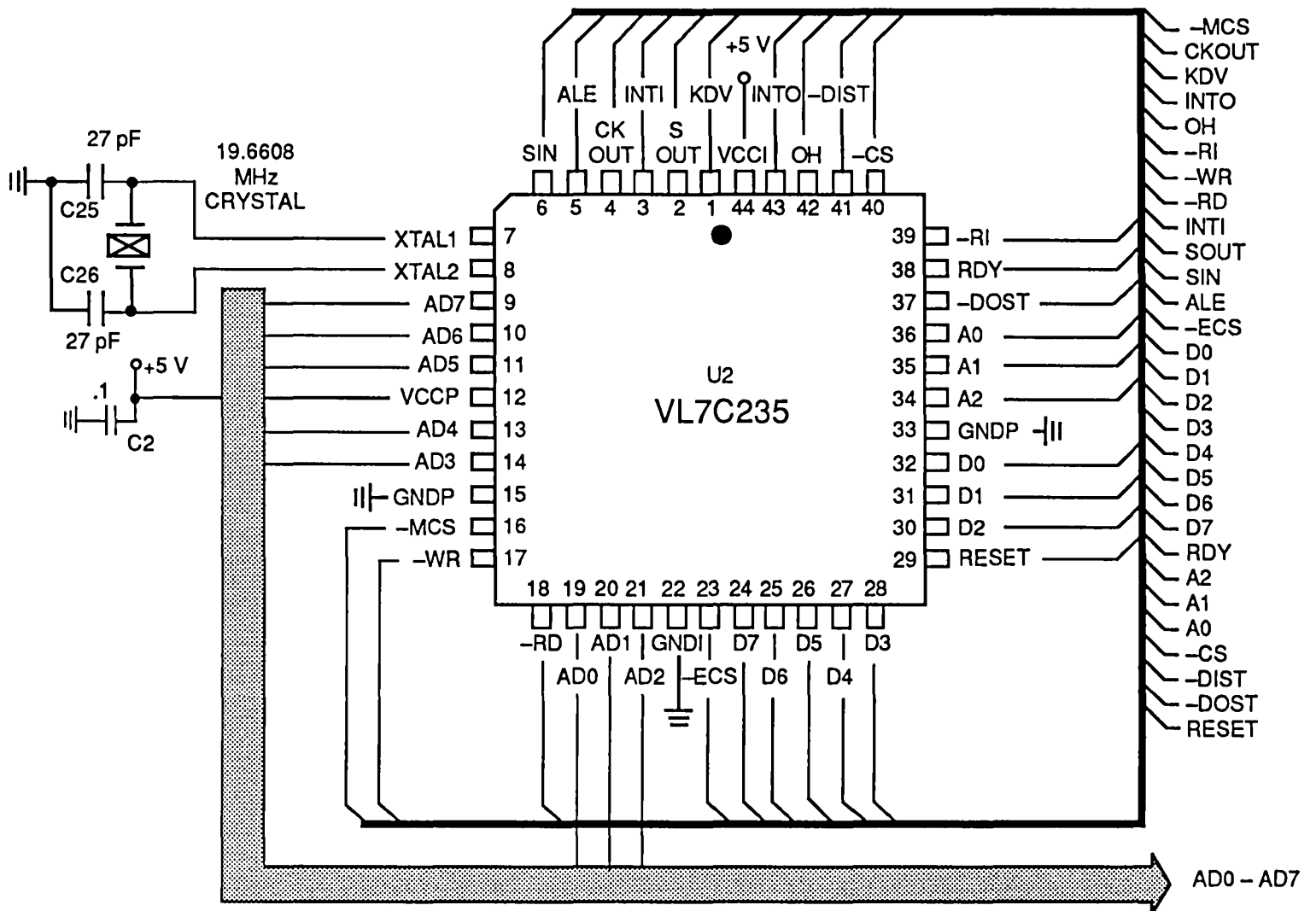


FIGURE 11. ALTERNATE PC BUS MODEM CONTROLLER



VL7C225 • VL7C235 • VL7C245

2400 BIT-PER-SECOND MODEM ADVANCED COPROCESSOR FAMILY

FEATURES

- Direct interface to the VL7C224A single-chip modem
- Complete "AT" command set in firmware
- Built-in 82C50B UART equivalent
- Direct IBM PC bus interface
- External ROM/RAM addressable
- Two-micron CMOS technology
- 2400 bps intelligent modem using just two chips
- Compatible with industry standard software
- No external buffers required

DESCRIPTION

The VL7C225 family are specialized controllers that interface directly to the VL7C224A Modem to form a 2400 bps full duplex intelligent modem. The two-chip set performs all the modem functions as well as automatic control features compatible to the Hayes "AT" Command Set. The chip set is compatible to the CCITT V.22 BIS with V.22 fallback, Bell 212A with 103 fallback, as well as the V.21 standard.

The VL7C235 interfaces to a parallel system bus, such as the bus in the IBM PC, while the VL7C245 interfaces to an RS232 port.

The controller receives 8-bit signal samples from the VL7C224A and performs adaptive equalization, Carrier

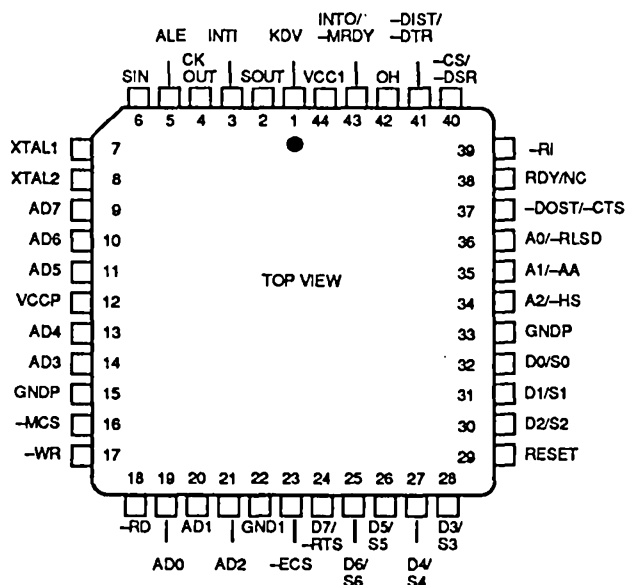
phase recovery, data decode, and de-scrambling.

The VL7C225, VL7C235, and VL7C245 have identical hardware. However, they can be configured as a parallel (VL7C235), or serial (VL7C245) device by programming the internal ROM. The VL7C225 is the ROM-less version and is available in a 68-pin PLCC package. It is intended for use with external memory to accommodate customized firmware.

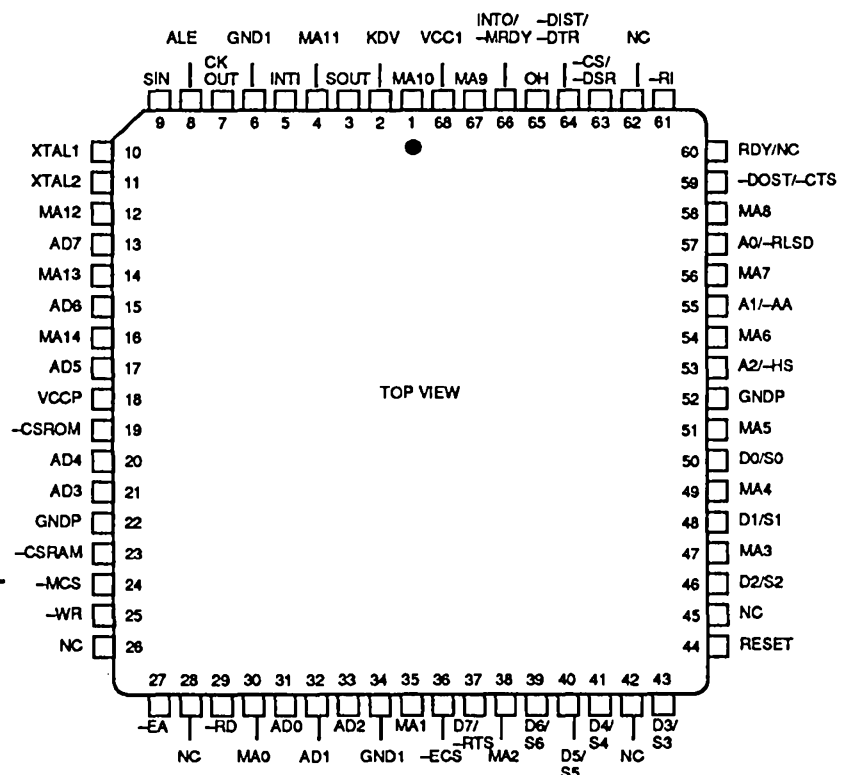
These controllers use a bit slice core processor to perform digital signal processing (DSP) and the control function. Its instruction set is a fast subset of the 8096 instruction set.

PIN DIAGRAMS

**VL7C235-QC
VL7C245-QC**



VL7C225-QC



ORDER INFORMATION

Part Number	Package
VL7C235-PC	Plastic DIP
VL7C235-QC	Plastic Leaded Chip Carrier (PLCC)
VL7C245-PC	Plastic DIP
VL7C245-QC	Plastic Leaded Chip Carrier (PLCC)
VL7C225-QC	Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range is 0°C to +70°C.

VL7C225 SIGNAL DESCRIPTIONS (68 PINS - PARALLEL)

Signal Name	Pin Number	Signal Type	Signal Description
KDV	2	O	This output controls the operation of the data/voice relay. When low, the data/voice relay is off and the phone line is connected to the phone set. during a data call, the VL7C225 makes this output high to operate the data/voice relay, disconnecting the phone set from the phone line. It may also be used to drive a relay for multi-line phone applications to close the A and A1 leads. (See Note.)
SOUT	3	O	This pin is a serial data output pin. During a data call, after the connection is established, the VL7C225 converts parallel data received from the computer bus and outputs it in a serial format to the VL7C224A modem for modulation. At all other times the VL7C225 holds this output in the Mark (high) condition.
INTI	5	I	Interrupt Input - Received from the VL7C224A at 600 Hz. Interrupt is detected when this pin has a low to high transition. This signal must stay high for at least 200 nsec.
GNDI	6, 34		Ground.
CKOUT	7	O	Clock Output pin - 9.8304 MHz.
ALE	8	O	Address Latch Enable - The address on AD0-AD7 is valid at the falling edge of this normally low signal.
SIN	9	I	Received serial data . FSK data from the VL7C224A is input on this pin.
XTAL1	10	I	Used with XTAL2 for crystal (19.6608 MHz).
XTAL2	11	O	Crystal output pin (19.6608 MHz).
VCCP	18		Positive supply (+5 V).
-CSROM	19	O	Chip Select for external ROM - Active for addresses from 8000H to FFFFH.
GNDP	22, 52		Ground.
-CSRAM	23	O	Chip Select for external RAM - Active for addresses from 4000H to 7FFFH.
-MCS	24	O	Chip Select for VL7C224A - Active for addressing from 1000H to 10FFH.
-WR	25	O	Write enable - Data on AD0-AD7 is valid at the rising edge of this signal.
-EA	27	I	External Access enable - A high on this pin will cause the chip to use internal ROM. When this pin is low the chip will use external program memory.
-RD	29	O	Read enable - Data on AD0-AD7 must be valid at the rising edge of this signal.
-ECS	36	O	External EEPROM Chip Select - Active for addressing space from 1100H to 11FFH.
RESET	44	I	Master Reset - Schmitt-trigger input. A high will cause the VL7C225 to reset.
A0-A2	57, 55, 53	I	These three address inputs are used during read or write operation to select an internal UART register in the VL7C225 as shown in Table 2. The Divisor Latch Access Bit (DLAB) must be set high by the system software to access the bit rate divisor latches as shown in Table 2. (See Note.)

Note: The use of these pins is determined by the external program. Typical designations for parallel and serial applications are given in the above pin descriptions

VL7C225 SIGNAL DESCRIPTIONS (68 PINS - PARALLEL - CONT.)

Signal Name	Pin Number	Signal Type	Signal Description
-DOST	59	I	The system bus can write data or control words into a selected register of the internal UART when -DOST is low and the chip is selected. Data is latched on the rising edge of the signal. (See Note.)
RDY	60	O	This open-drain output will go low upon a write or read operation on D0-D7, and remain low until internal data setup and hold times have been satisfied.
-RI	61	I	The output of the ring detector in the DAA is connected to this input. A low level on this input indicates the "On" duration of the ring cycle. This is a Schmitt-trigger input, allowing for slow rising and falling signals on this pin. (See Note.)
-CS	63	I	The VL7C225 is selected when this input is low. When high, the VL7C225 forces the data bus lines, D0-D7, into a high impedance state.
-DIST	64	I	The system CPU can read data or status information from a selected register of the internal UART when -DIST is low and the chip is selected. (See Note.)
OH	65	O	This output controls the operation of the hookswitch relay in the DAA. During a data call, this output is high. It operates the hookswitch relay which causes the phone line to be seized. During rotary dialing, the VL7C225 pulses this output at a rate of ten pulses per second with appropriate Mark/Space ratio depending on mode. (See Note.)
INTO	66	O	This output goes high whenever any one of the following interrupt types has an active condition and is enabled via the IER of the internal UART: Receiver Line Status flag, Received Data Available, Transmitter Holding Register Empty, and Modem Status. It is reset low upon the appropriate interrupt servicing. The INTO pin is forced to a high impedance state when the OUT2 bit of the Modem Control Register (MCR) is low (power on state). (See Note.)
VCCP	68		Positive supply (+5 V).
NC	26, 28, 42 45, 62		No Connect.
MA0-MA14	30, 35, 38, 47, 49, 51, 54, 56, 58, 67, 1, 4, 12, 14, 16	O	15 bit address bus for external program/data access.
AD0-AD7	31-33, 21 20, 17, 15, 13	I/O	8-bit bidirectional multiplexed address/data bus for addresses from 1000H to 11FFH. Also serves as a bidirectional data bus for external program memory.
D0-D7	50, 48, 46	I/O	This is the 8-bit data bus comprising of three-state input/output lines. This bus provides bidirectional communication between the VL7C225 and the system CPU. Data control words and status information are transferred via the D0-D7 data bus.

Note: The use of these pins is determined by the external program. Typical designations for parallel and serial applications are given in the above pin descriptions



VL7C225 SIGNAL DESCRIPTIONS (68 PINS - SERIAL)

Signal Name	Pin Number	Signal Type	Signal Description
KDV	2	O	This output controls the operation of the data/voice relay. When low, the data/voice relay is off and the phone line is connected to the phone set. during a data call, the VL7C225 makes this output high to operate the data/voice relay, disconnecting the phone set from the phone line. It may also be used to drive a relay for multi-line phone applications to close the A and A1 leads. (See Note.)
SOUT	3	O	This pin is a serial data output pin. The VL7C225 converts parallel data received from the VL7C224A or internally generated and outputs it in a serial format to the RS232 interface. At all other times the VL7C225 holds this output in the Mark (high) condition.
INTI	5	I	Interrupt Input - Received from the VL7C224A at 600 Hz. Interrupt is detected when this pin has a low to high transition. This signal must stay high for at least 200 nsec.
GNDI	6, 34		Ground.
CKOUT	7	O	Clock Output pin - 9.8304 MHz.
ALE	8	O	Address Latch Enable - The address on AD0-AD7 is valid at the falling edge of this normally low signal.
SIN	9	I	Received serial data . Data from the RS232 interface is input on this pin.
XTAL1	10	I	Used with XTAL2 for crystal (19.6608 MHz).
XTAL2	11	O	Crystal output pin (19.6608 MHz).
VCCP	18		Positive supply (+5 V).
-CSROM	19	O	Chip Select for external ROM - Active for addresses from 8000H to FFFFH.
GNDP	22, 52		Ground.
-CSRAM	23	O	Chip Select for external RAM - Active for addresses from 4000H to 7FFFH.
-MCS	24	O	Chip Select for VL7C224A - Active for addressing from 1000H to 10FFH.
-WR	25	O	Write enable - Data on AD0-AD7 is valid at the rising edge of this signal.
-EA	27	I	External Access enable - A high on this pin will cause the chip to use internal ROM. When this pin is low the chip will use external program memory.
-RD	29	O	Read enable - Data on AD0-AD7 must be valid at the rising edge of this signal.
-ECS	36	O	External EEPROM Chip Select - Active for addressing space from 1100H to 11FFH.
-RTS	37	I	Request to Send - Input from RS232 interface. (See Note.)
RESET	44	I	Master Reset - Schmitt-trigger input. A high will cause the VL7C225 to reset.

Note: The use of these pins is determined by the external program. Typical designations for parallel and serial applications are given in the above pin descriptions

VL7C225 SIGNAL DESCRIPTIONS (68 PINS -SERIAL - CONT.)

Signal Name	Pin Number	Signal Type	Signal Description
-HS	53	O	This output, when low, indicates that the modem is in the high speed (2400 bps) mode. When high, it indicates that it is in the low speed modes. (See Note.)
-AA	5	O	This output is low when the VL7C225 is set for auto-answer mode. The output goes high during each ring. If the device is not set to answer the phone, this output goes low each time the phone rings. (See Note.)
-RLSD	57	O	This output goes low when the VL7C225 detects a carrier signal from the remote modem. If the connection is broken or never established, it remains high. (See Note.)
-CTS	59	O	This output goes low to indicate the modem is ready to receive data from the RS232 interface. (See Note.)
-RI	61	I	The output of the ring detector in the DAA is connected to this input. A low level on this input indicates the "On" duration of the ring cycle. This is a Schmitt-trigger input, allowing for slow rising and falling signals on this pin. (See Note.)
-DSR	63	O	This output indicates the status of the modem. Normally connected to the RS232 interface. (See Note.)
-DTR	64	I	This input from the RS232 interface may be used to control the status of the modem. (See Note.)
OH	65	O	This output controls the operation of the hookswitch relay in the DAA. During a data call, this output is high. It operates the hookswitch relay which causes the phone line to be seized. During rotary dialing, the VL7C225 pulses this output at a rate of ten pulses per second with appropriate Mark/Space ratio depending on mode. (See Note.)
-MRDY	66	O	This output goes low when the mode is ready for operation. (An LED indicator is normally driven by this pin.) (See Note.)
VCCP	68		Positive supply (+5 V).
N.C.	26, 28, 42, 45, 60, 62		No Connect.
MA0-MA14	30, 35, 38, 47, 49, 51, 54, 56, 58, 67, 1, 4, 12, 14, 16	O	15 bit address bus for external program/data access.
AD0-AD7	31-33, 2, 20, 17, 15, 13	I/O	8-bit bidirectional multiplexed address/data bus for addresses from 1000H to 11FFH.
S0-S6	50, 48, 46, 43, 41, 40, 39	I	7-bit input port for sensing switch settings.

Note: The use of these pins is determined by the external program. Typical designations for parallel and serial applications are given in the above pin descriptions



VL7C235 SIGNAL DESCRIPTIONS (44 PINS)

Signal Name	Pin Number	Signal Type	Signal Description
KDV	1	O	This output controls the operation of the data/voice relay. When low, the data/voice relay is off and the phone line is connected to the phone set. during a data call, the VL7C235 makes this output high to operate the data/voice relay, disconnecting the phone set from the phone line. It may also be used to drive a relay for multi-line phone applications to close the A and A1 leads.
SOUT	2	O	This pin is a serial data output pin. During a data call, after the connection is established, the VL7C235 converts parallel data received from the computer bus and outputs it in a serial format to the VL7C224A modem for modulation. At all other times the VL7C235 holds this output in the Mark (high) condition.
INTI	3	I	Interrupt Input - Received from the VL7C224A at 600 Hz. Interrupt is detected when this pin has a low to high transition. This signal must stay high for at least 200 nsec.
CKOUT	4	O	Clock Output pin - 9.8304 MHz.
ALE	5	O	Address Latch Enable - The address on AD0-AD7 is valid at the falling edge of this normally low signal.
SIN	6	I	Received serial data . FSK data from the VL7C224A is input on this pin.
XTAL1	7	I	Used with XTAL2 for crystal (19.6608 MHz).
XTAL2	8	O	Crystal output pin (19.6608 MHz).
VCCP	12		Positive supply (+5 V).
GNDP	15, 33		Ground.
-MCS	16	O	Chip Select for VL7C224A - Active for addressing from 1000H to 10FFH.
-WR	17	O	Write enable - Data on AD0-AD7 is valid at the rising edge of this signal.
-RD	18	O	Read enable - Data on AD0-AD7 must be valid at the rising edge of this signal.
GNDI	22		Ground.
-ECS	23	O	External EEPROM Chip Select - Active for addressing space from 1100H to 11FFH.
RESET	29	I	Master Reset - Schmitt-trigger input. A high will cause the VL7C235 to reset.
A0-A2	36, 35, 34	I	These three address inputs are used during read or write operation to select an internal UART register in the VL7C235 as shown in Table 2. The Divisor Latch Access Bit (DLAB) must be set high by the system software to access the bit rate divisor latches as shown in Table 2.
-DOST	37	I	The system bus can write data or control words into a selected register of the internal UART when -DOST is low and the chip is selected. Data is latched on the rising edge of the signal.
RDY	38	O	This open-drain output will go low upon a write or read operation on D0-D7, and remain low until internal data setup and hold times have been satisfied.

VL7C235 SIGNAL DESCRIPTIONS (44 PINS - CONT.)

Signal Name	Pin Number	Signal Type	Signal Description
-RI	39	I	The output of the ring detector in the DAA is connected to this input. A low level on this input indicates the "On" duration of the ring cycle. This is a Schmitt-trigger input, allowing for slow rising and falling signals on this pin.
-CS	40	I	The VL7C235 is selected when this input is low. When high, the VL7C235 forces the data bus lines, D0-D7, into a high impedance state.
-DIST	41	I	The system CPU can read data or status information from a selected register of the internal UART when -DIST is low and the chip is selected.
OH	42	O	This output controls the operation of the hookswitch relay in the DAA. During a data call, this output is high. It operates the hookswitch relay which causes the phone line to be seized. During rotary dialing, the VL7C235 pulses this output at a rate of ten pulses per second with appropriate Mark/Space ratio depending on mode.
INTO	43	O	This output goes high whenever any one of the following interrupt types has an active condition and is enabled via the IER of the internal UART: Receiver Line Status flag, Received Data Available, Transmitter Holding Register Empty, and Modem Status. It is reset low upon the appropriate interrupt servicing. The INTO pin is forced to a high impedance state when the OUT2 bit of the Modem Control Register (MCR) is low (power on state).
VCCI	44		Positive supply (+5 V).
AD0-AD7	19, 20, 21, 14, 13, 11, 10, 9	I/O	8-bit bidirectional multiplexed address/data bus for addresses from 1000H to 11FFH. Also serves as bidirectional data bus for external program memory.
D0-D6	32, 31, 30, 28, 27, 26, 25, 24	I/O	This is the 8-bit data bus comprising of three-state input/output lines. This bus provides bidirectional communication between the VL7C235 and the system CPU. Data control words and status information are transferred via the D0-D7 data bus.

VL7C245 SIGNAL DESCRIPTIONS (44 PINS)

Signal Name	Pin Number	Signal Type	Signal Description
KDV	1	O	This output controls the operation of the data/voice relay. When low, the data/voice relay is off and the phone line is connected to the phone set. during a data call, the VL7C245 makes this output high to operate the data/voice relay, disconnecting the phone set from the phone line. It may also be used to drive a relay for multi-line phone applications to close the A and A1 leads.
SOUT	2	O	This pin is a serial data output pin. The VL7C245 converts parallel data received from the VL7C224A or internally generated and outputs it in a serial format to the RS232 interface. At all other times the VL7C245 holds this output in the Mark (high) condition.
INTI	3	I	Interrupt Input - Received from the VL7C224A at 600 Hz. Interrupt is detected when this pin has a low to high transition. This signal must stay high for at least 200 nsec.
CKOUT	4	O	Clock Output pin - 9.8304 MHz.
ALE	5	O	Address Latch Enable - The address on AD0-AD7 is valid at the falling edge of this normally low signal.
SIN	6	I	Received serial data . Data from the RS232 interface is input on this pin.
XTAL1	7	I	Used with XTAL2 for crystal (19.6608 MHz).
XTAL2	8	O	Crystal output pin (19.6608 MHz).
VCCP	12		Positive supply (+5 V).
GNDP	15, 33		Ground.
-MCS	16	O	Chip Select for VL7C224A - Active for addressing from 1000H to 10FFH.
-WR	17	O	Write enable - Data on AD0-AD7 is valid at the rising edge of this signal.
-RD	18	O	Read enable - Data on AD0-AD7 must be valid at the rising edge of this signal.
GNDI	22		Ground.
-ECS	23	O	External EEPROM Chip Select - Active for addressing space from 1100H to 11FFH.
-RTS	24	I	Request to Send - Input for RS232 interface.
RESET	29	I	Master Reset - Schmitt-trigger input. A high will cause the VL7C245 to reset.
-HS	34	O	This output, when low, indicates that the modem is in the high speed (2400 bps) mode. When high, it indicates that it is in the low speed modes.
-AA	35	O	This output is low when the VL7C245 is set for auto-answer mode. The output goes high during each ring. If the device is not set to answer the phone, this output goes low each time the phone rings.
-RLSD	36	O	This output goes low when the VL7C245 detects a carrier signal from the remote modem. If the connection is broken or never established, it remains high.

VL7C245 SIGNAL DESCRIPTIONS (44 PINS - CONT.)

Signal Name	Pin Number	Signal Type	Signal Description
-CTS	37	O	This output goes low to indicate the modem is ready to receive data from the RS232 interface.
N.C.	38		No Connect.
-RI	39	I	The output of the ring detector in the DAA is connected to this input. A low level on this input indicates the "On" duration of the ring cycle. This is a Schmitt-trigger input, allowing for slow rising and falling signals on this pin.
-DSR	40	O	This output indicates the status of the modem. Normally connected to the RS232 interface.
-DTR	41	I	This input from the RS232 interface may be used to control the status of the modem.
OH	42	O	This output controls the operation of the hookswitch relay in the DAA. During a data call, this output is high. It operates the hookswitch relay which causes the phone line to be seized. During rotary dialing, the VL7C245 pulses this output at a rate of ten pulses per second with appropriate Mark/Space ratio depending on mode.
-MRDY	43	O	This output goes low when the modem is ready for operation. (An LED indicator is normally driven by this pin.)
VCCI	44		Positive supply (+5 V).
AD0-AD7	19-21, 14, 13, 11, 10, 9	I/O	8-bit bidirectional multiplexed address/data bus for addresses from 1000H to 11FFH.
S0-S6	32, 31, 30, 28, 27, 26, 25	I	7-bit input port for sensing switch settings.

**VL7C235 SIGNAL DESCRIPTIONS (40 PINS)**

Signal Name	Pin Number	Signal Type	Signal Description
KDV	1	O	This output controls the operation of the data/voice relay. When low, the data/voice relay is off and the phone line is connected to the phone set. during a data call, the VL7C235 makes this output high to operate the data/voice relay, disconnecting the phone set from the phone line. It may also be used to drive a relay for multi-line phone applications to close the A and A1 leads.
SOUT	2	O	This pin is a serial data output pin. During a data call, after the connection is established, the VL7C235 converts parallel data received from the computer bus and outputs it in a serial format to the VL7C224A modem for modulation. At all other times the VL7C235 holds this output in the Mark (high) condition.
INTI	3	I	Interrupt Input - Received from the VL7C224A at 600 Hz. Interrupt is detected when this pin has a low to high transition. This signal must stay high for at least 200 nsec.
CKOUT	4	O	Clock Output pin - 9.8304 MHz.
ALE	5	O	Address Latch Enable - The address on AD0-AD7 is valid at the falling edge of this normally low signal.
SIN	6	I	Received serial data . FSK data from the VL7C224A is input on this pin.
XTAL1	7	I	Used with XTAL2 for crystal (19.6608 MHz).
XTAL2	8	O	Crystal output pin (19.6608 MHz).
-MCS	14	O	Chip Select for VL7C224A - Active for addressing from 1000H to 10FFH.
-WR	15	O	Write enable - Data on AD0-AD7 is valid at the rising edge of this signal.
-RD	16	O	Read enable - Data on AD0-AD7 must be valid at the rising edge of this signal.
GND	20		Ground.
-ECS	23		External EEPROM Chip Select - Active for addressing space from 1100H to 11FFH.
RESET	27	I	Master Reset - Schmitt-trigger input. A high will cause the VL7C235 to reset.
A0-A2	33, 32, 31		These three address inputs are used during read or write operation to select an internal UART register in the VL7C235 as shown in Table 2. The Divisor Latch Access Bit (DLAB) must be set high by the system software to access the bit rate divisor latches as shown in Table 2.
-DOST	34	I	The system bus can write data or control words into a selected register of the internal UART when -DOST is low and the chip is selected. Data is latched on the rising edge of the signal.
-RI	35	I	The output of the ring detector in the DAA is connected to this input. A low level on this input indicates the "On" duration of the ring cycle. This is a Schmitt-trigger input, allowing for slow rising and falling signals on this pin.

VL7C235 SIGNAL DESCRIPTIONS (40 PINS - CONT.)

Signal Name	Pin Number	Signal Type	Signal Description
-CS	36		The VL7C235 is selected when this input is low. When high, the VL7C235 forces the data bus lines, D0-D7, into a high impedance state.
-DIST	37	I	The system CPU can read data or status information from a selected register of the internal UART when -DIST is low and the chip is selected.
OH	38	O	This output controls the operation of the hookswitch relay in the DAA. During a data call, this output is high. It operates the hookswitch relay which causes the phone line to be seized. During rotary dialing, the VL7C235 pulses this output at a rate of ten pulses per second with appropriate Mark/Space ratio depending on mode.
INTO	39	O	This output goes high whenever any one of the following interrupt types has an active condition and is enabled via the IER of the internal UART: Receiver Line Status flag, Received Data Available, Transmitter Holding Register Empty, and Modem Status. It is reset low upon the appropriate interrupt servicing. The INTO pin is forced to a high impedance state when the OUT2 bit of the Modem Control Register (MCR) is low (power on state).
VCC	40		Positive supply (+5 V).
AD0-AD7	17-19, 13 12, 11, 10 9	I/O	8-bit bidirectional multiplexed address/data bus for address from 1000H to 11FFH.
D0-D7	30, 29, 28 26, 25, 24 23, 22	I/O	This is the 8-bit data bus comprising of three-state input/output lines. This bus provides bidirectional communication between the VL7C235 and the system CPU. Data control words and status information are transferred via the D0-D7 data bus.

VL7C245 SIGNAL DESCRIPTIONS (40 PINS)

Signal Name	Pin Number	Signal Type	Signal Description
KDV	1	O	This output controls the operation of the data/voice relay. When low, the data/voice relay is off and the phone line is connected to the phone set. during a data call, the VL7C245 makes this output high to operate the data/voice relay, disconnecting the phone set from the phone line. It may also be used to drive a relay for multi-line phone applications to close the A and A1 leads.
SOUT	2	O	This pin is a serial data output pin. The VL7C245 converts parallel data received from the VL7C224A or internally generated and outputs it in a serial format to the RS232 interface. At all other times the VL7C245 holds this output in the Mark (high) condition.
INTI	3	I	Interrupt Input - Received from the VL7C224A at 600 Hz. Interrupt is detected when this pin has a low to high transition. This signal must stay high for at least 200 nsec.
CKOUT	4	O	Clock Output pin - 9.8304 MHz.
ALE	5	O	Address Latch Enable - The address on AD0-AD7 is valid at the falling edge of this normally low signal.
SIN	6	I	Received serial data . Data from the RS232 interface is input on this pin.
XTAL1	7	I	Used with XTAL2 for crystal (19.6608 MHz).
XTAL2	8	O	Crystal output pin (19.6608 MHz).
-MCS	14	O	Chip Select for VL7C224A - Active for addressing from 1000H to 10FFH.
-WR	15	O	Write enable - Data on AD0-AD7 is valid at the rising edge of this signal.
-RD	16	O	Read enable - Data on AD0-AD7 must be valid at the rising edge of this signal.
GND	20		Ground.
-ECS	21	O	External EEPROM Chip Select - Active for addressing space from 1100H to 11FFH.
-RTS	22		Request to Send - Input from RS232 interface.
RESET	27	I	Master Reset - Schmitt-trigger input. A high will cause the VL7C245 to reset.
-HS	31	O	This output, when low, indicates that the modem is in the high speed (2400 bps) mode. When high, it indicates that it is in the low speed modes.
-AA	32	O	This output is low when the VL7C245 is set for auto-answer mode. The output goes high during each ring. If the device is not set to answer the phone, this output goes low each time the phone rings.
-RLSD	33	O	This output goes low when the VL7C245 detects a carrier signal from the remote modem. If the connection is broken or never established, it remains high.

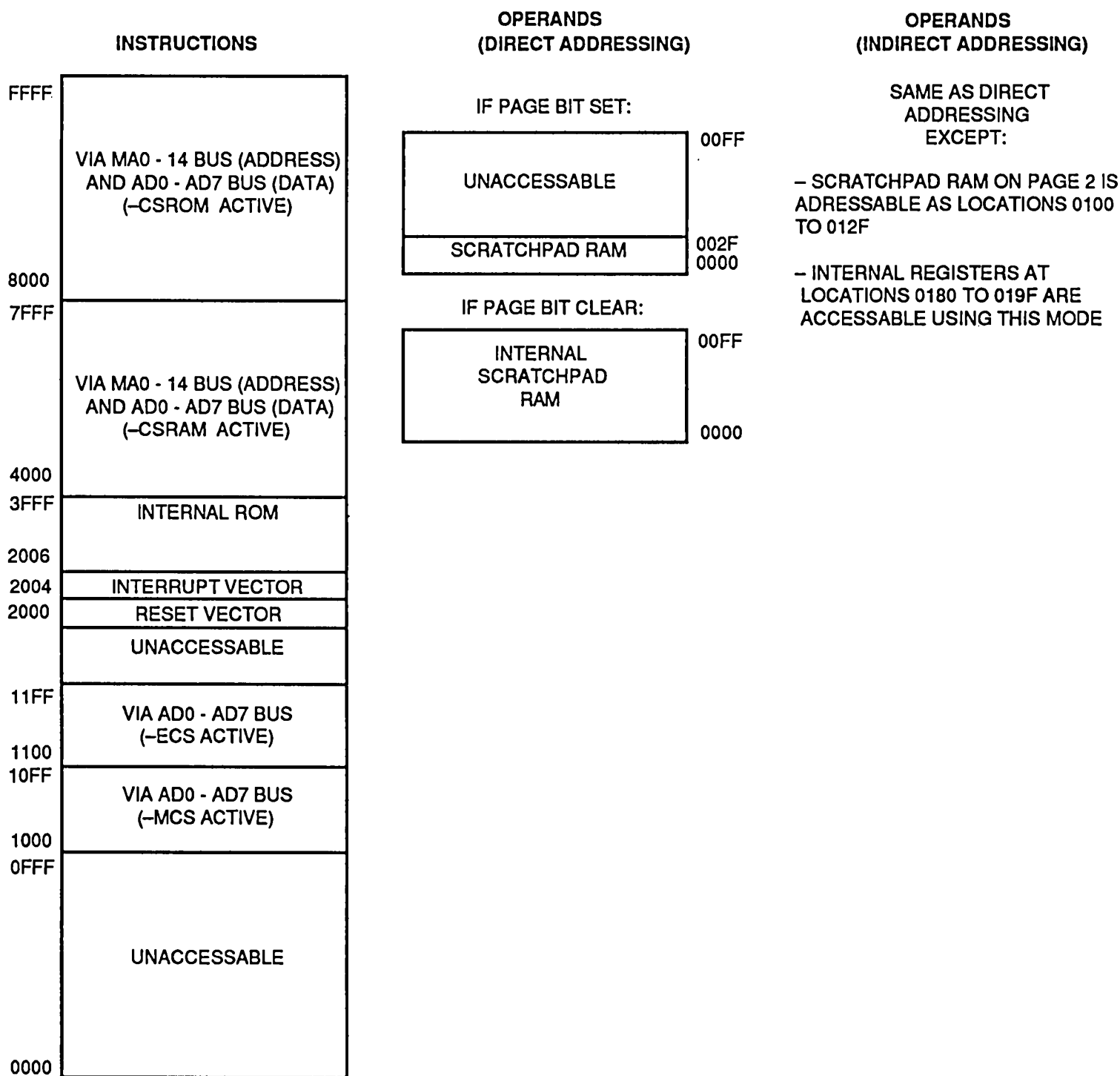
VL7C245 SIGNAL DESCRIPTIONS (40 PINS - CONT.)

Signal Name	Pin Number	Signal Type	Signal Description
-CTS	34	O	This output goes low to indicate the modem is ready to receive data from the RS232 interface.
-RI	35	I	The output of the ring detector in the DAA is connected to this input. A level on this input indicates the "On" duration of the ring cycle. This is a Schmitt-trigger input, allowing for slow rising and falling signals on this pin.
-DSR	36	I/O	This output indicates the status of the modem. Normally connected to the RS232 interface.
-DTR	37	I	This input from the RS232 interface may be used to control the status of the modem.
OH	38	O	This output controls the operation of the hookswitch relay in the DAA. During a data call, this output is high. It operates the hookswitch relay which causes the phone line to be seized. During rotary dialing, the VL7C245 pulses this output at a rate of ten pulses per second with appropriate Mark/Space ratio depending on mode.
-MRDY	39	O	This output goes low when the modem is ready for operation. (An LED indicator is normally driven by this pin.)
VCC	40		Positive supply (+5 V).
AD0-AD7	17-19, 13 12, 11, 10 9	I/O	8-bit bidirectional multiplexed address/data bus for addresses from 1000H to 11FFH.
S0-S6	30, 29, 28, 26, 25, 24, 23	I	7-bit input port for sensing switch settings.

The block diagram illustrates the internal architecture and external interfaces of the 68000 microprocessor. The central component is the 68000 microprocessor, which is divided into several functional blocks:

- Configurable Port and UART:** This block handles external communication. It includes a set of 16 bidirectional pins (A0/-RLSD to D7/-RTS) and a set of 4 pins (OH, KDV, -RI, and RDY/N.C.).
- I/O Port:** This block handles internal data flow between the microprocessor and external devices.
- BUAD RATE GENERATOR:** This block generates the baud rate for the UART. It is connected to the 8-bit UDB0-UDB7 bus and the 8-bit DB0-DB7 bus.
- TIMER:** This block is used for timing and is connected to the 8-bit UDB0-UDB7 bus.
- TRANSMITTER/RECEIVER:** This block handles serial communication. It is connected to the 8-bit UDB0-UDB7 bus and the 8-bit DB0-DB7 bus. It also has a SIN (Serial Input) and SOUT (Serial Output) pin.
- 16 BIT RALU (2901 BASED):** This block is the 16-bit Register Address Latch Unit, which is connected to the 16-bit ADDRESS BUS and the 8-bit DB0-DB7 bus.
- PLA AND CONTROL:** This block is the Programmable Logic Array and Control logic. It is connected to the 16-bit ADDRESS BUS and the 8-bit DB0-DB7 bus. It also has a RESET pin and a CLKOUT pin.
- 8K ROM AND MEMORY INTERFACE:** This block is the memory interface for the 8K ROM. It is connected to the 16-bit ADDRESS BUS and the 8-bit DB0-DB7 bus. It has a set of 16 pins (MA0-MA14, AD0-AD7, -RD, -WR, ALE, INT1, -CSRAM, -CSROM, -MCS, and -ECS).
- 256 BYTE RAM:** This block is the 256-byte Random Access Memory. It is connected to the 16-bit ADDRESS BUS and the 8-bit DB0-DB7 bus. It has a set of 16 pins (00, FF, 100, 12F, 180, and 193).

The diagram shows the interconnections between these blocks, including the 8-bit UDB0-UDB7 bus, the 8-bit DB0-DB7 bus, and the 16-bit ADDRESS BUS.

FIGURE 2. MAC MEMORY MAP




FUNCTIONAL DESCRIPTION

HARDWARE ARCHITECTURE

Figure 1 shows the internal block diagram of the MAC. The MAC is organized with two buses that interconnect its four main logic sections. The two buses are the internal data bus (DB) and address bus. The four sections of the device are:

1. PLA/RALU/control section
2. RAM, register file and I/O ports
3. Program memory and memory control
4. UART

The two bus architecture was chosen to allow the MAC to execute a subset of the 8096 instruction set as fast or faster than the 8096 itself. The device is intended to run at 9.8304 MHz. A typical three operand instruction effectively executes in 10 clock cycles or 1.02 μ S. The signed 16 x 16 multiply operation requires 34 clock cycles or 3.3 μ S. A comparison of execution times to those of an 8096 is given in Table 9.

The internal data bus is an 8-bit bus that interconnects all four sections of the device. All internal data travels on DB. The address bus is a 16-bit output only bus from the RALU that provides addresses to the memory and register sections of the device.

The control/PLA/RALU section controls MAC operations and performs all of the required computation functions. The internal processor consists of a micro-control PLA and a 16-bit registered arithmetic/logic unit which inputs 8096 instruction opcodes and generates the control sequences necessary to implement the instructions. The RALU performs instruction execution, operand address calculation, jump address calculation, program sequencing, and stack control. The program counter (PC) and stack pointer (SP) are contained within the RALU. On reset, the PC points to address 2000 and the SP points to 0131. The RALU is implemented with the 2901 compiler.

The RAM and register file section of the MAC includes RAM and the I/O ports of the device. These locations are all treated as registers and may be accessed in register direct mode.

However, program code can't be executed from registers. The UART and I/O registers are functionally, but not physically, part of the register section. The UART registers are accessed via indirect addressing mode only. There are 304 bytes of RAM to support DSP functions and the modem command set.

The memory section of the MAC includes the program ROM and the external memory interface. The device contains 8k bytes of program ROM. External memory interface allows the MAC to access program or data storage from external memory.

The UART section of the device implements the industry standard 8250B UART. In its parallel configuration the MAC appears as an 8250B to the user via the D0 - D7 data bus. The UART contains dual-port capability to allow the user and the internal processor access to its internal registers independently. The I/O lines of this section may be configured for use in serial modems also and this is internally controlled via a register bit.

MEMORY DESCRIPTION

The memory map of the MAC is shown in Figure 2. The accessibility of memory address locations is dependent on whether the MAC is attempting to fetch an instruction or an operand as shown in the figure. Access of the internal scratchpad RAM and internal registers is via a paged memory system. The first 256 bytes of RAM may be directly addressed if the page bit in the GCR register is clear. The remaining 48 bytes of RAM and the registers are mapped as the second page of low memory and may either be indirectly addressed as locations 0100 to 019F or directly addressed as 0000 to 009F if the page mode bit has been set.

External Read/Write

Three different types of external memory operations are defined.

- A) For addresses from 1000H to 11FFH:
These external operations occur through the AD bus, and take six clock cycles, four more than most

internal operations. This space is intended for MAP & EEROM interfaces, however, instructions and data can also be fetched from this memory space.

- B) For addresses from 4000H to 7FFFH: VL7C225 only.
This memory space is used for external DATA storage. The MAC can access this external RAM space through MA bus and AD bus. These are six clocks memory bytes for easy access. Program instructions may also be fetched from these locations.
- C) For addresses from 8000H to FFFFH: VL7C225 only.
These locations can be used to fetch instructions from external program storage via the MA and AD buses. These operations are exactly the same as internal ROM fetches which take 2 clock cycles.

INTERNAL REGISTER DESCRIPTIONS

This section contains a description of each of the registers in the MAC. All of the registers of the device are 8-bits wide. The registers are made up of bits that are either read-only (RO) or are read/write (R/W). Register addresses are shown in Table 1.

UART Registers

Table 2 summarizes the organization of the UART registers. For a detailed explanation consult an 82C50B data sheet.

UART Monitor Register (UMR)

The UART Monitor register allows the processor to monitor UART operations. A read operation to the UART Monitor register will clear Bit 0 to Bit 4. See Table 3.

Switch Port Register (SWPx) (serial configuration only)

The Switch Port is a 7-bit input port used only in the serial configuration of the MAC. It allows for reading of the external switches in a stand-alone modem application. See Table 4.

Timer Register (TIM)

The Timer includes an 11 bit counter and a timer flip-flop. It is used to aid in software timing functions. The counter



is not readable, however it can be reset by a write to this register. The timer flip-flop bit can be read to test it is set, indicating that the timer has completed one divide by 2048 cycle on the 9.8304 MHz internal clock. Reading or writing this register resets this bit and clears the divide by 2048 counter. This may be used to generate an interrupt at 4.8 KHz for internal processing.

General Control Register (GCR)

GCR (General Control Register) contains a miscellaneous set of control and status bits. See Table 6.

Processor Status Byte (PSB)

This register contains the result codes for each program instruction execution and the global interrupt status and enable bits. See Table 7.

Interrupt Control Register (ICR)

This is an 8 bit register to enable or disable each of the four interrupt sources and to record the interrupt sources. The upper four bits are read/write registers which enable the interrupts, while the lower four bits are read only registers indicating which event(s) generated an interrupt. A read operation to the register will automatically clear these lower four bits.

BIT0: "1" indicates UART requested an interrupt.

BIT1: "1" indicates -RI pin leading edge requested an interrupt.

BIT2: "1" indicates TIMER overflow requested an interrupt.

BIT3: "1" indicates EXTERNAL source requested an interrupt via the INTI pin

BIT4: "1" to enable UART interrupt.

BIT5: "1" to enable -RI pin leading edge interrupt.

BIT6: "1" to enable TIMER overflow interrupt

BIT7: "1" to enable EXTERNAL interrupt

Any one of these four interrupts will drive the processor to address 2004. From there the software can check interrupt sources and do priority control to branch to different service routines.

VL7C235 AND VL7C245 DIFFERENCES

The primary differences between the VL7C225 and the VL7C235 and VL7C245 is that the later have no

provision for accessing external RAM or program memory via the MA bus and that these devices contain internal ROM pre-programmed to implement either a stand-alone serial modem (VL7C245) or PC bus oriented modem (VL7C235) featuring a modem command set compatible with the Hayes 'AT' set.

Another difference is that in order to allow external ROM to function the VL7C225 has a short code segment at the reset and interrupt vector locations of its internal ROM which causes the MAC to vectors to locations 8000 and 8004 for these events.

APPLICATIONS INFORMATION

For complete applications information and circuit diagrams of the VL7C225/235/245 family's use in a V.22 bis modem using the VL7C224A 2400 bps Modem IC, please refer to the VL7C224A data sheet.

SOFTWARE ARCHITECTURE

Operand Types

MAC instructions may use four types of operands: Short Integers, Integers, Long Integers, and Bits.

Short Integers - Short integers are 8-bit signed 2's complement variables. Arithmetic operations which generate results outside the range -128 and +127 will set the overflow bit in the Processor Status Byte (PSB). There are no alignment restrictions on short integers.

Integers - Integers are 16-bit signed 2's complement variables. Arithmetic operation which generate results outside the range -32768 and +32767 will set the overflow bit in the PSB. The least significant byte of the integers is at the even byte address and the most significant byte is at the next higher (odd) address. Therefore the integers must be aligned at even byte boundaries in the address space. The address of a integer is the address of its least significant byte (always an even address).

Bits - The bits within the bytes of the register file are numbered from 0 to 7 with 0 referring to the LSB. The only instructions that use bit addressing are JBC and JBS.

Long Integers - Long integers are 32-bit signed 2's complement variables. The

result of a 16 x 16-bit multiply will be stored as a long integer. Only SHRL and SHLL can manipulate this data type. Long integers are addressed by the address of their least significant byte in the register file. They should be aligned such that their address is evenly divisible by 4. The most significant byte of a long integer resides on "address" +3, where "address" is the long integer's address.

Operand Addressing

Three types of addressing are allowed:

Immediate Addressing - This is a direct address field within the instruction. For short integers, this is an 8-bit field, whereas, for the integers this is a 16-bit field. Only one operand within an instruction can be immediate reference type. This operand must always be the last (right most) operand within an instruction.

e.g. ADD AX,BX,#340H is allowed

ADD AX,#340H, BX is NOT allowed

Register Direct Addressing - In this mode an 8-bit field is used to access a location from the 304 byte scratchpad RAM or internal registers. The address must conform to the alignment rules.

e.g. ADD AX, BX : AX, BX must be "even" numbers and from 00H to FFH in range

ADDB AX, BX : AX, BX can be "odd" or "even" and from 00H to FFH in range

Indirect Addressing - A memory location can be addressed indirectly by placing its 16-bit address in a internal RAM location. Only one operand (the right most operand) within an instruction can be indirect.

e.g. ADDB AX, BX, [CX] is allowed

ADDB AX, [CX], BX is NOT allowed

Instruction Set

The MAC instruction set is a subset of Intel 8096 instruction set and is shown in Table 8. The object codes, formats, and the flags they effect are identical to those of 8096. The differences are:

- No VT or ST flags exist in the MAC.
- Internal register locations can only be accessed by using indirect addressing.



- The operands refer to one or more bytes of the internal RAM. ROM locations can only be addressed using indirect addressing.
- If a memory location is addressed between 1000H and 11FFH an external six clock multiplexed bus operation is initiated. The multiplexed address/data will use AD7-AD0 bus.
- When using ST or STB operations, the destinations are always considered to be indirect addresses.
e.g. ST AX, [BX] is allowed
ST AX, BX is NOT allowed

Interrupt Structure

Four interrupt sources exist in the MAC, namely the external interrupt, timer interrupt, ring leading edge interrupt, and UART interrupt. The interrupt service routine address is 2004H.

External interrupt - A low to high transition on the INTI pin initiates this interrupt.

Timer interrupt - Timer overflow interrupt - 4.8 KHz frequency

Ring leading edge - Interrupt generated by leading edge of ring input pin, -RI

UART interrupts - Interrupt from UART:
Parallel Configuration: From UMR register.

Serial Configuration: In this configuration, the interrupt signal from the UART is used directly as an interrupt source to the internal CPU.

TABLE 1. REGISTER ADDRESS MAP

Name	ABV	Internal (Indirect Addressing Only)		External (A0 - A3)	
		ADR	R/W	ADR	R/W
UART Registers:					
Receive Buffer	RBR	180H	R/W	00H*	RO
Transmit Buffer	THR	18AH	R/W	00H*	WO
Interrupt Enable	IER	181H	R/W	01H*	R/W
Interrupt ID	IIR	182H	RO	02H	RO
Line Control	LCR	183H	R/W	03H	R/W
Modem Control	MCR	184H	R/W	04H	R/W
Line Status	LSR	185H	R/W	05H	R/W
Modem Status	MSR	186H	R/W	06H	R/W
Scratch Pad (8 Bit)	STR	187H	R/W	07H	R/W
Divisor Latch LSB	DLL	188H	R/W	00H**	R/W
Divisor Latch MSB	DLM	189H	R/W	01H**	R/W
Internal Registers:					
UART Monitor	UMR	18BH	R/W		
Switch Port	SWP	18DH	RO		
GCR (General Control Register)	GCR	190H	R/W		
Timer	TIM	191H	R/W		
PSB (Processor Status Byte)	PSB	192H	R/W		
ICR (Interrupt Register)	ICR	193H	R/W		

*DLAB bit in UART LCR register must be zero for access.

**DLAB bit in UART LCR register must be one for access.



TABLE 2. UART REGISTERS

Register Mnemonic	Register Bit Number							
	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
RBR	Data	Data	Data	Data	Data	Data	Data	Data
THR	Data	Data	Data	Data	Data	Data	Data	Data
IER	Receive Data Available Interrupt Enable	THRE Interrupt Enable	Receive Line Status Interrupt Enable	Modem Status Interrupt Enable	0	0	0	0
IIR	0 If Interrupt Pending	Interrupt ID Bit 0	Interrupt ID Bit 1	0	0	0	0	0
LCR	0 = 7 Bit Data 1 = 8 Bit Data	1	0 = 1 Stop Bit 1 = 2 Stop Bits	1 = Parity Enable	1 = Even Parity	1 = Stick Parity	1 = Set Break	DLAB
MCR	Data Terminal Ready	Request to Send	OUT1	OUT2 0 = INT Output to HI-Z	No Function	0	0	0
LSR	Data Ready	Overrun Error	Parity Error	Framing Error	Break Interrupt	THRE	TSRE	0
MSR	0	0	Trailing Edge Ring	Delta RLSD	1 (CTS)	1 (DSR)	RING	RLSD
DLM	Data	Data	Data	Data	Data	Data	Data	Data
DLL	Data	Data	Data	Data	Data	Data	Data	Data
STR	Data	Data	Data	Data	Data	Data	Data	Data

TABLE 3. UART MONITOR (UMR)

Bit Number	Bit Name	Bit Description
7	RTRST	Reset Receiver and Transmitter. When set high, both receiver and transmitter will be put into reset state.
6	CM	UART Command/Modem Control. When set high, the UART is placed in modem mode and data from SIN and SOUT flows to/from the UART. When low, SOUT is forced high and SIN is disconnected from the UART receive register. At reset it is low. This bit together with bit 6 in LCR can be used for bit by bit echoing. In serial mode the user can set bit 6 of LCR = 1, and set CM = to the complement of the RDI bit to echo a bit out the SOUT pin.
5	RDI	Receive Data Input. This bit monitors the Rxd input of the UART.
4	DLF	Divisor Latch Flag. This bit indicates if a new baud rate count has been written to the Divisor Latch.
3	LCF	Line Control Flag. This bit indicates if the line control register has been written.
2	TXF	Transmit Buffer Full Flag. This bit indicates if a new character is in the transmit shadow register.
1	RXF	Receive Buffer Empty Flag. This bit indicates if the last character has been read from the receive buffer.
0	MCF	Modem Control Flag. This bit indicates if the modem control register has been written.

TABLE 4. SWITCH PORT (SWP)

Bit Number	Bit Name	Bit Description
6-0	S6-0	Switch Input. These bits monitor the external switches.
7		Unused.

TABLE 5. TIMER (TIM)

Bit Number	Bit Name	Bit Description
0	TFF0	Timer flip-flop bit.
1-7		Unused.

**TABLE 6. GENERAL CONTROL (GCR)**

Bit Number	Bit Name	Bit Description
7	CONF	Configuration Output. This bit controls the state of the MAC configuration. When high, the MAC is configured with the serial interface. It is configured with the parallel interface after a reset or when a zero (0) is written to this bit.
6	OH	Off Hook Output. When set high, the phone will be placed off hook.
5	KDV	KDV Output.
4	MRDY	Modem Ready Output. (Note.)
3	AA	Active high AA indicator. When high, this bit sets the –AA pin low. (Note.)
2	HS	Active high HS indicator. When high, this bit sets the –HS pin low. (Note.)
1	PAGE	Register Page Bit. This bit selects the active register page. When low, the lower 256 registers are accessed during register operations and when high, the upper page is active.
0	EA	Inverted External Access enable status from –EA pin. This pin reflects the state of the –EA pin.

Note: These bits only have effect if CONF = 1 (i.e., controller is in serial configuration).

TABLE 7. PROGRAM STATUS BYTE (PSB)

Bit Number	Bit Name	Bit Description
7	Not Used	N/A
6	Not Used	N/A
5	IP	Global interrupt pending bit - Set upon receipt of interrupt. Cleared when interrupt service begins.
4	IE	Global interrupt enable bit - When zero, all interrupt are disabled.
3	Z	Zero bit - Indicates the last arithmetic or compare instruction produced a zero result.
2	N	Negative bit; indicates the last arithmetic or compare instruction produced a negative result.
1	C	Carry bit - Indicates the state of the arithmetic carry from the most significant bit of the ALU for an arithmetic operation or the state of the last bit shifted out of the operand for a shift. Arithmetic "borrow" after a subtract is the complement of the C flag (i.e., if borrow generated, then C = 0).
0	V	Overflow bit - Indicates the last arithmetic operation produced an overflow.



TABLE 8. INSTRUCTION SET TABLE

Mnemonic	Number Of Operands	Operation	Bytes*	Time**
ADD/ADDB	2	$B \leftarrow A + B$	3	10
ADD/ADDB	3	$D \leftarrow A + B$	4	10
AND/ANDB	2	$B \leftarrow A \text{ AND } B$	3	10
AND/ANDB	3	$D \leftarrow A \text{ AND } B$	4	10
CMP/CMPB	2	$D - A$	3	10
DJNZ	1	Decrement & JNZ	3	9/12
EXTB	1	Sign Extend Byte	2	7
JBC	0	Jump if Bit Clear	3	10/13
JBS	0	Jump if Bit Set	3	10/13
JC	0	Jump if Carry Set	2	5/8
JNC	0	Jump if No Carr	2	5/8
JE	0	Jump if =	2	5/8
JNE	0	Jump if not =	2	5/8
JGT	0	Jump if >	2	5/8
JGE	0	Jump if > =	2	5/8
JLE	0	Jump if < or =	2	5/8
JLT	0	Jump if <	2	5/8
JV	0	Jump if Overflow	2	5/8
JNV	0	Jump if No Overflow	2	5/8
JH	0	Jump if Higher	2	5/8
JNH	0	Jump if Not Higher	2	5/8
LCALL	1	Long Call	3	11
LD/LDB	2	Load	3	10
MUL	3	$D \leftarrow A * B$	5	33
NOP	0	No Operation	1	2
OR/ORB	2	$D \leftarrow D \text{ OR } A$	3	10
XOR/XORB	2	$D \leftarrow D \text{ XOR } A$	3	10
PUSHF	0	Push PSB	1	5
POPF	0	Pop PSB	1	5
RET	0	Return	1	10
SHL/SHLB	1	Shift Left	3	$11 + N^{***}$
SHLL	1	Shift Left Long	3	$15 + N^{***}$
SHR/SHRB	1	Shift Right	3	$11 + N^{***}$
SHRL	1	Shift Right Long	3	$15 + N^{***}$



TABLE 8. INSTRUCTION SET TABLE (CONT.)

Mnemonic	Number Of Operands	Operation	Bytes*	Time**
SHRA	1	Arith. Right Shift	3	10 + N***
SHRAL	1	Arith. Right Long	3	15 + N***
SJMP	0	Short Jump	2	7
LJMP	0	Long Jump		3
ST/STB	2	Store to Memory	3	13****
SUB/SUBB	2	$B \leftarrow B - A$	3	10
SUB/SUBB	3	$D \leftarrow B - A$	4	10

*Add one for immediate words.

**Add 9 for indirect mode and 2 or 0 for immediate mode, see table.

***N is number of bit shifts.

****Indirect mode

**THE MAC AND INTEL 8096 SPEED COMPARISON**

Table 9 is an instruction execution time comparison for the MAC and Intel 8096. The biggest improvement over 8096 is the 16 bit multiplication it is 3.3 μ s versus 6.5 μ s. The jump instructions are twice faster. The shift instructions

are also about twice faster. The other arithmetic and logic instructions are about the same speed. Indirect addressing instructions in the MAC is about 20% slower than in the 8096.

The following comparison is for the

8096 with 12 MHz crystal and the MAC with 19.6608 MHz. The time unit is " μ s". The instructions and operands are all from internal storage. Both the MAC and Intel 8096 will run slower for external RAM access.

TABLE 9. MAC AND 8096 SPEED COMPARISON

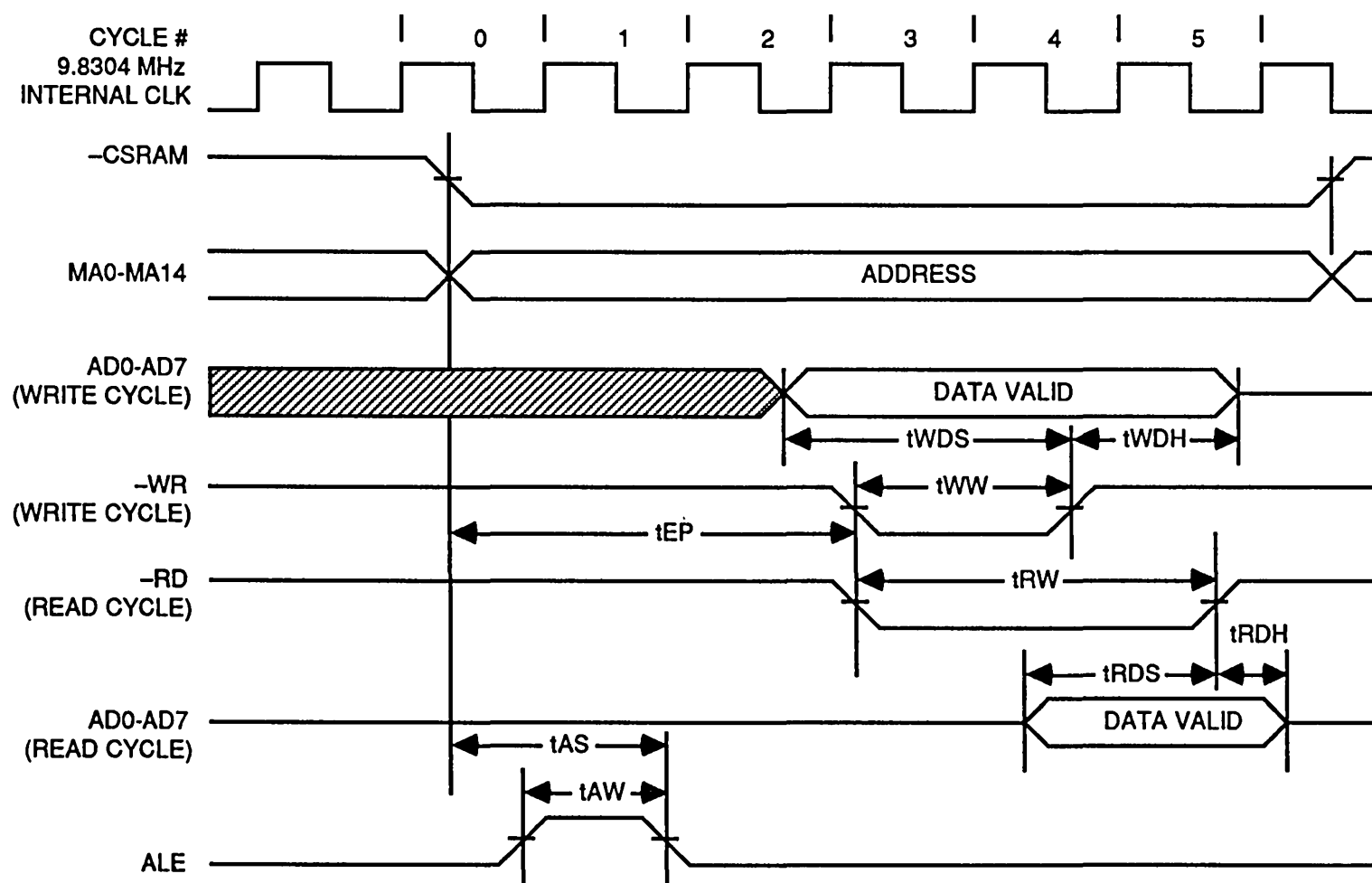
Instr.	Operands	Direct ^a		Immediate		Indirect	
		MAC (μ s)	8096 (μ s)	MAC (μ s)	8096 (μ s)	MAC (μ s)	8096 (μ s)
ADD	2	1.02	1.00	1.22	1.25	1.94	1.50
ADD	3	1.02	1.25	1.22	1.50	1.94	1.75
ADDB	2	1.02	1.00	1.02	1.00	1.94	1.50
ADDB	3	1.02	1.25	1.02	1.25	1.94	1.75
AND	2	1.02	0.75	1.22	1.25	1.94	1.50
AND	3	1.02	1.00	1.22	1.50	1.94	1.75
ANDB	2	1.02	1.00	1.02	1.00	1.94	1.50
ANDB	3	1.02	1.25	1.02	1.25	1.94	1.75
CMP	2	1.02	1.00	1.22	1.25	1.94	1.50
CMPB	2	1.02	1.00	1.02	1.00	1.94	1.50
DJNZ		0.92/1.25	1.25/2.25	(No Jump/Jump)			
EXTB		0.71	1.00				
JBC		1.02/1.32	1.25/2.25				
JBS		1.02/1.32	1.25/2.25				
JC		0.51/0.82	1.00/2.00				
JE		0.51/0.82	1.00/2.00				
JGE		0.51/0.82	1.00/2.00				
JGT		0.51/0.82	1.00/2.00				
JH		0.51/0.82	1.00/2.00				
JLE		0.51/0.82	1.00/2.00				
JLT		0.51/0.82	1.00/2.00				
JNC		0.51/0.82	1.00/2.00				
JNE		0.51/0.82	1.00/2.00				
JNH		0.51/0.82	1.00/2.00				
JNV		0.51/0.82	1.00/2.00				
JV		0.51/0.82	1.00/2.00				

TABLE 9. MAC AND 8096 SPEED COMPARISON (CONT.)

Instr.	Operands	Direct		Immediate		Indirect	
		MAC (μ S)	8096 (μ s)	MAC (μ s)	8096 (μ s)	MAC (μ s)	8096 (μ s)
LCALL		1.12	3.25				
LD	2	1.02	1.00	1.22	1.25	1.94	1.50
LDB	2	1.02	1.00	1.02	1.00	1.94	1.50
MUL	3	3.36	6.50		(Biggest Improvement)		
NOP		0.24	1.00				
OR	2	1.02	1.00	1.22	1.25	1.94	1.50
ORB	2	1.02	1.00	1.02	1.00	1.94	1.50
PUSHF		0.51	2.00				
POPF		0.51	2.25				
RET		1.02	3.00				
SHL		$1.12 + 0.10N$	$1.75 + 0.25N$	(N = Shift Count)			
SHLB		$1.12 + 0.10N$	$1.75 + 0.25N$				
SHLL		$1.53 + 0.10N$	$1.75 + 0.25N$				
SHR		$1.12 + 0.10N$	$1.75 + 0.25N$				
SHRB		$1.12 + 0.10N$	$1.75 + 0.25N$				
SHRL		$1.53 + 0.10N$	$1.75 + 0.25N$				
SHRA		$1.02 + 0.10N$	$1.75 + 0.25N$				
SHRAL		$1.53 + 0.10N$	$1.75 + 0.25N$				
SJMP		0.71	2.00				
ST		1.32	1.75				
STB		1.32	1.75				
SUB	2	1.02	1.00	1.22	1.25	1.94	1.50
SUBB	2	1.02	1.00	1.02	1.00	1.94	1.50
SUB	3	1.02	1.25	1.22	1.50	1.94	1.75
SUBB	3	1.02	1.25	1.02	1.25	1.94	1.75
XOR	2	1.02	1.00	1.22	1.25	1.94	1.50
XORB	2	1.02	1.00	1.02	1.00	1.94	

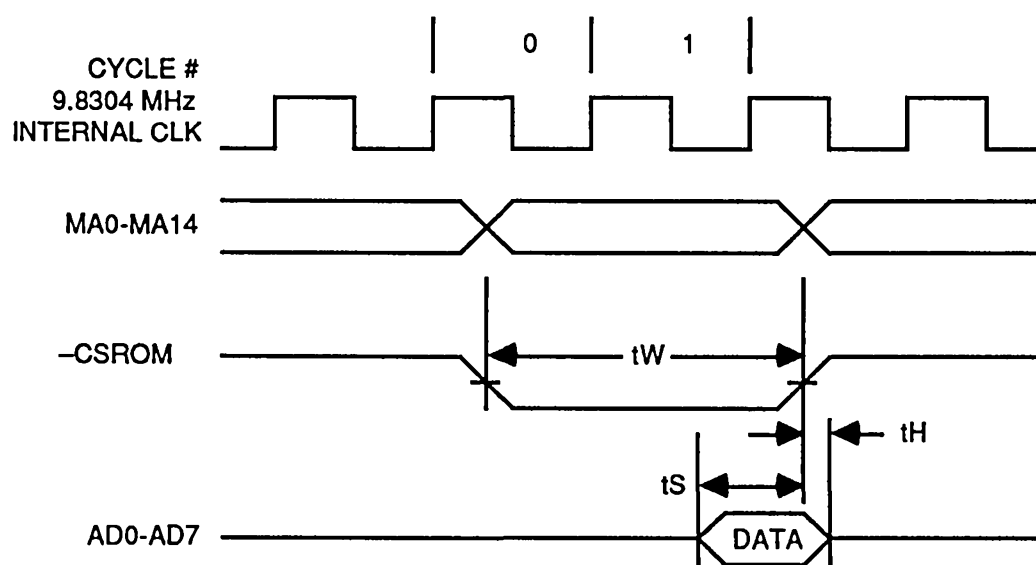
RAM READ OR WRITE CYCLE TIMING

Symbol	Parameter	Min	Typ	Max	Unit	Condition
tAS	Address Setup		152		ns	
tWDS	Write Data Setup		203		ns	
tRDS	Read Data Setup		305		ns	
tSW	–CSRAM Strobe Width		610		ns	
tAW	ALE Strobe Width		101		ns	
tWW	–WR Strobe Width		203		ns	
tRW	–RD Strobe Width		305		ns	
tED	Delay to –WR/–RD		254		ns	
tWDH	Write Data Hold		25		ns	
tRDH	Read Data Hold		0		ns	

RAM READ OR WRITE CYCLE WAVEFORMS


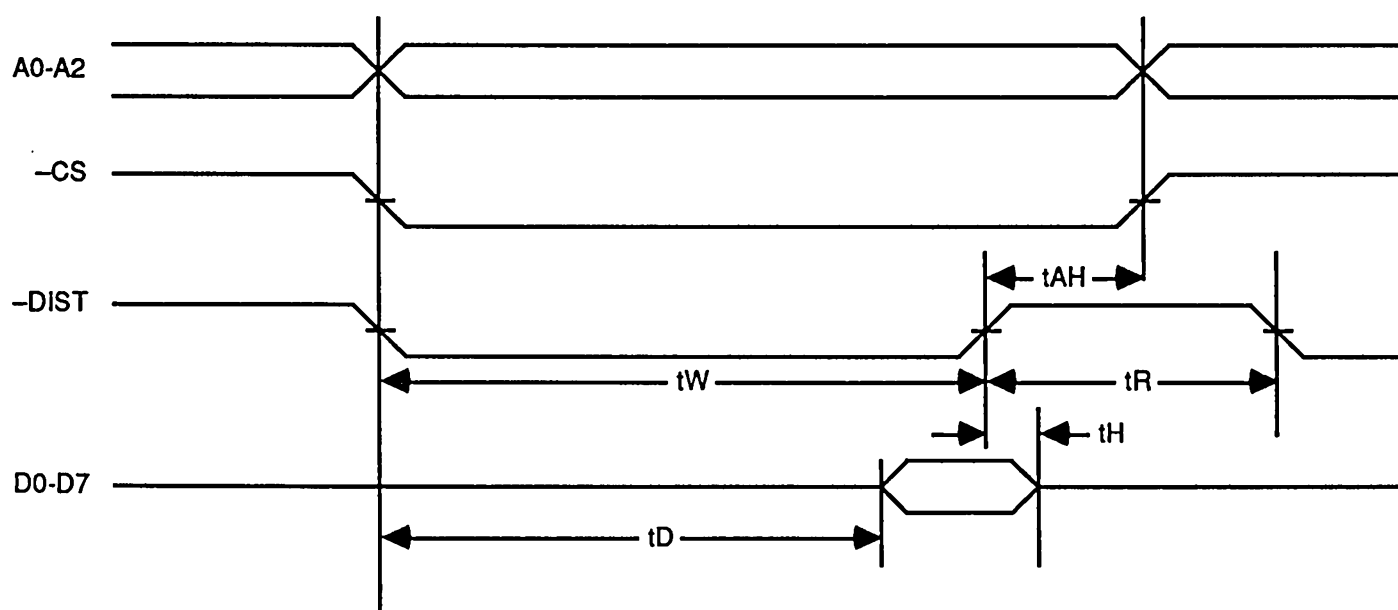
EXTERNAL PROGRAM STORAGE READ BUS CYCLE TIMING

Symbol	Parameter	Min	Typ	Max	Unit	Condition
tS	Data Setup		40		ns	
tH	Data Hold		0		ns	
tW	—CSROM Strobe Width		203		ns	

EXTERNAL PROGRAM STORAGE READ BUS CYCLE WAVEFORMS


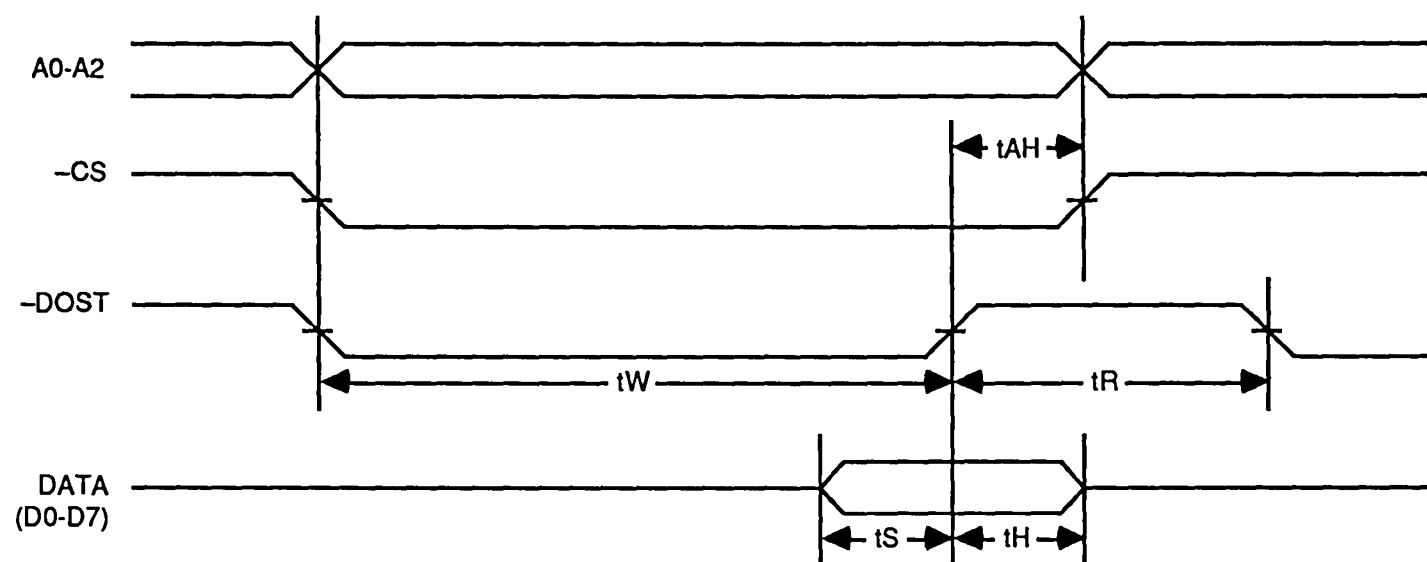
READ CYCLE: PC BUS READ FROM UART REGISTER TIMING

Symbol	Parameter	Min	Typ	Max	Unit	Condition
tW	Enable Strobe Width	300			ns	
tD	–DIST to Data Delay			250	ns	
tH	Data Hold	15			ns	
tAH	Address Hold	0			ns	
tR	Read Cycle Delay	175			ns	

READ CYCLE: PC BUS READ FROM UART REGISTER WAVEFORMS (Parallel Configuration Only)


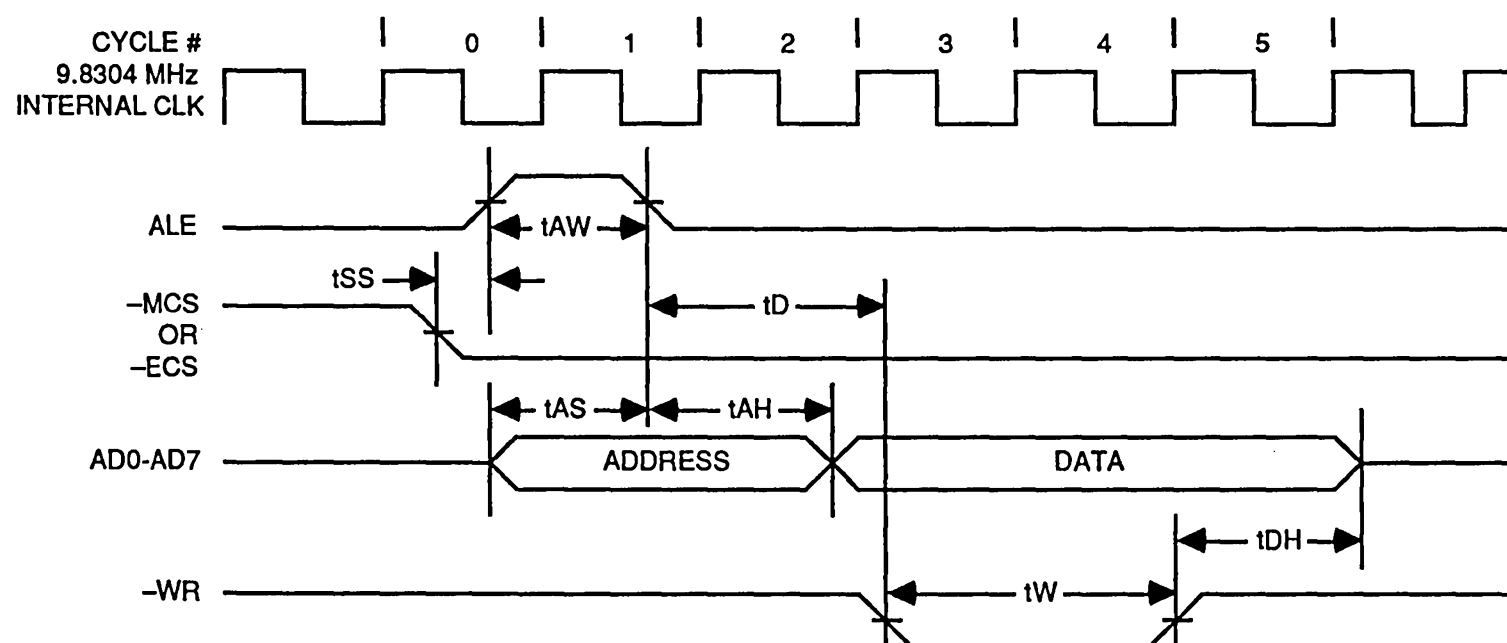
WRITE CYCLE: PC BUS WRITE INTO UART REGISTER TIMING

Symbol	Parameter	Min	Typ	Max	Unit	Condition
tW	-DOST Strobe Width	300			ns	
tS	Data Setup	40			ns	
tH	Data Hold	40			ns	
tAH	Address/Select Hold	20			ns	
tR	Write Cycle Delay	200			ns	

WRITE CYCLE: PC BUS WRITE INTO UART REGISTER WAVEFORMS (Parallel Configuration Only)


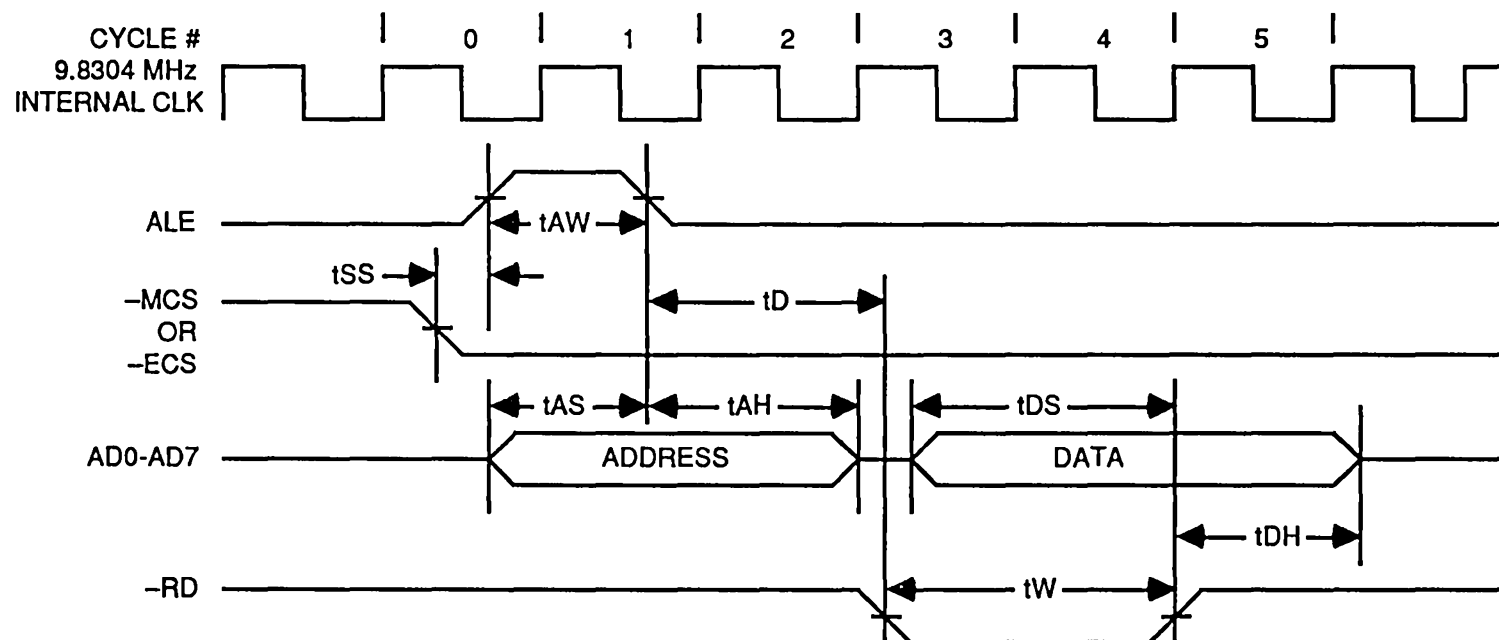
MAP AND EERAM BUS INTERFACE WRITE CYCLE TIMING

Symbol	Parameter	Min	Typ	Max	Unit	Condition
tSS	Delay to ALE		50		ns	
tAW	ALE Strobe Width		101		ns	
tAS	Address Setup		75		ns	
tAH	Address Hold		101		ns	
tD	Delay to $\overline{\text{WR}}$		101		ns	
tW	$\overline{\text{WR}}$ Strobe Width		203		ns	
tDH	Data Hold		101		ns	

MAP AND EERAM BUS INTERFACE WRITE CYCLE WAVEFORM


MAP AND EERAM BUS INTERFACE READ CYCLE TIMING

Symbol	Parameter	Min	Typ	Max	Unit	Condition
t _{SS}	Delay to ALE		50		ns	
t _{AW}	ALE Strobe Width		101		ns	
t _{AS}	Address Setup		75		ns	
t _{AH}	Address Hold		101		ns	
t _D	Delay to $\overline{\text{RD}}$		101		ns	
t _W	$\overline{\text{RD}}$ Strobe Width		305		ns	
t _{DS}	Data Setup		50		ns	
t _{DH}	Data Hold		0		ns	

MAP AND EERAM BUS INTERFACE READ CYCLE WAVEFORMS


ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature 0°C to +70°C
 Storage Temperature -65°C to +150°C
 Supply Voltage to Ground Potential +6 V
 Applied Voltage -0.6 V to VCC +0.6 V
 Power Dissipation 300 mW

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above

those indicated on the operational sections of this specification is not implied and exposure to conditions for extended periods may affect device reliability.

DC CHARACTERISTICS: TA = 0°C to +70°C, VCC = 5 V ±10%

Symbol	Parameter	Min	Typ	Max	Unit	Condition
VCC	Positive Supply Voltage	4.5	5.0	5.5	V	
ICC	Operating Current		35.0		mA	VCC = 5 V
VIH	High Level Input Voltage for: D0-D7, -CS, -DIST, -DOST	2.0			V	
	All Other Input Pins	0.8VCC			V	
VIL	Low Level Input Voltage for: D0-D7, -CS, -DIST, -DOST			0.8	V	
	All Other Input Pins			0.2VCC	V	
IL	Input Leakage Current		±1.0		μA	
VT+	Positive Hysteresis Threshold for RESET and -RI Input Pins		2.5		V	
VT-	Negative Hysteresis Threshold for RESET and -RI Input Pins		1.8		V	
VOH	High Level Output Voltage for: D0-D7, -INTO	0.7VCC + 0.5			V	IOH = 8 mA
	RDY				V	Open Collector
	All Other Output Pins	0.7VCC + 0.5			V	IOH = 2 mA
VOL	Low Level Output Voltage for: D0-D7, -INTO			0.3VCC - 0.5	V	IOL = 8 mA
	RDY			0.3VCC - 0.5	V	IOL = 8 mA
	All Other Output Pins			0.3VCC - 0.5	V	IOL = 2 mA
FCLK	Crystal Frequency	19.6606	19.6608	19.6610	MHz	

300/1200 BIT-PER-SECOND MODEM WITH PIN PROGRAMMABLE RECEIVER GAIN

FEATURES

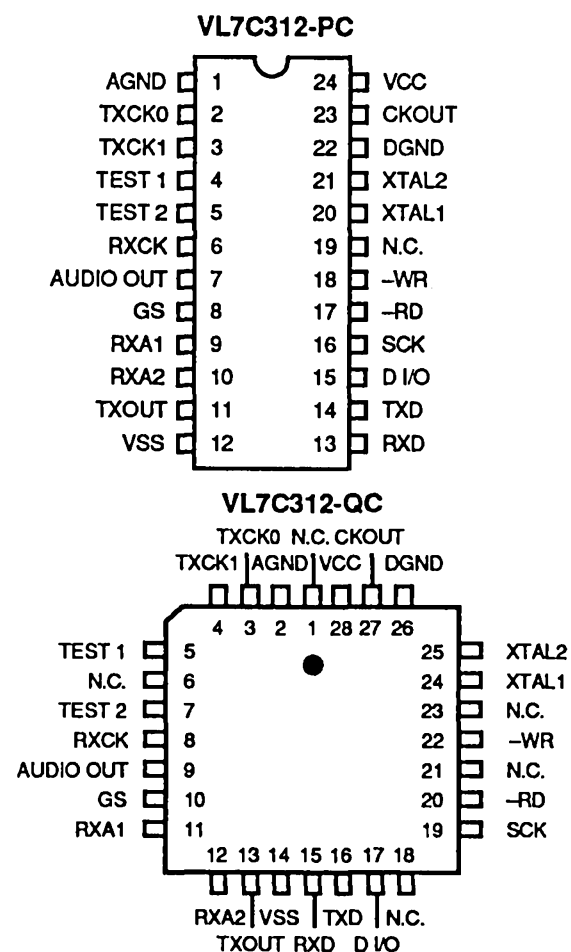
- FSK and PSK modulators and demodulators, high-band and low-band filters with compromise amplitude and group delay equalizers
- Pin programmable receiver gain
- Built-in call progress mode and tone generators for DTMF V.21 and V.22 guard tones
- Bell 212A and CCITT V.21 and V.22 compatible; V.22 notch filters included
- Serial control interface
- Programmable audio output port
- Analog, digital, and remote digital loopback capabilities
- 24-pin DIP and 28-pin plastic leaded chip carrier available

- High level of integration provides a highly cost effective 300/1200 bit-per-second modems
- Eliminates external components, easing design of intelligent modems
- Usable in North American and European modem designs
- Simple board layout
- Simple speaker interface for monitoring phone line
- Testable signal path
- Reduced board area
- Direct replacement for Sierra SC11015

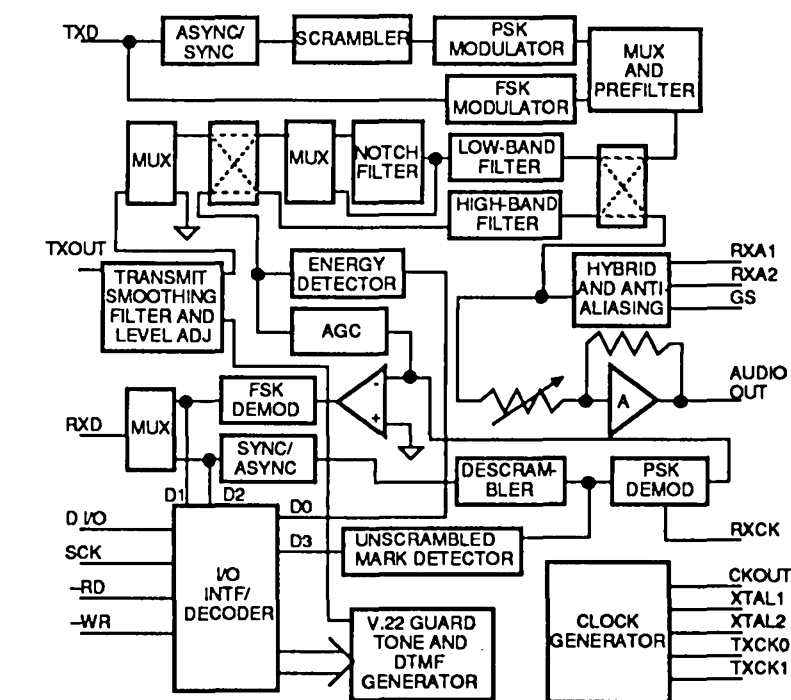
DESCRIPTION

The VL7C312 is a complete 300/1200 bit-per-second modem enhanced with a pin to allow external control of the modem receiver's gain. All of the signal processing functions needed for a full duplex, 300/1200 bit-per-second 212A (V.21 or V.22) modem, including both FSK and PSK modulators and demodulators and the high-band and low-band filters, are integrated on a single chip. It is built using a three-micron CMOS double-polysilicon process that allows analog and digital functions to be combined on the same chip. This design includes capabilities for progress monitoring and for generating DTMF as well as V.21 or V.22 guard tones. The two-to-four wire hybrid is also included, simplifying the interface to a DAA. The VL7C312 also includes analog loopback and remote digital loopback functions for self-testing.

PIN DIAGRAMS



BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Package
VL7C312-PC	Plastic DIP
VL7C312-QC	Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range is 0°C to +70°C.

SIGNAL DESCRIPTIONS

Signal Name	Pin Number (Note)	Signal Description
TXD	14	Transmit Data- Data on this input is modulated by the modem and output on TXOUT pin. A logic low is space and a logic high is mark.
RXD	13	Receive data- The modem demodulates the received carrier and outputs data on this pin. A logic low level is space and a logic high level is mark. The controller can force the demodulator output to the mark state by sending the code 02.
D I/O	15	Data I/O- Data is shifted in serially when WR is low on rising edges of SCK clock. Data is transferred to a latch when WR goes high. Up to seven data bits can be sent. Input codes are defined in Table 1. Data is read from the modem serially when RD is low, on rising edges of SCK clock. Up to four data bits can be read. Output codes are defined in Table 1.
-WR	18	Strobe output from the controller for shifting data to the modem.
-RD	17	Strobe output from the controller for serially reading data from the modem.
SCK	16	Serial shift clock is applied to this pin. It is normally high until data is sent to, or read from, the modem.
TXOUT	11	Transmit data carrier output.
RXA1, RXA2	9, 10	Received data carriers.
GS	8	Gain Select- When left open or tied to VSS, the received signal gain compensation is 0 dB; connected to ground, +2 dB compensation is provided; connected to VCC, the compensation is +3 dB.
AUDIO OUT	7	Output of the hybrid is passed through a programmable attenuator and brought out on this pin. Four levels of received signal can be programmed using the control codes listed in Table 1.
XTAL1, XTAL	20, 21	Pins for connecting a 7.3728 MHz crystal. An external clock signal can be applied to the XTAL1 pin.
CKOUT	23	Buffered crystal oscillator signal is output on this pin. It can drive one LS TTL load.
TXCKO	2	Transmitter Clock Output- In high speed, synchronous internal mode, this output supplies a 1200 Hz clock to the DTE.
TXCK1	3	In high speed, synchronous external mode this pin is an input for receiving a 1200 Hz clock from the DTE.
RXCK	6	Receiver Clock Output- In high speed, synchronous, external mode, the modem supplies a 1200 Hz clock on this output.
VCC	24	+ 5 V power supply.
VSS	12	- 5 V power supply.
DGND	22	Digital ground.
AGND	1	Analog ground.
TEST1, 2	4, 5	Used by VLSI for testing. Make no connection to these pins. They must be left floating.
N.C.	19	No Connect- No internal connection is made to this pin and it may be left floating.

Note: Pin numbers refer to the DIP package.



FUNCTIONAL DESCRIPTION

With the addition of a digital controller, such as an 8-bit microcontroller and a data access arrangement (DAA), a highly cost effective, integrated, intelligent modem can be built. When used with the VLSI VL7C213A modem controller, which is an 8-bit processor combined with a UART, a complete Hayes command set compatible modem can be configured, taking up a minimum of board area. For stand-alone applications, the VL7C312 modem, the VL7C213 controller, a DAA and an RS232-interface are all that are required.

The VL7C312 is truly a modem on a chip. All of the signal processing functions needed for a full duplex, 300/1200 bps Bell 212A or CCITT V.21 or V.22 modem are integrated on a single chip. It operates in a synchronous or asynchronous mode and handles 8, 9, 10, or 11 bit words.

Like all modems, the VL7C312 needs a controller to determine the mode of operation, initiate the call to the remote modem (either pulse or tone dialing), set up the handshaking sequence with the remote modem, monitor the call progress tones on the line (ringing, busy, answer tone, and voice) and switch into the data mode. A simple four-line serial data interface was designed for the VL7C312, enabling it to work with just about any 8-bit microcontroller or microprocessor. The control lines are: DATA INPUT/OUTPUT, SHIFT CLOCK, READ and WRITE.

MODEM

Major sections of the VL7C312 modem are a transmitter, a receiver, low-band and high-band filters, a two-to-four wire hybrid, tone generators and interface logic. It also contains an energy detector that's used for detecting the carrier and call progress monitoring and an audio output for monitoring the line.

The VL7C312 modem requires plus and minus five volts and is available in a 24-pin DIP as well as a 28-pin plastic chip carrier with "J" leads for surface mount applications. The transmitter section consists of an async/sync converter, scrambler, PSK modulator, and FSK modulator. In the high speed mode (1200 bps), the PSK modulator is

connected to the filter. In the low speed mode (300 bps), the FSK modulator is connected to the filter.

TRANSMITTER

Since data terminals and computers may not have the timing accuracy required for 1200 bps transmission (0.01%), timing correction on the incoming data stream must be made. The async/sync converter accepts asynchronous serial data clocked at a rate between 1200 Hz \pm 1%, \pm 2.5%. It outputs serial data at a fixed rate of 1200 Hz \pm 0.01% derived from the master clock oscillator. To compensate for the input and output rate differences, a stop bit is either deleted or inserted when necessary. If the input data rate is slower than the output data rate, a stop bit is inserted. If the input data rate is faster than the output data rate, a stop bit is deleted. The output of the async/sync converter is applied to the scrambler.

The scrambler is a 17-bit shift register clocked at 1200 Hz. Outputs from the 14th and 17th stages are exclusive OR'd and further exclusive OR'd with the input data. The resultant data is supplied to the D input of the shift register. Outputs from the first two stages of the shift register form the dibit that is applied to the PSK modulator. The purpose of the scrambler is to randomize data so that the energy of the modulated carrier is spread over the band of interest. The high-band being centered at 2400 Hz or the low-band, centered at 1200 Hz. A 1200 bps modem actually sends two bits at a time, called a dibit; dibits are sent at 600 baud, the actual rate of transmission; 600 baud is the optimum rate that can be transmitted over the general switched telephone network for a full duplex FDM (frequency division multiplexing) modem because band limit filters in the central office cut off at about 3000 Hz.

The dibit applied to the PSK modulator produces one of four differential phase shifts of the square wave carrier signal (1200 Hz or 2400 Hz) at the 600 Hz baud rate. The resultant waveform is passed through a wave shaping circuit that performs a raised cosine function (this is the shape factor called out in the CCITT V.21 and V.22 specifications;

and it also meets the Bell 212A requirement for optimum transmission). The wave shaped signal is then passed through either the low-band or high-band filter depending upon originate or answer mode selection.

For low speed operation the FSK modulator is used. It produces one of four precision frequencies depending on originate or answer mode and the 1 (mark) or 0 (space) level of the transmit data. The frequencies are produced from the master clock oscillator using programmable dividers. The dividers respond quickly to data changes, introducing negligible bit jitter while maintaining phase coherence. The output of the FSK modulator is applied to the appropriate filter when the low speed mode of the operation is selected.

The filter section consists of low-band (1200 Hz) and high-band (2400 Hz) filters, half-channel compromise amplitude and group delay equalizers for both bands, smoothing filters for both bands and multiplexers for routing of the transmit and receive signals through the appropriate band filters. For CCITT V.21 or V.22 applications, a notch filter is included that can be programmed for either 550 Hz or 1800 Hz. In the call progress monitor mode, the low-band filter is scaled down by a factor of 2.5 to center it over a frequency range of 300 to 660 Hz. Thus, during call establishment in the originate mode, call progress tones can be monitored through the scaled low-band filter and the modem answer tone or voice can be monitored through the unscaled high-band filter.

The low-band filter is a 10th order switched-capacitor band-pass filter with a center frequency of 1200 Hz. In the originate mode, this filter is used in the transmit direction; in the answer mode it is used in the receive direction. When analog loopback is used in the originate mode, this filter, together with the low-band delay equalizer, is in the test loop. In the call progress monitoring mode the filter response is scaled down by 2.5, moving the center frequency to 480 Hz.

The low-band delay equalizer is a 10th order switched-capacitor all-pass filter that compensates for the group delay variation of the low-band filter and half of the compromise line characteristics,

producing a flat delay response within the pass-band.

The high-band filter is a 10th order switched-capacitor band-pass filter with a center frequency of 2400 Hz. In the answer mode, this filter is used in the transmit direction; in the originate mode, it is used in the receive direction. When analog loopback is used in the answer mode, this filter, together with the high-band delay equalizer, will be in the test loop.

The high-band delay equalizer is a 10th order switched-capacitor all-pass filter that compensates for the group delay variation of the high-band filter and half of the compromise line characteristics, producing a flat delay response within the pass-band. The transmit smoothing filter is a second order low-pass switched-capacitor filter that adds the modem transmit signal to the DTMF (V.21 or V.22) guard tones. It also provides a 3 dB per step programmable gain function to set the output level.

RECEIVER

The receiver section consists of an energy detector, AGC, PSK demodulator, FSK demodulator, descrambler, and sync/async converter.

The received signal is routed through the appropriate band-pass filter and applied to both the energy detector and AGC circuit. The energy detector is based on a peak detection algorithm. It provides a detection within 17 to 24 ms. It is set to turn on when the signal exceeds -43 dBm and turn off when the signal falls below -48 dBm. A 2 dB minimum hysteresis is provided between the turn on and turn off levels.

The AGC circuit is a programmable gain amplifier that covers a range of 28 dB in seven steps. The gain is controlled by a 3 bit up/down counter and the Gain Select (GS) pin. See the Signal Description section for operation. Output of the AGC amplifier is rectified and compared with two preset levels corresponding to desired high and low limits. Outputs of the comparators control the up/down counter such that the received signal is amplified to the desired level.

The PSK demodulator uses a coherent demodulation technique. Output of the AGC amplifier is applied to a dual phase splitter that produces an in-phase and

90 degree out of phase component. These components are then demodulated to baseband in a mixer stage where individual components are multiplied by the recovered carrier. The baseband components are low-pass filtered to produce I and Q (In-phase and Quadrature) channel outputs. The I and Q channel outputs are rectified, summed, and passed through a band-pass filter giving a 600 Hz signal. This signal is applied to a digital phase lock loop (DPLL) to produce a baud rate clock. Using the recovered clock signal, the I and Q channels are sampled to produce the received dibit data. The recovered carrier for the demodulator is generated by another PLL which is controlled by the amplitude of the error signal formed by the difference of the I and Q outputs.

The descrambler is similar to the scrambler. The received dibit data is applied to the D input of a 17 bit shift register clocked at 1200 Hz. Outputs from the 14th and 17th stages are exclusive OR'd and further exclusive OR'd with input data to produce received data.

In the asynchronous mode, data from the descrambler is applied to the sync/async converter to reconstruct the originally transmitted asynchronous data. For data which had stop bits deleted at the transmitter (overspeed data), these stop bits are reinserted. Underspeed data is passed essentially unchanged. Output of the sync/async converter along with the output of the FSK demodulator is applied to a multiplexer. The multiplexer selects the appropriate output, depending on the operating speed, and outputs received data on the RXD pin.

For low speed operation, the FSK demodulator is used. The output of the AGC amplifier is passed through a zero crossing detector and applied to a counter that is reset on zero crossings. The counter is designed to cycle at a rate four times faster than the carrier signal. The counter output is low-pass filtered and hard limited to generate FSK data.

HYBRID

The signal on the phone line is the sum of the transmit and receive signals. The hybrid subtracts the transmitted signal

from the signal on the line to form the received signal. It is important to match the hybrid impedance as closely as possible to the telephone line to produce only the received signal. This matching is provided by an external resistor connected between the RXA1 and RXA2 pins on the VL7C312. The filter section provides sufficient attenuation of the out of band signals to eliminate leftover transmit signals from the received signal. The hybrid also acts as a first order low-pass antialiasing filter.

INTERNAL HYBRID

The VL7C312's internal hybrid is intended to simplify the phone line interface. In addition, there is a gain select feature to compensate for the loss in the line coupling transformer used in the DAA. By tying this pin to VSS, ground or VDD, compensation levels of 0, +2 or +3 dB, respectively, are provided.

With a higher loss transformer, some degradation in performance at lower signal levels will occur. Specifically, the bit error rate, when operating at receive will be higher. The energy detect on/off levels measured at the line will also be different from those specified at the chip. With a 3 dB loss transformer, for example, the energy detect on/off levels measured at the line will be in the range of -40/-45 dB rather than -43/-48 dB as specified at the chip. The +3 dB compensation should then be used.

tone generator

The tone generator section consists of a DTMF generator and a V.21 (or V.22) guard tone generator. The DTMF generator produces all of the tones corresponding to digits 0 through 9 and * and # keys. The V.21 (or V.22) guard tone generator produces either 550 Hz or 1800 Hz. Selection of either the 550 Hz or 1800 Hz tone will cascade the corresponding notch filter with the low-band filter. The tones are selected by applying appropriate codes through the Data I/O pin. Before a tone can be generated, tone mode must be selected. Facility is also provided to generate single tones corresponding to the individual rows or column of the DTMF signal.

AUDIO OUTPUT STAGE

A programmable attenuator that can drive a load impedance of 50 K Ω is

provided to allow monitoring of the received line signal through an external speaker. The attenuator is connected to the output of the hybrid. Four levels of attenuation: no attenuation, 6 dB attenuation, 12 dB attenuation and squelch are provided through the ALC1, ALC0 and audio output level control codes. Output of the attenuator is available on the audio output pin where an external audio amplifier (LM386-type) can be connected to drive a low impedance speaker. The output can directly drive a high impedance transducer, but the volume level will be low.

CRYSTAL OSCILLATOR

The VL7C312 includes an inverting amplifier between pins 20 and 21 with an internal bias resistor to simplify the design for the crystal oscillator. A parallel resonant, 7.3728 MHz $\pm 0.001\%$ crystal, designed for a load capacitance of 20 pF, should be connected across pins 20 and 21. Two capacitors of typical values 27 pF from pin 20 to digital ground (DGND pin 22) and 47 pF from pin 21 to DGND should be connected. With the recommended crystal, Saronix, NYMPH, NYP073-20 and these capacitor values, a highly accurate and stable crystal oscillator can be designed. Since the carrier frequency must be within $\pm 0.01\%$ of the nominal 1200/2400 Hz, it is important to measure the actual crystal oscillator frequency at CKOUT (pin 23) and adjust the external capacitors for a given circuit board layout, if necessary.

VL7C213 AND VL7C214 CONTROLLERS

The VL7C213 modem controller, implemented in VLSI's two-micron CMOS process, was designed specifically to handle all of the modem control functions, as well as the interface to a system bus. Besides including an 8-bit microprocessor, 8K by 8 bytes of ROM, and 128 by 8 bytes of RAM, it also contains the functionality of a VL82C50 UART, greatly simplifying the interface to a parallel system bus, such as used in an IBM PC-compatible personal computer (PC). In fact, a complete, Hayes compatible modem for the PC consists of the VL7C213 controller, the VL7C312 modem and the DAA. All of the popular communications software

written for the PC will work with the VL7C312/VL7C213 set.

Another version of the controller, the VL7C214, is intended for RS-232 applications. It contains the same processor, memory, and UART as the VL7C213 and has the same interface to the modem chip. The difference is that the UART is turned around so that serial data from the RS-232 port is converted to parallel data handled by the internal processor. Pins are provided for connecting the familiar switches and indicator lamps found on most stand-alone modems, although the switches and lamps are not needed for operation. All of the switch settings can be done through software.

The VL7C214 provides a standard five volt logic level interface. RS-232 drivers are required to interface to the port. Like the VL7C213, the VL7C214 comes preprogrammed with the Hayes "AT" command set, and when used with the VL7C312 modem, emulates a Hayes-type stand-alone modem. The VL7C213 and VL7C312 emulate a Hayes-type IBM PC plug-in card modem. But the chip set is by no means limited to implementing a Hayes-type smart modem. VLSI is in the custom IC business and both chips were designed with this in mind. For example, only about 6K bytes of the VL7C213's ROM is used for the handshaking and smart modem code, leaving 2K bytes for additional features that a customer may specify. Since the controller is ROM programmable, any command set can be implemented.

Both the VL7C213 and VL7C214 require plus five volts and are available in either a 28-pin DIP or a 28-pin plastic chip carrier with "J" leads for surface mount applications. Besides the four-line interface for the VL7C312 modem, the VL7C213 controller has an 8-bit data port, three address lines, a chip select input, an interrupt line, and the DOST and DIST control lines found in the 8250B UART. It also has control lines for ring indication, the off-hook relay and a data/voice relay; these three lines connect to the DAA.

In the VL7C214, the 8-bit port becomes the switch input lines and the address, chip select, DIST and DOST lines

become the six lines for the RS-232 interface. These six lines are also used to drive the LEDs. Internally, all of these lines are treated as programmable I/O ports under software control. The primary difference between the VL7C213 and VL7C214 is the ROM code. It also contains the same modem and DAA interface lines as the VL7C213.

The VL7C213 and VL7C214 are truly ASIC controllers. They are designed to control a modem or other peripheral that operates at a moderately slow data rate up to 1200 bits per second. The VL7C213 allows a slow peripheral to interface to a high speed bus, without making the main processor slow down.

This is done through the UART interface and the on-chip registers which look somewhat like dual port registers. The main processor can write to and read from them at will, while the on-chip controller can do the same. The controller was designed this way because most communication software has to have unrestrained access to the UART registers. To make the VL7C213 compatible with this software, the registers were included.

The internal processor monitors the registers to determine the mode of operation. Command mode or data mode: at power-up it is automatically put in the command mode and it looks for instructions. Once carrier is detected, it goes into the data mode, and stays there until escape sequence is three "+" signs (+++) in the default mode, but it can be changed in software.

The processor contains an 8-bit data path and can execute 19 instructions with five addressing modes: direct, indirect, immediate, register direct, and register indirect. There is 8K by 8 of ROM on-chip for program storage.

To the system bus, the VL7C213 looks and acts just like a VL82C50 UART. All of the communications software written for this UART will work with the VL7C213 and VL7C214. The VLSI chip set is a Hayes-type modem in two chips.

The VL7C312 AND VL7C213/VL7C214 System

The only external components required by the VL7C212A are the 600 Ω line

matching resistor, a 7.3728 MHz crystal (a standard frequency) and a 20 pF capacitor from each leg of the crystal to ground. If it is desired to drive a speaker to monitor the line, an amplifier such as the LM386 can be added, but the output provided on the VL7C312 can directly drive a high impedance (50 k Ω) earphone-type transducer.

The VL7C213 modem controller's clock in line is driven by the VL7C312's clock out line, so only one crystal is needed. The VL7C213 interfaces directly to an IBM PC bus -- no buffers are required. The only external parts may be an eight input NAND gate for COM1 and COM2 decoding inside the PC.

For tone dialing, the controller sends a code to the modem chip which in turn puts out the called for DTMF tone on the line via the on-chip DTMF generator. For pulse dialing, the controller pulses the OH (off-hook) relay. Both dialing modes work with the built-in call progress algorithm so they won't start dialing until a dial tone is detected.

All modems require a DAA. A DAA (data access arrangement) is a piece of equipment required by the FCC to connect anything to the general switched telephone network. It consists of an isolation transformer, typically 600 Ω to 600 Ω ; a relay for disconnecting the modem from the line; a ring detector, typically an opto-isolator; and high voltage surge protectors. The DAA has to be FCC registered and this can be done by any of many consultants and labs around the country. Another alternative is to buy a DAA, supplied by several manufacturers.

212A is a Bell specification that calls for 1200 bit per second, full or half duplex data transmission with a fallback mode of 300 baud (Bell 103). It is not 1200 baud; the spec calls for transmission of dibits, or 2 bits per baud so the 1200 bps transmission takes place at 600 baud. The same is true for V.22; it's 1200 bps or 600 baud. V.22 does not call for a 300 baud fallback; the CCITT

standard for 300 baud is V.21. It is not a required fallback for V.22, however, it is included in the VL7C312A.

V.22 also calls for guard tones to be sent along with the data. In most of Europe the tone is 1800 Hz except in Sweden where 550 Hz is used. The VL7C312A modem has the 550 Hz and 1800 Hz tone generators built in as well as the 550 and 1800 Hz notch filter to remove the guard tone when in the receive mode.

All modems require a hybrid. Hybrid is a term used to describe a circuit, passive or active, that takes the separate transmit and receive signals and combines them to go over the phone line. In the VL7C312A, this is done with op amps, but the separate signals (TXOUT and RXA2) are also brought out so an external hybrid can be used, if desired. The combined signal comes out on the RXA1 pin and a matching resistor (typically 600 Ω) is connected between RXA1 and RXA2.

TABLE 1. DEFINITION OF I/O CODES
1. Instructions to the modem IC

Data on the D I/O pin is shifted into the modem when WR is low, on rising edges of the SCK clock. Data is transferred into a latch when WR goes high. (See Figure 2 for write cycle waveforms.) Up to seven data bits (D0--D6) can be sent to the device. These bits control the operating modes of the modem as show below:

D6	D5	D4	D3-D0	Mode/Function
0	1/0	0	0	Non-Tone Mode: Reset (set default values)
0	1/0	0	1	Tone On/Off
0	1/0	0	2	Force Receive Data to Mark Off/On
0	1/0	0	3	TLC0 Transmit Level Control Bit 0 (default 0)
0	1/0	0	4	TLC1 Transmit Level Control Bit 1 (default 0)
0	1/0	0	5	TX Transmitter On/Off
0	1/0	0	6	ALB Analog Loopback On/Off
0	1/0	0	7	CPM Call Progress Monitor Mode On/Off
0	1/0	0	8	Connection Indicator (CI) On/Off
0	1/0	0	9	ALCO Audio Output Level Control Bit 0 (default 0)
0	1/0	0	A	ALC1 Audio Output Level Control Bit 1 (default 0)
0	1/0	0	B	WLS0 Word Length Select 0 (default 0)
0	1/0	0	C	WLS1 Word Length Select 1 (default 1)
0	1/0	0	D	Sync/Async
0	1/0	0	E	LS/HS: Low Speed/High Speed
0	1/0	0	F	A/O: Answer/Originate
0	1/0	1	0	Transmit Mark On/Off
0	1/0	1	1	Transmit Space On/Off
0	1/0	1	2	Scrambler Disable On/Off
0	1/0	1	3	DLB Digital Loopback On/Off
0	1/0	1	4	TXDP Transmit Dotting Pattern On/Off
0	1/0	1	5	Locked/Internal
0	1/0	1	6	External/Slave
0	1/0	1	7	2100 Hz Tone On/Off (Must select low speed mode for operation)
0	1/0	1	8	1300 Hz Tone On/Off (Must select low speed mode for operation)
0	1/0	1	9	V.21 On/Off (Must select low speed mode for operation)
1	1/0	0	0	Tone Mode: Dial 0
1	1/0	0	1	Dial 1
1	1/0	0	2	Dial 2
1	1/0	0	3	Dial 3
1	1/0	0	4	Dial 4
1	1/0	0	5	Dial 5
1	1/0	0	6	Dial 6
1	1/0	0	7	Dial 7
1	1/0	0	8	Dial 8
1	1/0	0	9	Dial 9
1	1/0	0	A	Dial *
1	1/0	0	B	Dial #
1	1/0	0	C	Output 550 Hz and Insert 550 Hz Notch in Low-Band Filter
1	1/0	0	D	Output 1800 Hz and Insert 1800 Hz Notch in Low-Band Filter
1	1/0	0	E	Row Disable On/Off
1	1/0	0	F	Column Disable On/Off

TABLE 1. DEFINITION OF I/O CODES (Cont.)

WLS1		WLS0	Word Length
0	0	0	8 Bits
0	1	1	9 Bits
1	0	0	10 Bits (default)
1	1	1	11 Bits
TLC1		TLC0	Transmitter Output Level (dBm) at the Phone Line
0	0	0	-12 (default)
0	1	1	-9
1	0	0	-6
1	1	1	0
ALC1		ALC0	Audio Output Level
0	0	0	Output Off (default)
0	1	1	12 dB Attenuation
1	0	0	6 dB Attenuation
1	1	1	No Attenuation

2. Information from the Modem IC

Data is read serially from the modem when RD is low, on rising edges of the SCK clock. (See Figure 1 for read cycle waveforms.) Up to four data bits (D0--D3) can be read as defined below:

D0 Energy Detect 0 - No Energy 1 - Energy Present

In the CPM mode, the energy detector is connected to the output of the high-band filter, if ALB is off, or the scaled low-band filter, if ALB is on.

D1 Received Data (FSK) 1 - Mark 0 - Space

D2 Received Data (PSK) 1 - Mark 0 - Space

D3 Unscrambled Mark 1 - Detected 0 - Not Detected

Notes:

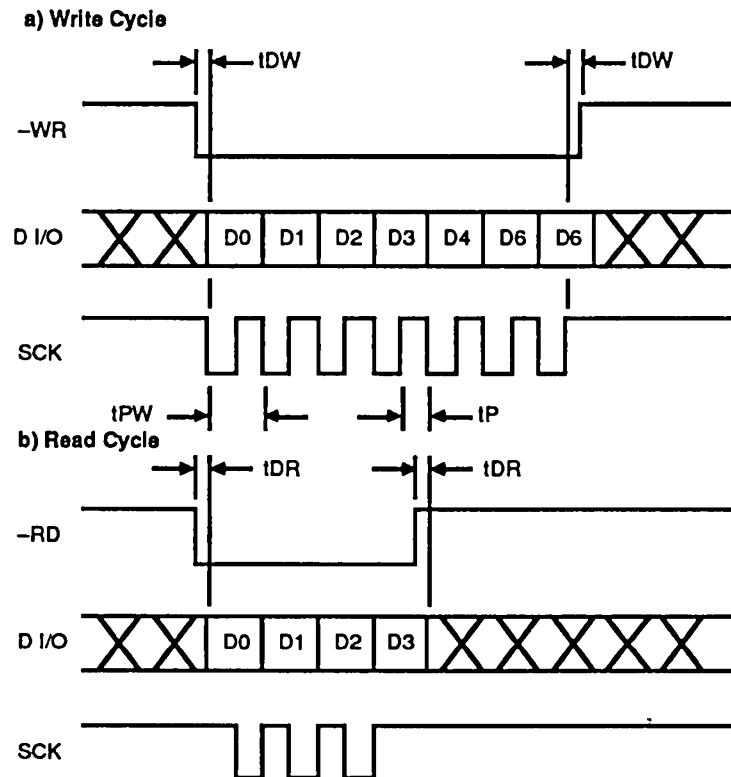
1. Default values for the operating modes on power-up are those shown to the right of the "/" unless otherwise specified.
2. Data is shifted in and out of the modem with LSB first.



TABLE 2. AC CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Units	Conditions
tDW	Delay Time to Write	200			ns	
tDR	Delay Time to Read	200			ns	
tPW	Complete SCK Cycle	1.0			ms	
tP	SCK High Pulse Duration	30		70	%	Duty Cycle
fC	Crystal Frequency	7.3721	7.3728	7.3735	MHz	

FIGURE 1. WAVEFORMS FOR WRITE AND READ CYCLES

DTMF GENERATOR CRYSTAL FREQUENCY = 7.372800 MHz \pm 0%

Parameter	Nominal Frequency	Allowable Error	Actual Error
Row 1	697 Hz	$\pm 1\%$	+ 0.17%
Row 2	770 Hz	$\pm 1\%$	- 0.26%
Row 3	852 Hz	$\pm 1\%$	+ 0.16%
Row 4	941 Hz	$\pm 1\%$	- 0.47%
Column 1	1209 Hz	$\pm 1\%$	- 0.74%
Column 2	1336 Hz	$\pm 1\%$	-0.89%
Column 3	1477 Hz	$\pm 1\%$	- 0.01%
Guard Tones	550 Hz	± 20 Hz	- 1.4 Hz
	1800 Hz	± 20 Hz	+ 7 Hz

DTMF GENERATOR (Cont.)

Parameter	Conditions	Min	Typ	Max	Units
Second Harmonic Distortion	VCC = + 5 V		- 40		dB
Row Output Level	VSS = - 5 V		0		dBm
Column Output Level	TLC0 = 1		2		dBm
550 Hz Guard Tone Level	TLC1 = 1		- 3		dB (Note 2)
1800 Hz Guard Tone Level	Measured at TXOUT Pin		- 6		dB (Note 2)

Note: Guard tone levels are referenced to the TX signal level. When guard tones are added, the TXOUT level is adjusted to maintain a constant level on the line. For 1800 Hz, the adjustment is -0.97 dB; for 550 Hz, the adjustment is -1.76 dB, per the CCITT specification.

MODEM TRANSMIT SIGNALS CRYSTAL FREQUENCY = 7.372800 MHz ±0%

Mode		Bell 103		CCITT V.21		Bell 212A / CCITT V.22	
		Nominal	Actual	Nominal	Actual	Nominal	Actual
Answer	Mark	2225 Hz	2226 Hz	1650 Hz	1649.4 Hz	2400 Hz	2400 Hz
	Space	2025 Hz	2024.4 Hz	1850 Hz	1850.6 Hz		
Originate	Mark	1270 Hz	1269.4 Hz	980 Hz	978.34 Hz	1200 Hz	1200 Hz
	Space	1070 Hz	1070.4 Hz	1180 Hz	1181.53 Hz		
Calling Tone				1300 Hz	1301.7 Hz	1300 Hz	1301.7 Hz
Answer Tone				2100 Hz	2096.9 Hz	2100 Hz	2096.9 Hz

RECEIVER

Parameter	Conditions	Min	Typ	Max	Units
Input Signal Range	At RXA1 (pin 9)	- 45		0	dBm
Intra - Character Bit Rate	At RXD (pin 13)	1170	1200	1224	bps
Carrier Detect	At RXA1 (pin 9)	- 48		- 43	dBm
Carrier Detect Hysteresis		2			dB
Carrier Detect Delay	For 103, 212A and V.22	10	20	30	ms
Carrier Detect Hold	For 103, 212A and V.22	15	20	24	ms
Carrier Detect Delay	For V.21 mode	15	30	40	ms
Carrier Detect Hold	For V.21 mode	20	30	50	ms

TRANSMITTER

Parameter	Conditions	Min	Typ	Max	Units
Input Character Length	Start Bit + Data Bit + Stop Bit	8		11	bits
Intra - Character Bit Rate	At TXD (pin 14)	1170	1200	1212	bps
Input Break Sequence Length	M = Character Length	2M + 3			bits
Output Level Tolerance			± 1		dB

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature
Under Bias: -10°C to +80°C

Storage Temperature
Range: -65°C to +140°C

Maximum Supply
Voltage: VCC = +7.0 V, VSS = -7.0 V

Input Voltage Range:
Analog Pins; VSS -0.6 V to VCC+0.6 V
Digital Pins; DGND-0.6 V to VCC+0.6 V

Maximum Power
Dissipation @25°C: 500 mW

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional Operation of this device at these or any other conditions above

those in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may effect device reliability.

DC CHARACTERISTICS TA= 0°C to 70° C unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Units	Conditions
VCC	Positive Supply Voltage	4.5	5.0	5.5	V	
VSS	Negative Supply Voltage	-4.5	-5.0	-5.5	V	
ICC	Quiescent Current		15		mA	VCC = 5 V
ISS	Quiescent Current			15	mA	VSS = -5 V
VIH	High Level Input Voltage	2.0			V	Digital Signal Pins: -RD, -WR, DI/O, SCK, TXCK1, TXD
VIL	Low Level Input Voltage			0.8	V	Digital Signal Pins: -RD, -WR, DI/O, SCK, TXCK1, TXD
VOH	High Level Output Voltage	4.0 2.0			V V	@IOH= 40 µA (D S Pins: D I/O, CKOUT, RXD, TXCK0, RXCK) @IOH= 500 µA
VOL	Low Level Output Voltage			0.4	V	@IOL=160 µA (D S Pins: D I/O, CKOUT, RXD, TXCK0, RXCK)
VOM	Maximum Output Signal	4.0			Vp-p	TXOUT, RL=1200 Ω (TLC1=1, TLC0=0)
VOM	Maximum Output Signal	1.0			Vp-p	Audio Out, RL= 50 kΩ
VIM	Maximum Input Signal			4.0	Vp-p	RXA1, RXA2

300/1200 BIT-PER-SECOND MODEM (SINGLE 5-VOLT POWER SUPPLY)

FEATURES

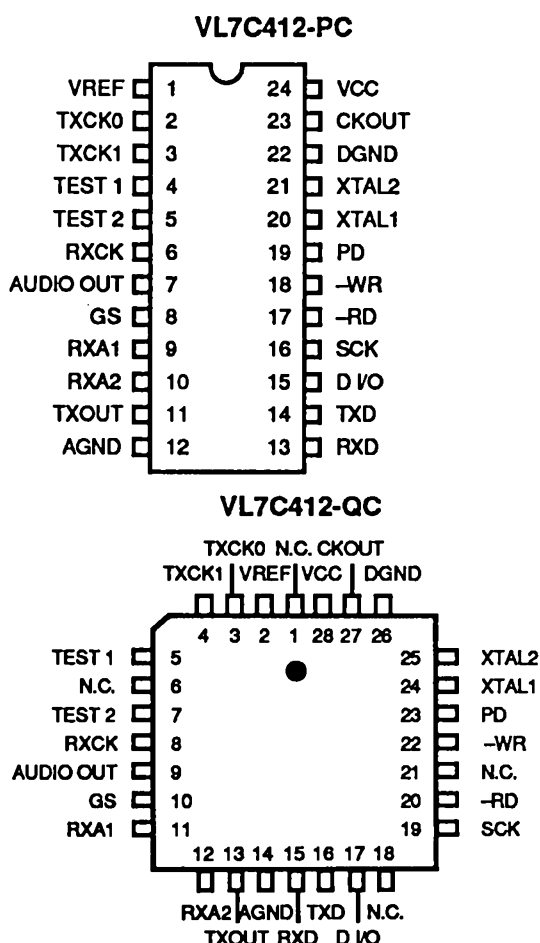
- FSK and PSK modulators and demodulators, high-band and low-band filters with compromise amplitude and group delay equalizers
- Single 5 V power supply with power down by pin or code
- Pin programmable receiver gain
- Built-in call progress mode and tone generators for DTMF V.21 and V.22 guard tones
- Bell 212A and CCITT V.21 and V.22 compatible; V.22 notch filters included
- Serial control interface
- Programmable audio output port
- Analog, digital, and remote digital loopback capabilities
- 24-pin DIP and 28-pin plastic leaded chip carrier available

- High level of integration provides a highly cost effective 300/1200 bit-per-second modems
- Eliminates external components, easing design of intelligent modems
- Usable in North American and European modem designs
- Simple board layout
- Simple speaker interface for monitoring phone line
- Testable signal path
- Reduced board area
- Direct replacement for Sierra SC11016

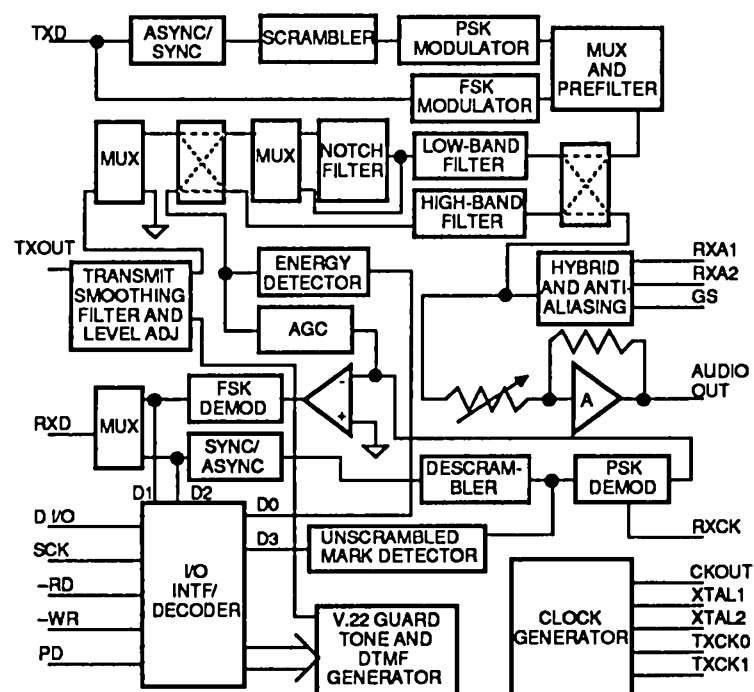
DESCRIPTION

The VL7C412 is a complete, 5 V single supply, 300/1200 bit-per-second modem enhanced with a pin to allow external control of the receiver's gain. All of the signal processing functions needed for a full duplex, 300/1200 bit-per-second 212A (V.21 or V.22) modem, including both FSK and PSK modulators and demodulators and the high-band and low-band filters, are integrated on a single chip. It is built using a three-micron CMOS double-polysilicon process that allows analog and digital functions to be combined on the same chip. This design includes capabilities for progress monitoring and for generating DTMF as well as V.21 or V.22 guard tones. The two-to-four wire hybrid is also included, simplifying the interface to a DAA. The VL7C412 also includes analog loopback and remote digital loopback functions for self-testing.

PIN DIAGRAMS



BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Package
VL7C412-PC	Plastic DIP
VL7C412-QC	Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range is 0°C to +70°C.

SIGNAL DESCRIPTIONS

Signal Name	Pin Number (Note)	Signal Description
TXD	14	Transmit Data- Data on this input is modulated by the modem and output on TXOUT pin. A logic low is space and a logic high is mark.
RXD	13	Receive data- The modem demodulates the received carrier and outputs data on this pin. A logic low level is space and a logic high level is mark. The controller can force the demodulator output to the mark state by sending the code 02.
D I/O	15	Data I/O- Data is shifted in serially when WR is low on rising edges of SCK clock. Data is transferred to a latch when WR goes high. Up to seven data bits can be sent. Input codes are defined in Table 1. Data is read from the modem serially when RD is low, on rising edges of SCK clock. Up to four data bits can be read. Output codes are defined in Table 1.
-WR	18	Strobe output from the controller for shifting data to the modem.
-RD	17	Strobe output from the controller for serially reading data from the modem.
SCK	16	Serial shift clock is applied to this pin. It is normally high until data is sent to, or read from, the modem.
TXOUT	11	Transmit data carrier output.
RXA1, RXA2	9, 10	Received data carriers.
GS	8	Gain Select- When left open or tied to ground, the received signal gain compensation is 0 dB; connected to VREF, +2 dB compensation is provided; connected to VCC, the compensation is +3 dB.
AUDIO OUT	7	Output of the hybrid is passed through a programmable attenuator and brought out on this pin. Four levels of received signal can be programmed using the control codes listed in Table 1.
XTAL1, XTAL	20, 21	Pins for connecting a 7.3728 MHz crystal. An external clock signal can be applied to the XTAL1 pin.
CKOUT	23	Buffered crystal oscillator signal is output on this pin. It can drive one LS TTL load.
TXCKO	2	Transmitter Clock Output- In high speed, synchronous internal mode, this output supplies a 1200 Hz clock to the DTE.
TXCK1	3	In high speed, synchronous external mode this pin is an input for receiving a 1200 Hz clock from the DTE.
RXCK	6	Receiver Clock Output- In high speed, synchronous, external mode, the modem supplies a 1200 Hz clock on this output.
PD	19	Power Down- When this input is high, the device will be powered down, but the oscillator will keep running. When the pin is low, the device will go into normal power mode.
VCC	24	+ 5 V power supply.
AGND	12	Analog Ground- This ground line should be routed separately, and connected to a central grounding point with the digital ground (DGND) as close to the power supply as possible.
DGND	22	Digital ground.
VREF	1	Voltage Reference- This output is a mid-supply reference, generated internally, that is approximately $VCC/2$ in value. It is used as a reference point for the line transformer. VREF should be bypassed to AGND using a 50 μF electrolytic capacitor and a 0.1 μF ceramic capacitor in parallel.
TEST1, 2	4, 5	Used by VLSI for testing. Make no connection to these pins. They must be left floating.

Note: Pin numbers refer to the DIP package.

FUNCTIONAL DESCRIPTION

With the addition of a digital controller, such as an 8-bit microcontroller and a data access arrangement (DAA), a highly cost effective, integrated, intelligent modem can be built. When used with the VLSI VL7C213A modem controller, which is an 8-bit processor combined with a UART, a complete Hayes command set compatible modem can be configured, taking up a minimum of board area. For stand-alone applications, the VL7C412 modem, the VL7C213 controller, a DAA and an RS232-interface are all that are required.

The VL7C412 is a modem on a chip. All of the signal processing functions needed for a full duplex, 300/1200 bps Bell 212A or CCITT V.21 or V.22 modem are integrated on a single chip. It operates in a synchronous or asynchronous mode and handles 8, 9, 10, or 11 bit words.

Like all modems, the VL7C412 needs a controller to determine the mode of operation, initiate the call to the remote modem (either pulse or tone dialing), set up the handshaking sequence with the remote modem, monitor the call progress tones on the line (ringing, busy, answer tone, and voice) and switch into the data mode. A simple four-line serial data interface was designed for the VL7C412, enabling it to work with just about any 8-bit microcontroller or microprocessor. The control lines are: DATA INPUT/OUTPUT, SHIFT CLOCK, READ and WRITE.

MODEM

Major sections of the VL7C412 modem are a transmitter, a receiver, low-band and high-band filters, a two-to-four wire hybrid, tone generators and interface logic. It also contains an energy detector that's used for detecting the carrier and call progress monitoring and an audio output for monitoring the line.

The VL7C212A modem requires only plus five volts, and is available in a 24-pin DIP as well as a 28-pin plastic chip carrier with "J" leads for surface mount applications. The transmitter section consists of an async/sync converter, scrambler, PSK modulator, and FSK modulator. In the high speed mode (1200 bps), the PSK modulator is

connected to the filter. In the low speed mode (300 bps), the FSK modulator is connected to the filter.

TRANSMITTER

Since data terminals and computers may not have the timing accuracy required for 1200 bps transmission (0.01%), timing correction on the incoming data stream must be made. The async/sync converter accepts asynchronous serial data clocked at a rate between 1200 Hz + 1%, -2.5%. It outputs serial data at a fixed rate of 1200 Hz +/- 0.01% derived from the master clock oscillator. To compensate for the input and output rate differences, a stop bit is either deleted or inserted when necessary. If the input data rate is slower than the output data rate, a stop bit is inserted. If the input data rate is faster than the output data rate, a stop bit is deleted. The output of the async/sync converter is applied to the scrambler.

The scrambler is a 17-bit shift register clocked at 1200 Hz. Outputs from the 14th and 17th stages are exclusive OR'd and further exclusive OR'd with the input data. The resultant data is supplied to the D input of the shift register. Outputs from the first two stages of the shift register form the dibit that is applied to the PSK modulator. The purpose of the scrambler is to randomize data so that the energy of the modulated carrier is spread over the band of interest. The high-band being centered at 2400 Hz or the low-band, centered at 1200 Hz. A 1200 bps modem actually sends two bits at a time, called a dibit; dibits are sent at 600 baud, the actual rate of transmission; 600 baud is the optimum rate that can be transmitted over the general switched telephone network for a full duplex FDM (frequency division multiplexing) modem because band limit filters in the central office cut off at about 3000 Hz.

The dibit applied to the PSK modulator produces one of four differential phase shifts of the square wave carrier signal (1200 Hz or 2400 Hz) at the 600 Hz baud rate. The resultant waveform is passed through a wave shaping circuit that performs a raised cosine function (this is the shape factor called out in the CCITT V.21 and V.22 specifications,

and it also meets the Bell 212A requirement for optimum transmission). The wave shaped signal is then passed through either the low-band or high-band filter depending upon originate or answer mode selection.

For low speed operation the FSK modulator is used. It produces one of four precision frequencies depending on originate or answer mode and the 1 (mark) or 0 (space) level of the transmit data. The frequencies are produced from the master clock oscillator using programmable dividers. The dividers respond quickly to data changes, introducing negligible bit jitter while maintaining phase coherence. The output of the FSK modulator is applied to the appropriate filter when the low speed mode of the operation is selected.

The filter section consists of low-band (1200 Hz) and high-band (2400 Hz) filters, half-channel compromise amplitude and group delay equalizers for both bands, smoothing filters for both bands and multiplexers for routing of the transmit and receive signals through the appropriate band filters. For CCITT V.21 or V.22 applications, a notch filter is included that can be programmed for either 550 Hz or 1800 Hz. In the call progress monitor mode, the low-band filter is scaled down by a factor of 2.5 to center it over a frequency range of 300 to 660 Hz. Thus, during call establishment in the originate mode, call progress tones can be monitored through the scaled low-band filter and the modem answer tone or voice can be monitored through the unscaled high-band filter.

The low-band filter is a 10th order switched-capacitor band-pass filter with a center frequency of 1200 Hz. In the originate mode, this filter is used in the transmit direction; in the answer mode it is used in the receive direction. When analog loopback is used in the originate mode, this filter, together with the low-band delay equalizer, is in the test loop. In the call progress monitoring mode the filter response is scaled down by 2.5, moving the center frequency to 480 Hz.

The low-band delay equalizer is a 10th order switched-capacitor all-pass filter that compensates for the group delay variation of the low-band filter and half of the compromise line characteristics,

producing a flat delay response within the pass-band.

The high-band filter is a 10th order switched-capacitor band-pass filter with a center frequency of 2400 Hz. In the answer mode, this filter is used in the transmit direction; in the originate mode, it is used in the receive direction. When analog loopback is used in the answer mode, this filter, together with the high-band delay equalizer, will be in the test loop.

The high-band delay equalizer is a 10th order switched-capacitor all-pass filter that compensates for the group delay variation of the high-band filter and half of the compromise line characteristics, producing a flat delay response within the pass-band. The transmit smoothing filter is a second order low-pass switched-capacitor filter that adds the modem transmit signal to the DTMF (V.21 or V.22) guard tones. It also provides a 3 dB per step programmable gain function to set the output level.

RECEIVER

The receiver section consists of an energy detector, AGC, PSK demodulator, FSK demodulator, descrambler, and sync/async converter.

The received signal is routed through the appropriate band-pass filter and applied to both the energy detector and AGC circuit. The energy detector is based on a peak detection algorithm. It provides a detection within 17 to 24 ms. It is set to turn on when the signal exceeds -43 dBm and turn off when the signal falls below -48 dBm. A 2 dB minimum hysteresis is provided between the turn on and turn off levels.

The AGC circuit is a programmable gain amplifier that covers a range of 28 dB in seven steps. The gain is controlled by a 3 bit up/down counter and the Gain Select (GS) pin. See Signal Descriptions for operation. Output of the AGC amplifier is rectified and compared with two preset levels corresponding to desired high and low limits. Outputs of the comparators control the up/down counter such that the received signal is amplified to the desired level.

The PSK demodulator uses a coherent demodulation technique. Output of the AGC amplifier is applied to a dual phase splitter that produces an in-phase and

90 degree out of phase component. These components are then demodulated to baseband in a mixer stage where individual components are multiplied by the recovered carrier. The baseband components are low-pass filtered to produce I and Q (In-phase and Quadrature) channel outputs. The I and Q channel outputs are rectified, summed, and passed through a band-pass filter giving a 600 Hz signal. This signal is applied to a digital phase lock loop (DPLL) to produce a baud rate clock. Using the recovered clock signal, the I and Q channels are sampled to produce the received dibit data. The recovered carrier for the demodulator is generated by another PLL which is controlled by the amplitude of the error signal formed by the difference of the I and Q outputs.

The descrambler is similar to the scrambler. The received dibit data is applied to the D input of a 17 bit shift register clocked at 1200 Hz. Outputs from the 14th and 17th stages are exclusive OR'd and further exclusive OR'd with input data to produce received data.

In the asynchronous mode, data from the descrambler is applied to the sync/async converter to reconstruct the originally transmitted asynchronous data. For data which had stop bits deleted at the transmitter (overspeed data), these stop bits are reinserted. Underspeed data is passed essentially unchanged. Output of the sync/async converter along with the output of the FSK demodulator is applied to a multiplexer. The multiplexer selects the appropriate output, depending on the operating speed, and outputs received data on the RXD pin.

For low speed operation, the FSK demodulator is used. The output of the AGC amplifier is passed through a zero crossing detector and applied to a counter that is reset on zero crossings. The counter is designed to cycle at a rate four times faster than the carrier signal. The counter output is low-pass filtered and hard limited to generate FSK data.

HYBRID

The signal on the phone line is the sum of the transmit and receive signals. The hybrid subtracts the transmitted signal

from the signal on the line to form the received signal. It is important to match the hybrid impedance as closely as possible to the telephone line to produce only the received signal. This matching is provided by an external resistor connected between the RXA1 and RXA2 pins on the VL7C412. The filter section provides sufficient attenuation of the out of band signals to eliminate leftover transmit signals from the received signal. The hybrid also acts as a first order low-pass antialiasing filter.

INTERNAL HYBRID

The VL7C412 internal hybrid is intended to simplify the phone line interface. In addition, there is a gain select feature to compensate for the loss in the line coupling transformer used in the DAA. By tying this pin to VSS, ground or VDD, compensation levels of 0, +2 or +3 dB, respectively, are provided.

With a higher loss transformer, some degradation in performance at lower signal levels will occur. Specifically, the bit error rate, when operating at receive will be higher. The energy detect on/off levels measured at the line will also be different from those specified at the chip. With a 3 dB loss transformer, for example, the energy detect on/off levels measured at the line will be in the range of -40/-45 dB rather than -43/-48 dB as specified at the chip. The +3 dB compensation should then be used.

tone generator

The tone generator section consists of a DTMF generator and a V.21 (or V.22) guard tone generator. The DTMF generator produces all of the tones corresponding to digits 0 through 9 and * and # keys. The V.21 (or V.22) guard tone generator produces either 550 Hz or 1800 Hz. Selection of either the 550 Hz or 1800 Hz tone will cascade the corresponding notch filter with the low-band filter. The tones are selected by applying appropriate codes through the Data I/O pin. Before a tone can be generated, tone mode must be selected. Facility is also provided to generate single tones corresponding to the individual rows or column of the DTMF signal.

AUDIO OUTPUT STAGE

A programmable attenuator that can drive a load impedance of 50 k Ω is provided to allow monitoring of the



received line signal through an external speaker. The attenuator is connected to the output of the hybrid. Four levels of attenuation: no attenuation, 6 dB attenuation, 12 dB attenuation and squelch are provided through the ALC1, ALC0 and audio output level control codes. Output of the attenuator is available on the audio output pin where an external audio amplifier (LM386-type) can be connected to drive a low impedance speaker. The output can directly drive a high impedance transducer, but the volume level will be low.

VL7C213 AND VL7C214 CONTROLLERS

The VL7C213 modem controller, implemented in VLSI's two-micron CMOS process, was designed specifically to handle all of the modem control functions, as well as the interface to a system bus. Besides including an 8-bit microprocessor, 8K by 8 bytes of ROM, and 128 by 8 bytes of RAM, it also contains the functionality of a VL82C50 UART, greatly simplifying the interface to a parallel system bus, such as used in an IBM PC-compatible personal computer (PC). In fact, a complete, Hayes compatible modem for the PC consists of the VL7C213 controller, the VL7C412 modem and the DAA. All of the popular communications software written for the PC will work with the VL7C412/VL7C213 set.

Another version of the controller, the VL7C214, is intended for RS-232 applications. It contains the same processor, memory, and UART as the VL7C213 and has the same interface to the modem chip. The difference is that the UART is turned around so that serial data from the RS-232 port is converted to parallel data handled by the internal processor. Pins are provided for connecting the familiar switches and indicator lamps found on most stand-alone modems, although the switches and lamps are not needed for operation. All of the switch settings can be done through software.

The VL7C214 provides a standard five volt logic level interface. RS-232 drivers are required to interface to the port. Like the VL7C213, the VL7C214 comes preprogrammed with the Hayes "AT" command set, and when used with the

VL7C412 modem, emulates a Hayes-type stand-alone modem. The VL7C213 and VL7C412 emulate a Hayes-type IBM PC plug-in card modem. But the chip set is by no means limited to implementing a Hayes-type smart modem. VLSI is in the custom IC business and both chips were designed with this in mind. For example, only about 6K bytes of the VL7C213's ROM is used for the handshaking and smart modem code, leaving 2K bytes for additional features that a customer may specify. Since the controller is ROM programmable, any command set, not just the Hayes "AT" set, can be implemented.

Both the VL7C213 and VL7C214 require plus five volts and are available in either a 28-pin DIP or a 28-pin plastic chip carrier with "J" leads for surface mount applications. Besides the four-line interface for the VL7C412 modem, the VL7C213 controller has an 8-bit data port, three address lines, a chip select input, an interrupt line, and the DOST and DIST control lines found in the 8250B UART. It also has control lines for ring indication, the off-hook relay and a data/voice relay; these three lines connect to the DAA.

In the VL7C214, the 8-bit port becomes the switch input lines and the address, chip select, DIST and DOST lines become the six lines for the RS-232 interface. These six lines are also used to drive the LEDs. Internally, all of these lines are treated as programmable I/O ports under software control. The primary difference between the VL7C213 and VL7C214 is the ROM code. It also contains the same modem and DAA interface lines as the VL7C213.

The VL7C213 and VL7C214 are truly ASIC controllers. They are designed to control a modem or other peripheral that operates at a moderately slow data rate up to 1200 bits per second. The VL7C213 allows a slow peripheral to interface to a high speed bus, without making the main processor slow down.

This is done through the UART interface and the on-chip registers which look somewhat like dual port registers. The main processor can write to and read from them at will, while the on-chip

controller can do the same. The controller was designed this way because most communication software has to have unrestrained access to the UART registers. To make the VL7C213 compatible with this software, the registers were included.

The internal processor monitors the registers to determine the mode of operation. Command mode or data mode: at power-up it is automatically put in the command mode and it looks for instructions. Once carrier is detected, it goes into the data mode, and stays there until escape sequence is three "+" signs (+++) in the default mode, but it can be changed in software.

The actual processor contains an 8-bit data path and can execute 19 instructions with five different addressing modes: direct, indirect, immediate, register direct, and register indirect. There is 8K by 8 of ROM on-chip for program storage.

To the system bus, the VL7C213 looks and acts just like a VL82C50 UART. All of the communications software written for this UART will work with the VL7C213 and VL7C214. The VLSI chip set is a Hayes-type modem in two chips.

CRYSTAL OSCILLATOR

The VL7C412 includes an inverting amplifier between pins 20 and 21 with an internal bias resistor to simplify the design for the crystal oscillator. A parallel resonant, 7.3728 MHz $\pm 0.001\%$ crystal, designed for a load capacitance of 20 pF, should be connected across pins 20 and 21. Two capacitors of typical values 27 pF from pin 20 to digital ground (DGND pin 22) and 47 pF from pin 21 to DGND should be connected. With the recommended crystal, Saronix, NYMPH, NYP073-20 and these capacitor values, a highly accurate and stable crystal oscillator can be designed. Since the carrier frequency must be within $\pm 0.01\%$ of the nominal 1200/2400 Hz, it is important to measure the actual crystal oscillator frequency at CKOUT (pin 23) and adjust the external capacitors for a given circuit board layout, if necessary.

The VL7C412 AND VL7C213/VL7C214 System

The only external components required by the VL7C412 are the 600 Ω line

matching resistor, a 7.3728 MHz crystal (a standard frequency) and a 20 pF capacitor from each leg of the crystal to ground. If it is desired to drive a speaker to monitor the line, an amplifier like the LM386 can be added, but the output provided on the VL7C412 can directly drive a high impedance (50 k Ω) earphone-type transducer.

The VL7C213 modem controller's clock in line is driven by the VL7C412's clock out line, so only one crystal is needed. The VL7C213 interfaces directly to an IBM PC bus -- no buffers are required. The only external parts may be an eight input NAND gate for COM1 and COM2 decoding inside the PC.

For tone dialing, the controller sends a code to the modem chip which in turn puts out the called for DTMF tone on the line via the on-chip DTMF generator. For pulse dialing, the controller pulses the OH (off-hook) relay. Both dialing modes work with the built-in call progress algorithm so they won't start

dialing until a dial tone is detected.

All modems require a DAA. A DAA (data access arrangement) is a piece of equipment required by the FCC to connect anything to the general switched telephone network. It consists of an isolation transformer, typically 600 Ω to 600 Ω ; a relay for disconnecting the modem from the line; a ring detector, typically an opto-isolator; and high voltage surge protectors. The DAA has to be FCC registered and this can be done by any of many consultants and labs around the country. Another alternative is to buy a DAA, supplied by several manufacturers.

212A is a Bell specification that calls for 1200 bit per second, full or half duplex data transmission with a fallback mode of 300 baud (Bell 103). It is not 1200 baud; the spec calls for transmission of dibits, or 2 bits per baud so the 1200 bps transmission takes place at 600 baud. The same is true for V.22; it's 1200 bps or 600 baud. V.22 does not

call for a 300 baud fallback; the CCITT standard for 300 baud is V.21. It is not a required fallback for V.22, however, it is included in the VL7C412.

V.22 also calls for guard tones to be sent along with the data. In most of Europe the tone is 1800 Hz except in Sweden where 550 Hz is used. The VL7C412 modem has the 550 Hz and 1800 Hz tone generators built in as well as the 550 and 1800 Hz notch filter to remove the guard tone when in the receive mode.

All modems require a hybrid. Hybrid is a term used to describe a circuit, passive or active, that takes the separate transmit and receive signals and combines them to go over the phone line. In the VL7C412, this is done with op amps, but the separate signals (TXOUT and RXA2) are also brought out so an external hybrid can be used, if desired. The combined signal comes out on the RXA1 pin and a matching resistor (typically 600 Ω) is connected between RXA1 and RXA2.

TABLE 1. DEFINITION OF I/O CODES
1. Instructions to the modem IC

Data on the D I/O pin is shifted into the modem when WR is low, on rising edges of the SCK clock. Data is transferred into a latch when WR goes high. (See Figure 2 for write cycle waveforms.) Up to seven data bits (D0--D6) can be sent to the device. These bits control the operating modes of the modem as show below:

D6	D5	D4	D3-D0	Mode/Function
Non-Tone Mode:				
0	1/0	0	0	Reset (set default values)
0	1/0	0	1	Tone On/Off
0	1/0	0	2	Force Receive Data to Mark Off/On
0	1/0	0	3	TLC0 Transmit Level Control Bit 0 (default 0)
0	1/0	0	4	TLC1 Transmit Level Control Bit 1 (default 0)
0	1/0	0	5	TX Transmitter On/Off
0	1/0	0	6	ALB Analog Loopback On/Off
0	1/0	0	7	CPM Call Progress Monitor Mode On/Off
0	1/0	0	8	Connection Indicator (CI) On/Off
0	1/0	0	9	ALCO Audio Output Level Control Bit 0 (default 0)
0	1/0	0	A	ALC1 Audio Output Level Control Bit 1 (default 0)
0	1/0	0	B	WLS0 Word Length Select 0 (default 0)
0	1/0	0	C	WLS1 Word Length Select 1 (default 1)
0	1/0	0	D	Sync/Async
0	1/0	0	E	LS/HS: Low Speed/High Speed
0	1/0	0	F	A/O: Answer/Originate
0	1/0	1	0	Transmit Mark On/Off
0	1/0	1	1	Transmit Space On/Off
0	1/0	1	2	Scrambler Disable On/Off
0	1/0	1	3	DLB Digital Loopback On/Off
0	1/0	1	4	TXDP Transmit Dotting Pattern On/Off
0	1/0	1	5	Locked/Internal
0	1/0	1	6	External/Slave
0	1/0	1	7	2100 Hz Tone On/Off (Must select low speed mode for operation)
0	1/0	1	8	1300 Hz Tone On/Off (Must select low speed mode for operation)
0	1/0	1	9	V.21 On/Off (Must select low speed mode for operation)
0	1	1	A	Power Down. To power up, device must be reset.
Tone Mode:				
1	1/0	0	0	Dial 0
1	1/0	0	1	Dial 1
1	1/0	0	2	Dial 2
1	1/0	0	3	Dial 3
1	1/0	0	4	Dial 4
1	1/0	0	5	Dial 5
1	1/0	0	6	Dial 6
1	1/0	0	7	Dial 7
1	1/0	0	8	Dial 8
1	1/0	0	9	Dial 9
1	1/0	0	A	Dial *
1	1/0	0	B	Dial #
1	1/0	0	C	Output 550 Hz and Insert 550 Hz Notch in Low-Band Filter
1	1/0	0	D	Output 1800 Hz and Insert 1800 Hz Notch in Low-Band Filter
1	1/0	0	E	Row Disable On/Off
1	1/0	0	F	Column Disable On/Off

TABLE 1. DEFINITION OF I/O CODES (Cont.)

WLS1		WLS0	Word Length
0	0	0	8 Bits
0	1	1	9 Bits
1	0	0	10 Bits (default)
1	1	1	11 Bits
TLC1		TLC0	Transmitter Output Level (dBm) at the Phone Line
0	0	0	-14 (default)
0	1	1	-12
1	0	0	-10
1	1	1	-8
ALC1		ALC0	Audio Output Level
0	0	0	Output Off (default)
0	1	1	12 dB Attenuation
1	0	0	6 dB Attenuation
1	1	1	No Attenuation

2. Information from the Modem IC

Data is read serially from the modem when RD is low, on rising edges of the SCK clock. (See Figure 1 for read cycle waveforms.) Up to four data bits (D0--D3) can be read as defined below:

D0 Energy Detect 0 - No Energy 1 - Energy Present

In the CPM mode, the energy detector is connected to the output of the high-band filter, if ALB is off, or the scaled low-band filter, if ALB is on.

D1 Received Data (FSK) 1 - Mark 0 - Space

D2 Received Data (PSK) 1 - Mark 0 - Space

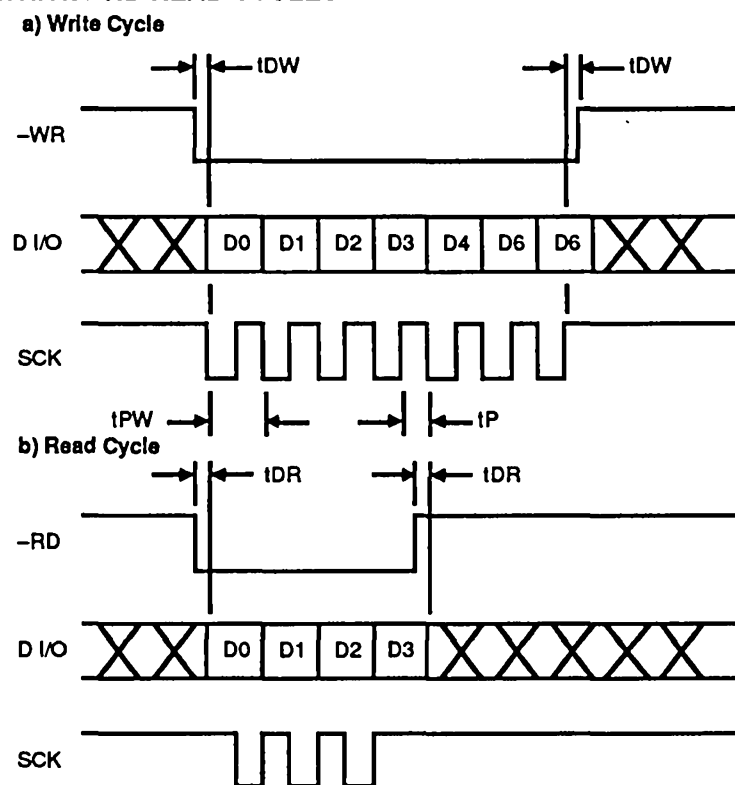
D3 Unscrambled Mark 1 - Detected 0 - Not Detected

Notes:

1. Default values for the operating modes on power-up are those shown to the right of the "/" unless otherwise specified.
2. Data is shifted in and out of the modem with LSB first.

TABLE 2. AC CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Units	Conditions
tDW	Delay Time to Write	200			ns	
tDR	Delay Time to Read	200			ns	
tPW	Complete SCK Cycle	1.0			ms	
tP	SCK High Pulse Duration	30		70	%	Duty Cycle
fC	Crystal Frequency	7.3721	7.3728	7.3735	MHz	

FIGURE 1. WAVEFORMS FOR WRITE AND READ CYCLES

DTMF GENERATOR CRYSTAL FREQUENCY = 7.372800 MHz \pm 0%

Parameter	Nominal Frequency	Allowable Error	Actual Error
Row 1	697 Hz	$\pm 1\%$	+ 0.17%
Row 2	770 Hz	$\pm 1\%$	- 0.26%
Row 3	852 Hz	$\pm 1\%$	+ 0.16%
Row 4	941 Hz	$\pm 1\%$	- 0.47%
Column 1	1209 Hz	$\pm 1\%$	- 0.74%
Column2	1336 Hz	$\pm 1\%$	-0.89%
Column 3	1477 Hz	$\pm 1\%$	- 0.01%
Guard Tones	550 Hz	± 20 Hz	- 1.4 Hz
	1800 Hz	± 20 Hz	+ 7 Hz

DTMF GENERATOR (Cont.)

Parameter	Conditions	Min	Typ	Max	Units
Second Harmonic Distortion	VCC = + 5 V		- 40		dB
Row Output Level	VSS = - 5 V		0		dBm
Column Output Level	TLC0 = 1		2		dBm
550 Hz Guard Tone Level	TLC1 = 1		- 3		dB (Note 2)
1800 Hz Guard Tone Level	Measured at TXOUT Pin		- 6		dB (Note 2)

Note: Guard tone levels are referenced to the TX signal level. When guard tones are added, the TXOUT level is adjusted to maintain a constant level on the line. For 1800 Hz, the adjustment is -0.97 dB; for 550 Hz, the adjustment is -1.76 dB, per the CCITT specification.

MODEM TRANSMIT SIGNALS CRYSTAL FREQUENCY = 7.372800 MHz \pm 0%

Mode		Bell 103		CCITT V.21		Bell 212A / CCITT V.22	
		Nominal	Actual	Nominal	Actual	Nominal	Actual
Answer	Mark	2225 Hz	2226 Hz	1650 Hz	1649.4 Hz	2400 Hz	2400 Hz
	Space	2025 Hz	2024.4 Hz	1850 Hz	1850.6 Hz		
Originate	Mark	1270 Hz	1269.4 Hz	980 Hz	978.34 Hz	1200 Hz	1200 Hz
	Space	1070 Hz	1070.4 Hz	1180 Hz	1181.53 Hz		
Calling Tone				1300 Hz	1301.7 Hz	1300 Hz	1301.7 Hz
Answer Tone				2100 Hz	2096.9 Hz	2100 Hz	2096.9 Hz

RECEIVER

Parameter	Conditions	Min	Typ	Max	Units
Input Signal Range	At RXA1 (pin 9)	- 45		0	dBm
Intra - Character Bit Rate	At RXD (pin 13)	1170	1200	1224	bps
Carrier Detect	At RXA1 (pin 9)	- 48		- 43	dBm
Carrier Detect Hysteresis		2			dB
Carrier Detect Delay	For 103, 212A and V.22	10	20	30	ms
Carrier Detect Hold	For 103, 212A and V.22	15	20	24	ms
Carrier Detect Delay	For V.21 mode	15	30	40	ms
Carrier Detect Hold	For V.21 mode	20	30	50	ms

TRANSMITTER

Parameter	Conditions	Min	Typ	Max	Units
Input Character Length	Start Bit + Data Bit + Stop Bit	8		11	bits
Intra - Character Bit Rate	At TXD (pin 14)	1170	1200	1212	bps
Input Break Sequence Length	M = Character Length	2M + 3			bits
Output Level Tolerance			± 1		dB

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature
Under Bias: -10°C to +80°C

Storage Temperature
Range: -65°C to +140°C

Maximum Supply
Voltage: VCC = +7.0 V

Input Voltage Range:
Anal. Pins; AGND -0.6 V to VCC+0.6 V
Digital Pins; DGND -0.6 V to VCC+0.6 V

Maximum Power
Dissipation @25°C: 500 mW

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional Operation of this device at these or any other conditions above

those in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may effect device reliability.

DC CHARACTERISTICS TA= 0°C to 70° C unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Units	Conditions
VCC	Positive Supply Voltage	4.5	5.0	5.5	V	
ICC	Quiescent Current		15		mA	VCC = 5 V
VIH	High Level Input Voltage	2.0			V	Digital Signal Pins: -RD, -WR, DI/O, SCK, TXCK1, TXD
VIL	Low Level Input Voltage			0.8	V	Digital Signal Pins: -RD, -WR, DI/O, SCK, TXCK1, TXD
VOH	High Level Output Voltage	4.0 2.0			V V	@IOH= 40 µA (D S Pins: D I/O, CKOUT, RXD, TXCK0, RXCK) @IOH= 500 µA
VOL	Low Level Output Voltage			0.4	V	@IOL=160 µA (D S Pins: D I/O, CKOUT, RXD, TXCK0, RXCK)
VOM	Maximum Output Signal	3.0			Vp-p	TXOUT, RL=1200 Ω (TLC1=1, TLC0=0)
VOM	Maximum Output Signal	1.0			Vp-p	Audio Out, RL= 50 kΩ
VIM	Maximum Input Signal			2.5	Vp-p	RXA1, RXA2

HIGH SPEED PARALLEL BUS MODEM CONTROLLER WITH AUTOMATIC MODEM POWER DOWN CONTROL

FEATURES

- Direct interface to VL7C412 single-chip, single-supply modems
- Complete Hayes AT command set in firmware
- Built-in UART
- Direct IBM PC bus interface
- IORDY pin for use on high-speed buses
- Complete intelligent modem in two ICs
- Compatible with industry-standard software
- Automatic power up/down control of VL7C412
- Replacement for Sierra SC11037

DESCRIPTION

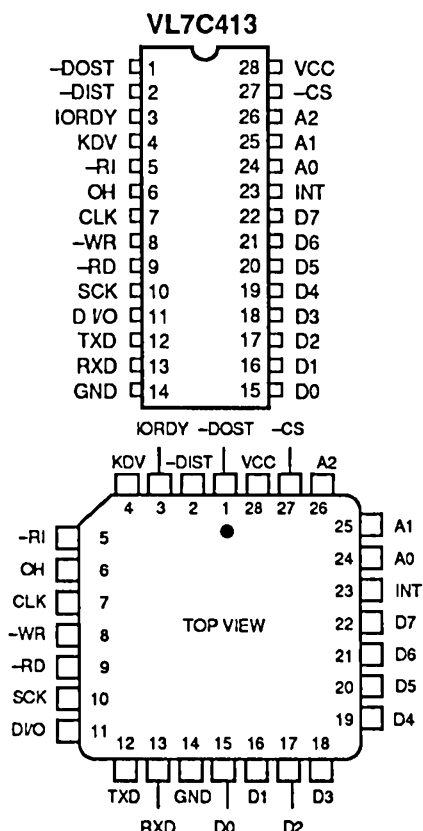
The VL7C413 Parallel Bus Modem Controller is specifically designed to control the VL7C412 single-chip, 300/1200 bit-per-second modem. Built with an advanced two-micron CMOS process, the VL7C413 provides a highly cost effective solution for interfacing a modem IC to a system bus. When connected to the VL7C412, with the addition of a data access arrangement (DAA), the VL7C413 implements a Hayes-type smart modem for board-level, integral-modem applications. Because the VL7C413 fully emulates the functionality of the VL82C50 UART and includes data bus transceivers, it can be directly interfaced to a computer's parallel data

bus (in particular to the bus of the IBM PC, XT or AT). All of the popular communications software written for the PC will work with the VL7C413/VL7C412 chip set. In addition to including the functionality of the VL82C50 UART, the VL7C413 contains an 8-bit microprocessor, 8K by 8 bits of ROM and 128 by 8 bits of RAM.

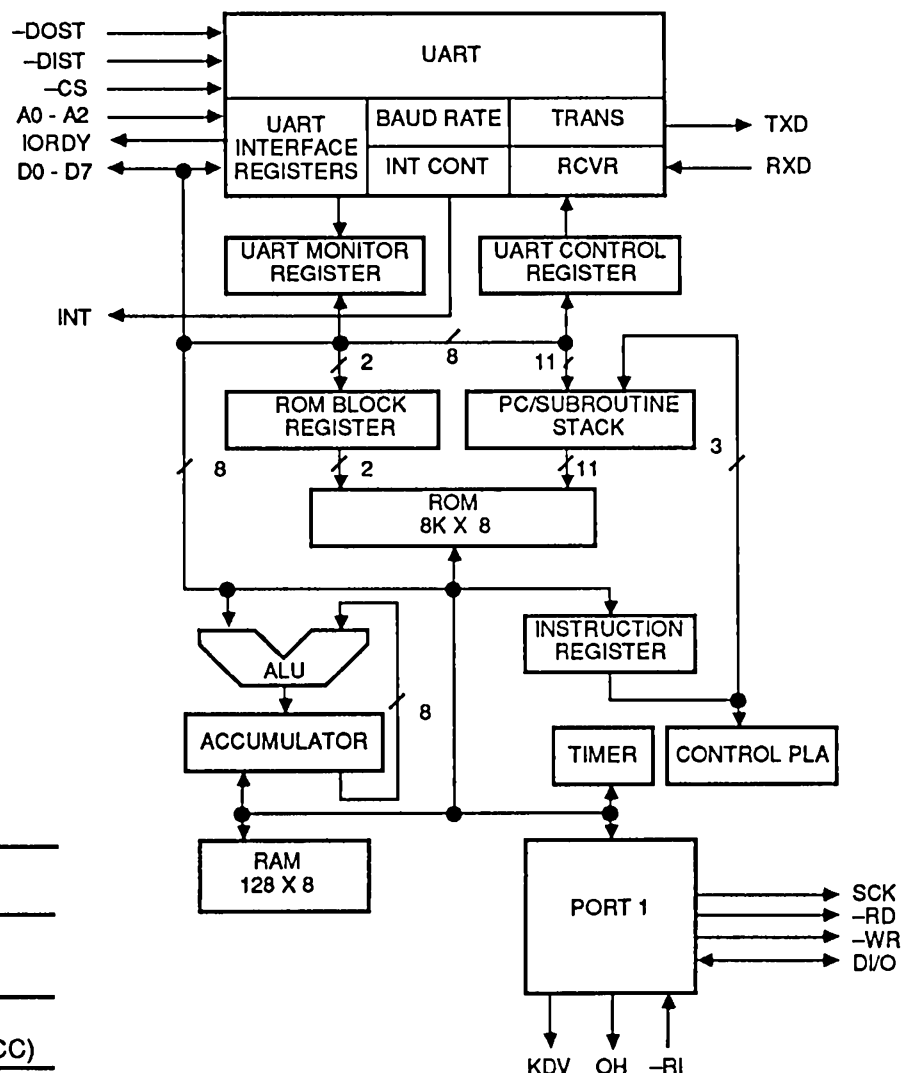
The VL7C413 automatically controls the power up/down feature of the VL7C412 to maintain lowest possible system power consumption.

For specific high-volume applications, the control program can be modified by VLSI to include additional command functions.

PIN DIAGRAMS



BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Package
VL7C413-PC	Plastic DIP
VL7C413-QC	Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range is 0°C to +70°C.

SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Description
-DOST	1	The CPU can write data or control words into a selected register of the VL7C413 when -DOST is low and the chip is selected. Data is latched on the rising edge of the signal.
-DIST	2	The CPU can read data or status information from a selected register of the VL7C413 when -DIST is low and the chip is selected.
IORDY	3	This open-drain output will go low upon a write or read operation, and remain low until internal data setup and hold times have been satisfied.
KDV	4	This output controls the operation of the data/voice relay. When low, the data/voice relay is off and the phone line is connected to the phone set. During a data call, the VL7C413 makes this output high to operate the data/voice relay, disconnecting the phone set from the phone line. It may also be used to drive a relay for multi-line phone applications to close the A and A1 leads.
-RI	5	The output of the ring detector in the DAA is connected to this input. A low level on this input indicates the "On" duration of the ring cycle. This is a Schmitt-trigger input, allowing for slow rising and falling signals on this pin.
OH	6	This output controls the operation of the hookswitch relay in the DAA. During a data call, this output is high. It operates the hookswitch relay which causes the phone line to be seized. During rotary dialing, the VL7C413 pulses this output at a rate of 10 pulses per second with appropriate Mark/Space ratio depending on 212A or V.22 mode.
CLK	7	A 7.3728 MHz clock signal must be connected to this input. Normally, the CKOUT pin of the VL7C412 modem is connected to this pin. All internal timing is derived from this clock. This clock must be adjusted to within 0.01%.
-WR	8	This pin is used to initiate writing of data to the VL7C412 modem. On power-up, it is an input for a brief time in which the VL7C413 reads the carrier status switch connected to this pin. If the switch is closed to ground through an 18 K Ω resistor, the VL7C413 sets the Received Line Signal Detect (RLSD) Bit in the Modem Status Register. If the switch is open, the VL7C413 resets this bit and writes the actual status of the carrier detector during a data call. If no switch is used, an internal pull-up sets the status during power-up to the default state (pull-up to VCC) which is to follow the remote modem's carrier.
-RD	9	This pin is used to initiate reading of data from the VL7C412 modem. On power-up, this pin is an input for a brief time in which the VL7C413 reads the DTR status switch connected to this pin. If this switch is open, the VL7C413 reacts to the status of the DTR bit in the UART Modem Control Register. If the switch is closed to ground through 18 k Ω , the VL7C413 ignores the state of the DTR bit. When the switch is open, writing a zero to the DTR bit in the Modem Control Register forces the VL7C413 into the command state and when on-line, causes it to hang up. If no switch is used, an internal pull-up to VCC sets the status during power-up to the default state (to follow the DTR status).
SCK	10	The VL7C413 supplies a shift clock on this pin to the VL7C412 modem for reading or writing data. On power-up, this pin is an input for a brief time in which the VL7C413 reads the Bell/CCITT select switch connected to this pin. If this switch is open, Bell protocol is selected. If this switch is closed to ground through 18 k Ω , CCITT V.22 protocol is selected. If no switch is used, an internal pull-up sets the status during power-up to the default state (212A mode).
DI/O	11	The VL7C413 shifts data serially out of this pin to VL7C412 during a write operation and shifts data serially into this pin during a read operation from the VL7C412. On power-up this pin is an input for a brief time in which the VL7C413 reads the Make/Break ratio select switch connected to this pin for selecting the pulse dialing standard. With the switch open, the Bell standard 39% Make, 61% Break is selected. With the switch closed to ground through 18 k Ω , the CCITT standard 33% Make, 67% Break is selected. If no switch is used, an internal pull-up sets the status during power-up to the default state (Bell standard).

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Description
TXD	12	This pin is a serial output pin. During a data call, after the connection is established, the VL7C413 converts parallel data received from the computer bus and outputs it in a serial, asynchronous format to the VL7C412 modem for modulation. At all other times the VL7C413 holds this output in the Mark (high) condition.
RXD	13	Demodulated data from the VL7C412 modem is received on this pin during a data call. A high level is considered Mark and a low level is Space. The VL7C413 converts the serial data into a parallel data byte and stores it in the Receiver Buffer Register (RBR). The Data Ready bit in the Line Status Register (LSR) is then set, and an appropriate interrupt identification code is written in the Interrupt Identification Register (IIR) to signal to the computer, the reception of a new data byte.
GND	14	Ground reference (0 V).
D0-D7	15-22	This is the 8 bit data bus comprising of three-state input/output lines. This bus provides bidirectional communication between the VL7C413 and the CPU. Data control words and status information are transferred via the D0 - D7 data bus.
INT	23	This output goes high whenever any one of the following interrupt types has an active condition and is enabled via the IER: Receiver Line Status flag, Received Data Available, Transmitter Holding Register Empty, and Modem Status. It is reset low upon the appropriate interrupt servicing. The INT pin is forced to a high impedance state when the OUT2 bit of the Modem Control Register (MCR) is low (power on state).
A0-A2	24-26	These three address inputs are used during read or write operation to select a UART register in the VL7C413 as shown in Table 1. The Divisor Latch Access Bit (DLAB) must be set high by the system software to access the bit rate divisor latches as shown in Table 2.
-CS	27	The VL7C413 is selected when this input is low. When high, the VL7C413 forces the Data bus lines into a high impedance state.
VCC	28	Positive supply (+5 V).

TABLE 1. VL7C413 UART REGISTERS

DLAB	A2	A1	A0	Mnemonic	Register
0	0	0	0	RBR	Receiver Buffer Register (read only)
0	0	0	0	THR	Transmitter Holding Register (write only)
0	0	0	1	IER	Interrupt Enable Register
X	0	1	0	IIR	Interrupt Identification Register (read only)
X	0	1	1	LCR	Line Control Register
X	1	0	0	MCR	Modem Control Register
X	1	0	1	LSR	Line Status Register
X	1	1	0	MSR	Modem Status (read only) Register
X	1	1	1	STR	Speed
1	0	0	0	DLL	Divisor Latch (LSB) (write only)
1	0	0	1	DLM	Divisor Latch (MSB) (write only)

X = "Don't Care"

0 = Logic Low

1 = Logic High

FIGURE 1. UART BLOCK DIAGRAM

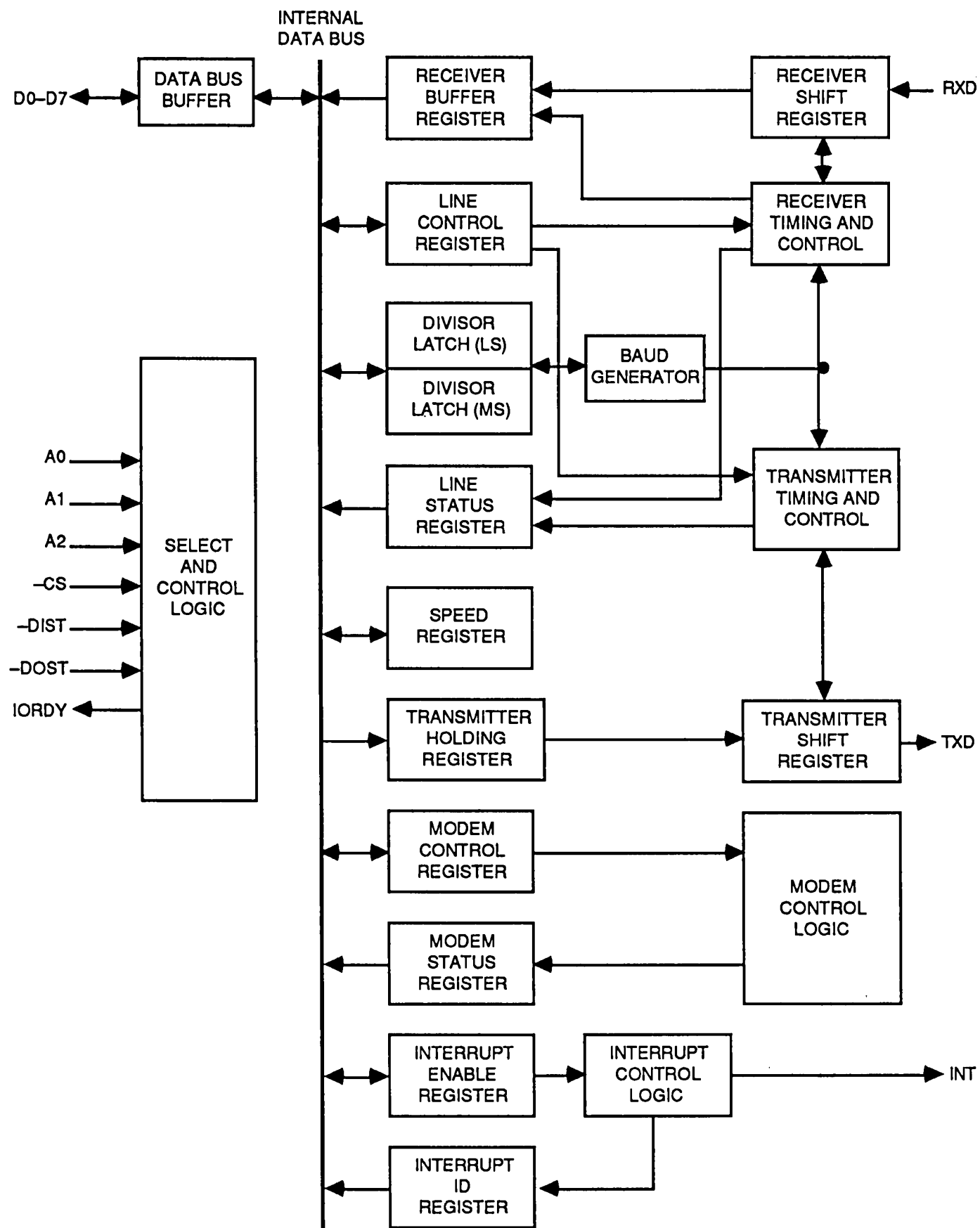


TABLE 2. VL7C413 UART REGISTER FUNCTION SUMMARY

Register Mnemonic	Register Bit Number							
	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
RBR	Data	Data	Data	Data	Data	Data	Data	Data
THR	Data	Data	Data	Data	Data	Data	Data	Data
IER	Receive Data Available Interrupt Enable	THRE Interrupt Enable	Receive Line Status Interrupt Enable	Modem Status Interrupt Enable	0	0	0	0
IIR	0 If Interrupt Pending	Interrupt ID Bit 0	Interrupt ID Bit 1	0	0	0	0	0
LCR	0 = 7 Bit Data 1 = 8 Bit Data	1	0 = 1 Stop Bit 1 = 2 Stop Bits	1 = Parity Enable	1 = Even Parity	1 = Stick Parity	1 = Set Break	DLAB
MCR	Data Terminal Ready	Request to Send	OUT1	OUT2 0 = INT Output to HI-Z	No Function	0	0	0
LSR	Data Ready	Overrun Error	Parity Error	Framing Error	Break Interrupt	THRE	TSRE	0
MSR	0	0	Trailing Edge Ring	Delta RLSD	1 (CTS)	1 (DSR)	RING	RLSD
DLM	Data	Data	Data	Data	Data	Data	Data	Data
DLL	Data	Data	Data	Data	Data	Data	Data	Data
STR	Data	Data	Data	Data	Data	Data	Data	Data

TABLE 3. VL7C413 SOFTWARE REGISTERS

Register	Range/Units	Description	Default
S0	0-255 Rings	Ring to answer telephone on	0
S1	0-255 Rings	Number of rings	0
S2	0-127 ASCII	Escape code character	43 (+)
S3	0-127 ASCII	Character recognized as carriage return	13 (CR)
S4	0-127 ASCII	Character recognized as line feedback	10 (LF)
S5	0-32, 127 ASCII	Character recognized as back space	8 (BS)
S6	2-255 sec.	Wait time for dial tone	2
S7	1-255 sec.	Wait time for carrier	30
S8	0-255 sec.	Pause time (caused by comma)	2
S9	1-255 1/10 sec.	Carrier detect response time	6
S10	1-255 1/10 sec.	Delay between loss of carrier and hang up	7
S11	50-255 millisec.	Duration and spacing of Touch-Tones	70
S12	20-255 1/50 sec.	Escape code guard time	50
S13	bit mapped	UART status register	-
S14	bit mapped	Option register	-
S15	bit mapped	Flag register	-
S16	0, 1, 2, 4	Test modes	0

TABLE 4. COMMAND SUMMARY
PREFIX, REPEAT AND ESCAPE COMMANDS

Command	Description (Notes 1 & 2)
AT	Attention prefix: precedes all command lines except + + + (escape) and A/(repeat) commands
A/	Repeat last command line (A/ is not followed by carriage return)
+ + +	Escape code: go from on-line state to command state (one second pause before and after escape code entry; ; + + + is not followed by carriage return)

DIALING COMMANDS

Command	Description (Notes 1 & 2)	Command	Description (Notes 1 & 2)
D	Dial	/	Wait for 1/8 second
P	Pulse*	@	Wait for silence
T	Touch-Tone	W	Wait for second dial tone
,	Pause	;	Return to command state after dialing
!	Flash	R	Reverse mode (to call originate-only modem)

OTHER COMMANDS

Commands	Description (Notes 1 & 2)	Commands	Description (Notes 1 & 2)
A	Answer call without waiting for ring	M1	Speaker on until carrier detected*
B/B0	CCITT V.22 mode (Note 3)	M2	Speaker always on
B1	Bell 103 and 212A mode*	O	Go to on-line state
C/C0	Transmit carrier off	O1	Remote digital loopback off*
C1	Carrier on*	O2	Remote digital loopback request
E/E0	Characters not echoed	Q/Q0	Result codes displayed*
E1	Characters echoed*	Q1	Result codes not displayed
F/F0	Half duplex	Sr?	Requests current value of register r
F1	Full duplex*	Sr = n	Sets register r to value of n
H/H0	On hook (hang up)	V/V0	Digit result codes
H1	Off hook; line and auxiliary relay	V1	Word result codes*
H2	Off hook; line relay only	X/X0	Compatible with Hayes-type 300 modems*
I/I0	Request product ID code (130)	X1	Result code CONNECT 1200 enabled
I1	Firmware revision number	X2	Enables dial tone detection
I2	Test internal memory	X3	Enables busy signal detection
L/L1	Low speaker volume	X4	Enables dial tone and busy signal detection
L2	Medium speaker volume	Y/Y0	Long space disconnect disabled*
L3	High speaker volume	Y1	Long space disconnect enabled
M/M0	Speaker always off	Z	Software reset: restores all default settings

Notes:

1. Default modes are indicated by *.
2. Commands entered with null parameters assume 0 - X is the same as X0.
3. When the ATB command is used in the answer mode, the VL7C412 is placed in either the V.21 or the V.22 mode, depending on the response from the remote modem. In the originate mode, the VL7C413 will sense if the baud rate is set at 300 or 1200 bits per second and will adjust the VL7C412 accordingly.

TABLE 5. RESULT CODES

Digit Code	Word Code	Description
0	OK	Command executed
1	Connect	Connected at 300 or 1200 bps Connected at 300 bps, if result of X1, X2, X3, or X4 command
2	Ring	Ringing signal detected (Note)
3	No Carrier	Carrier signal not detected or lost
4	Error	Illegal command Error in command line Command line exceeds buffer (40 characters, including punctuation) Invalid character format at 1200 bps
5	Connect 1200	Connected at 1200 bps. Results from X1, X2, X3, or X4 commands only
6	No Dialtone	Dialtone not detected and subsequent commands not processed Results from X2 or X4 commands only
7	Busy	Busy signal detected and subsequent commands not processed Results from X3 or X4 commands only
8	No Answer	Silence not detected and subsequent commands not processed Results from @ command only

Note: When the VL7C413 detects a ringing on the telephone line, it sends a RING result code. However, the VL7C413 will answer the call only if it is in auto-answer mode or is given an A command.

TABLE 6. RESET CONTROL OF REGISTERS AND PINOUT SIGNALS

Register/Signal	Reset Control	Reset State
Receiver Buffer Register	First word received	Data
Transmitter Holding Register	Writing into the Transmitter Holding Register	Data
Interrupt Enable Register	Power on reset	All bits low
Interrupt Identification Register	Power on reset	Bit 0 high; bits 1–7 low
Line Control Register	Writing into the LCR	Data
MODEM Control Register	Power on reset	All bits low
Line Status Register	Power on reset	Bits 0–4, 7 low; bits 5–6 high
Modem Status Register	Power on reset	Bits 0–3, 6–7 low; bits 4–5 high
Divisor Latch (high order bits)	Power on reset	1200 bps
TXD	Master reset	High
INT	Power on reset	Low (high impedance)

UART REGISTERS

Line Control Registers

This register controls the format of the asynchronous data communications.

Bit 0 and 1: Bit 1 is always high. Bit 0 specifies the number of bits in each transmitted or received serial character.

The encoding of bit 0 is as follows:

Bit 1	Bit 0	Word Length
1	0	7 Bits
1	1	8 Bits

Bit 2: This bit specifies the number of Stop bits in each transmitted or received serial character. If bit 2 is a logic 0, one Stop bit is generated or checked in the transmit or receive data, respectively. If bit 2 is a logic 1, when 7-bit word length with no Parity is selected, two Stop bits are generated or checked.

Bit 3: This bit is the Parity Enable bit. When bit 0 is a logic 0 and bit 3 is a logic 1, a Parity bit is generated (transmit data) or checked (receive data) between the last data word bit and the Stop bit of the serial data. (The Parity bit is used to produce an even or odd number of 1s when the data word bits and the Parity bit are summed.)

Bit 4: This bit is the Even Parity Select bit. When bit 3 is a logic 1 and bit 4 is logic 0, and odd number of logic 1s is transmitted or checked in the data word bits and Parity bit. When bit 3 is logic 1 and bit 4 is a logic 1, an even number of bits is transmitted or checked.

Bit 5: This bit is the Stick Parity bit. When bit 3 is logic 1 and bit 5 is logic 1, the Parity bit is transmitted and then detected by the receiver in the opposite state indicated by bit 4.

Bit 6: This bit is the Set Break Control bit. When bit 6 is a logic 1, the serial output (TXD) is forced to the Spacing state (logic 0) and remains there (until reset by a low-level bit 6) regardless of other transmitter activity. The feature enables the CPU to alert a terminal in a computer communications system.

Bit 7: This bit is the Divisor Latch Access Bit (DLAB). It must be set high (logic 1) to access the Divisor Latches of the Baud Rate Generator during a Read or Write operation. It must be set low (logic 0) to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

Programmable Baud Rate Generator

The VL7C413's Baud Rate Generator can be programmed for one of six baud rates. The desired speed is selected by writing into the Divisor Latch (DLM). On reset, the rate will be 1200 baud.

DLM (Hex Code)	Baud Rate
00	1200
01	300
03	150
04	110
06	75
09	50

Line Status Register

This 8-bit register provides status information to the CPU concerning the data transfer. The contents of the Line Status Register are indicated in Table 2 and are described below:

Bit 0: This bit is the receiver Data Ready (DR) indicator. Bit 0 is set to a logic 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register. Bit 0 will reset to a logic 0 either by the CPU reading the data in the Receiver Buffer Register or by writing a logic 0 into it from the CPU.

Bit 1: This bit is the Overrun Error (OE) indicator. Bit 1 indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.

Bit 2: This bit is the Parity Error (PE) indicator. Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even parity select bit. The PE bit is set to a logic 1 upon detection of parity error and is reset to a logic 0 whenever the CPU reads the contents of the Line Status Register.

Bit 3: This bit is the Framing Error (FE) indicator. Bit 3 indicates that the received character did not have a valid Stop bit. Bit 3 is set to a logic 1 whenever the Stop bit following the last data bit or parity bit is detected as a zero (Spacing level).

Bit 4: This bit is the Break Interrupt (BI) indicator. Bit 4 is set to a logic 1

whenever the received data input is held in the Spacing (Logic 0) state for longer than a full word transmission time - the total time of Start bit + data bits + Parity + Stop bits.

Bit 5: This bit is the Transmitter Holding Register Empty (THRE) indicator. Bit 5 indicates that the VL7C215 is ready to accept a new character for transmission. In addition, this bit causes the VL7C215 to issue an interrupt to the CPU when the Transmit Holding Register Empty enable is set high. The THRE bit is set to a logic 0 concurrently with the loading of the Transmitter Holding Register by the CPU.

Bit 6: This bit is the Transmitter Shift Register Empty (TSRE) indicator. Bit 6 is set to a logic 1 whenever the Transmitter Shift Register is idle. It is reset to logic 0 upon a data transfer from the Transmitter Holding Register to the Transmitter Shift Register.

Bit 7: This bit is permanently set to logic 0.

Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected.

Interrupt Identification Register

The VL7C413 has an on-chip interrupt capability that allows for complete flexibility in interfacing to all popular microprocessors. To provide minimum software overhead during data character transfers, the VL7C413 prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows: Receiver Line Status (priority 1); Received Data Ready (priority 2); Transmitter Holding Register Empty (priority 3); and MODEM Status (priority 4).

Information indicating that a prioritized interrupt is pending the source of that interrupt are stored in the Interrupt Identification Register (refer to Table 7). The Interrupt Identification Register (IIR), when addressed during chip-select time, freezes the highest priority interrupt pending and no other interrupts are acknowledged until the particular interrupt is serviced by the CPU. The contents of the IIR are indicated in Table 2 and are described below.

Bit 0: This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When bit 0 is a logic, no interrupt is pending.

Bits 1 and 2: These two bits of the IIR are used to identify the highest priority interrupt pending as indicated in Table 7.

Bits 3 through 7: These five bits of the IIR are always logic 0.

Interrupt Enable Register

This 8-bit register enables the four interrupt sources of the VL7C413 to separately activate the Interrupt (INT) output signal. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the Interrupt Enable Register. Similarly, by setting the appropriate bits of this register and the active (high) INT output from the chip. All other system functions operate in their normal manner, including the setting of the Line Status and MODEM Status Register. The contents of the Interrupt Enable Register are indicated in Table 2 and are described below.

Bit 0: This bit enables the Received Data Available Interrupt when set to logic 1.

Bit 1: This bit enables the transmitter Holding Register Empty Interrupt when set to a logic 1.

Bit 2: This bit enables the Receiver Line Status Interrupt when set to logic 1.

Bit 3: This bit enables the MODEM Status Interrupt when set to logic 1.

Bit 4 through 7: These four bits are always logic 0.

MODEM Control Register

This 8-bit register controls the interface with the MODEM. The contents of the MODEM Control Register are indicated in Table 2 and are described below.

Bit 0: This bit controls Data Terminal Ready (DTR) signal. If the external switch on the -RD pin is set to VCC through an 18 kΩ resistor, setting the DTR low will force the VL7C413 into the command state and if on line, it will hang up.

Bit 1: This bit controls the Request to Send (RTS) signal. This signal is not used by the VL7C413.

Bit 2: This bit controls the Output 1 (OUT1) signal. This signal is not used by the VL7C413.

Bit 3: This bit controls the Output 2 (OUT2) signal. When OUT2 is a 0, the interrupt output is in high impedance state.

Bit 4: Not used.

Bits 5 through 7: These bits are permanently set to logic 0.

MODEM Status Register

This 8-bit register provides the current state of the control lines from the

MODEM (or peripheral device) to the CPU. In addition to this current-state information, two bits of the MODEM Status Register provide change information. These bits are set to a logic 1 whenever a control input from the MODEM changes state. They are reset to logic 0 whenever the CPU reads the MODEM Status Register.

The contents of the MODEM Status Register are indicated in Table 2 and are described below.

Bits 0 and 1: These bits are always 0.

Bit 2: This bit is the Trailing Edge of Ring Indicator (TERI) detector. Bit 2 indicates that the -RI input to the chip has changed from On (logic 1) to an Off (logic 0) condition.

Bit 3: This bit is the Delta Received Line Signal Detector (DRLSD) indicator. Bit 3 indicates that the carrier detector has changed state.

Bit 4: This bit is always 1.

Bit 5: This bit is always 1.

Bit 6: This bit is the complement of the Ring Indicator (-RI) input.

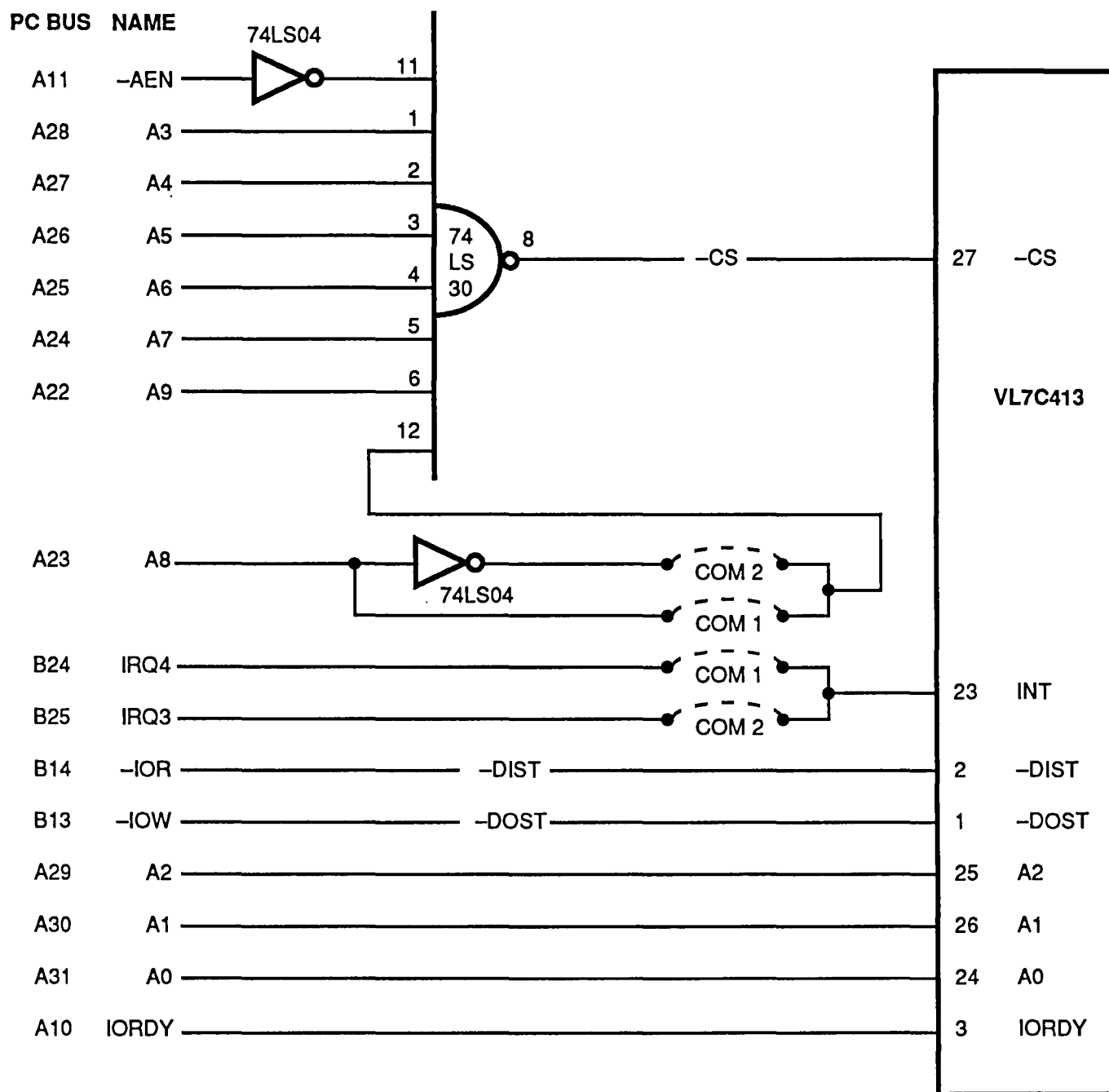
Bit 7: This bit is the Received Line Signal Detect (RLSD) signal.

Whenever bit 2 is set to logic 1, or bit 3 changes state, a MODEM Status Interrupt is generated if enabled.

TABLE 7. INTERRUPT CONTROL FUNCTIONS

Interrupt Identification Register			Interrupt Set and Reset Functions			
Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Flag	Interrupt Source	Interrupt Reset Control
0	0	1		None	None	
1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error or Framing Error or Break Interrupt	Reading the Line Status Register
1	0	0	Second	Received Data Available	Received Data Available	Reading the Receiver Buffer Register
0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR (if source of interrupt) or Writing into the Transmitter Holding Register
0	0	0	Fourth	MODEM Status	Ring Indicator or Received Line Signal Detect	Reading the MODEM Status Register

FIGURE 2. ADDRESS DECODER CIRCUIT



AC CHARACTERISTICS: TA = 0 TO 70°C, VCC = 5 V ±10%

Symbol	Parameter	Min	Max	Units	Conditions
tDIW	–DIST Strobe Width	300		ns	1TTL Load
tRC	Read Cycle Delay	300		ns	1TTL Load
RC	Read Cycle = tDIW + tRC + 20 ns	620		ns	1TTL Load
tDDD	Delay from –DIST to Data		300	ns	1TTL Load
tHZ	–DIST to Floating Data Delay	60		ns	1TTL Load
tDOW	–DOST Strobe Width	300		ns	1TTL Load
tWC	Write Cycle Delay	300		ns	1TTL Load
WC	Write Cycle = tDOW + tWC + 20 ns	620		ns	1TTL Load
tDS	Data Setup Time	60		ns	1TTL Load
tDH	Data Hold Time	60		ns	1TTL Load
tDIC	–DIST Delay from Select	150		ns	1TTL Load
tDOC	–DOST Delay from Select	150		ns	1TTL Load
tACR	Address and Chip Select Hold Time from –DIST	10		ns	1TTL Load
tACW	Address and Chip Select Hold Time from –DOST	1		ns	1TTL Load
tDIOR	–DIST/–DOST to IORDY Delay		TBD	ns	1TTL Load
tWIOR	IORDY Pulse Width	TBD		ns	1TTL Load
Receiver					
tRINT	Delay from –DIST (Read RBR) to Reset Interrupt		1	μs	100 pF Load
Transmitter					
tHR	Delay from –DOST (Write THR) to Reset Interrupt		1	μs	100 pF Load
tIRS	Delay from Initial INTR Reset to Transmit Start		1	Baud Cycle	
tSI	Delay from Initial Write to Interrupt		1	Baud Cycle	
tSS	Delay from Stop to Next Start		1	μs	
tSTI	Delay from Stop to Interrupt (THRE)		1	Baud Cycle	
tIR	Delay from –DIST (Read IIR) to Reset Interrupt (THRE)		1	μs	100 pF Load

Note: A TTL load is 40 μA sourced and -1.6 mA sinked current.

FIGURE 3. READ CYCLE TIMING

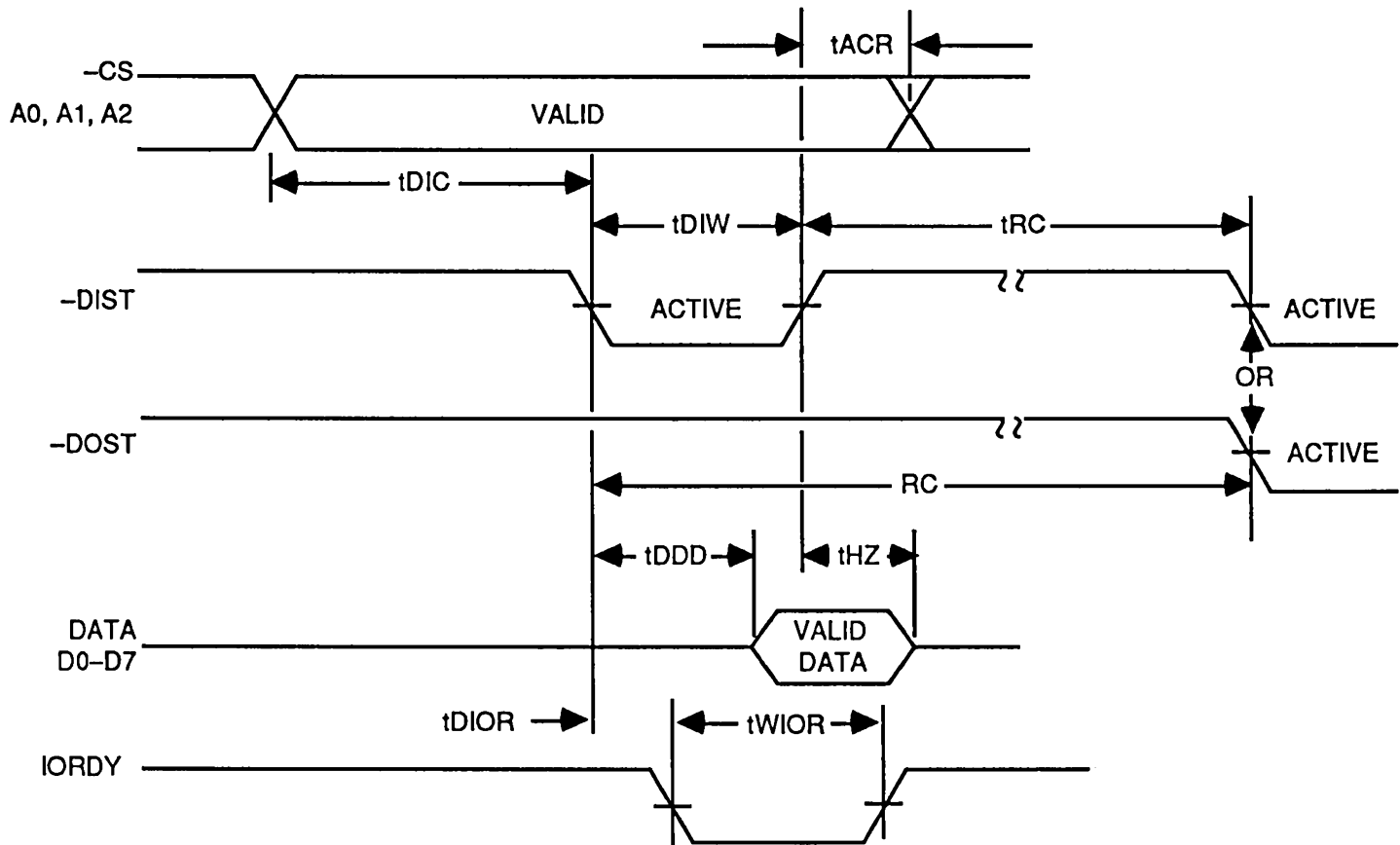


FIGURE 4. WRITE CYCLE TIMING

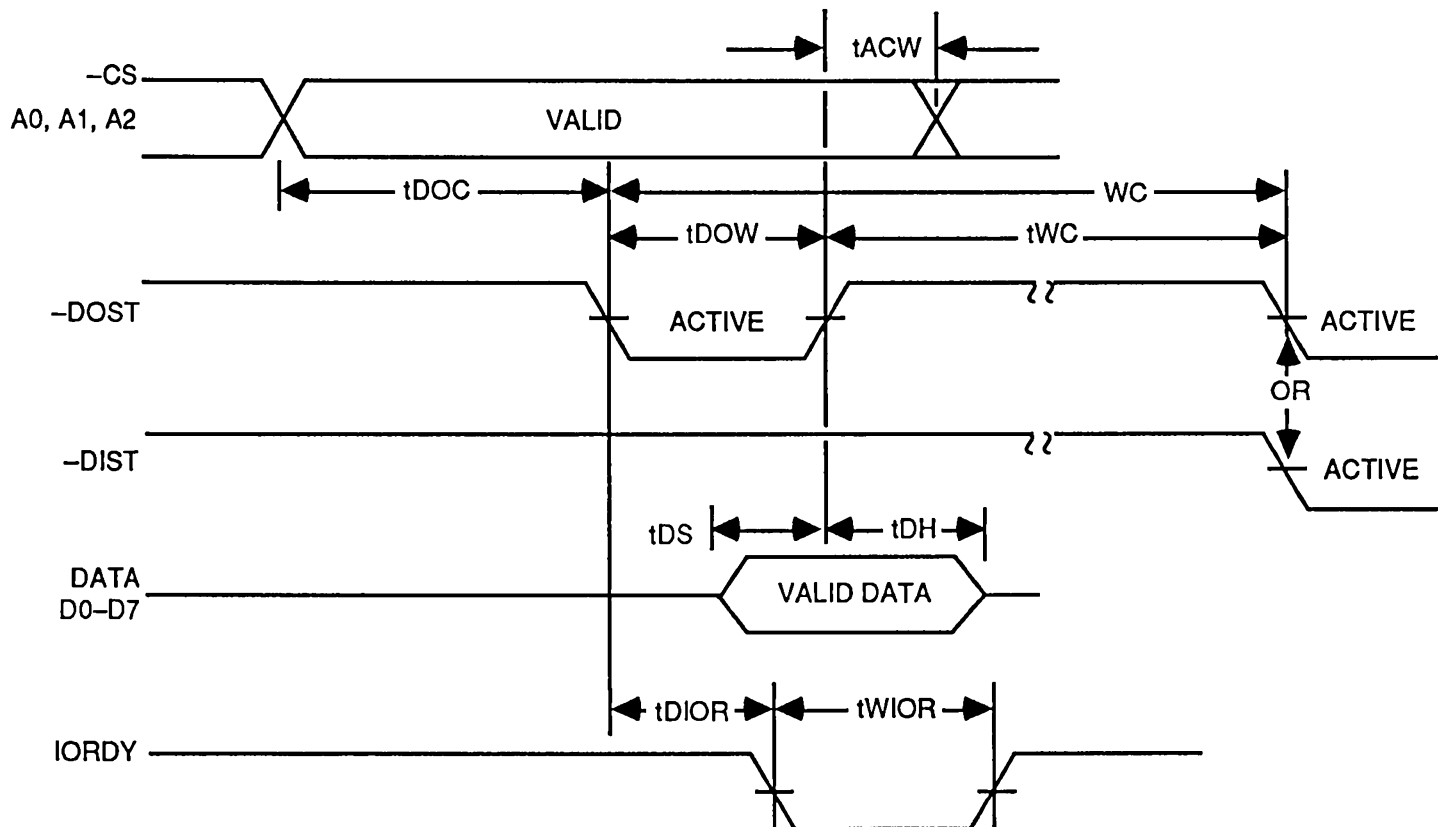


FIGURE 5. RECEIVER TIMING

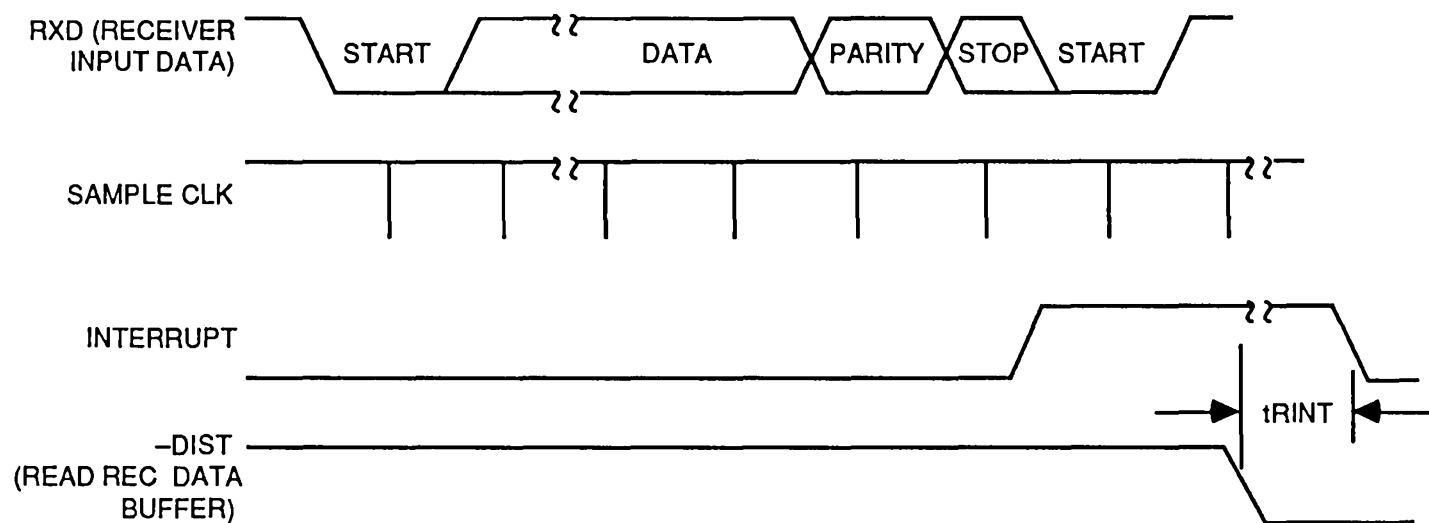
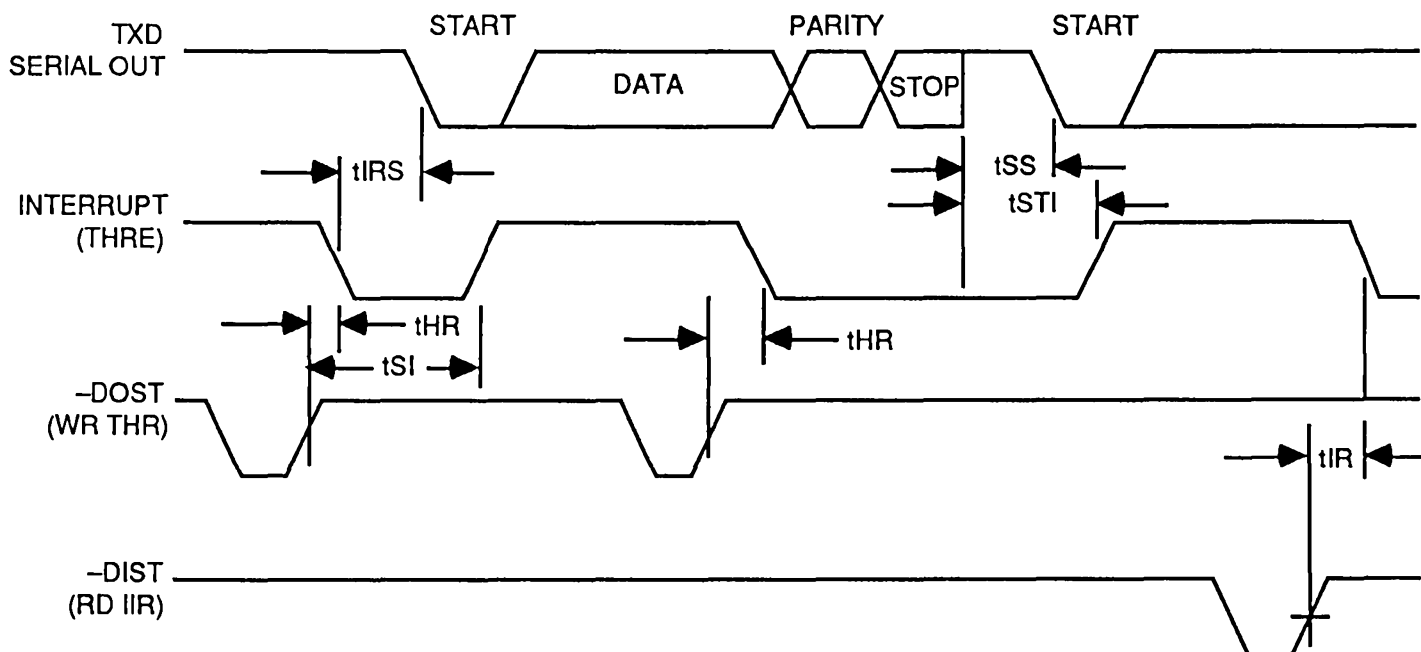


FIGURE 6. TRANSMITTER TIMING



ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature 0°C to +70°C
 Storage Temperature -65°C to +150°C
 Supply Voltage to Ground Potential +6 V
 Applied Input Voltage -0.6 V to VCC +0.6 V
 Power Dissipation 500 mW

Stresses above those listed may cause permanent damage to the device.
 These are stress ratings only, functional operation of this device at these or any other conditions above those indicated

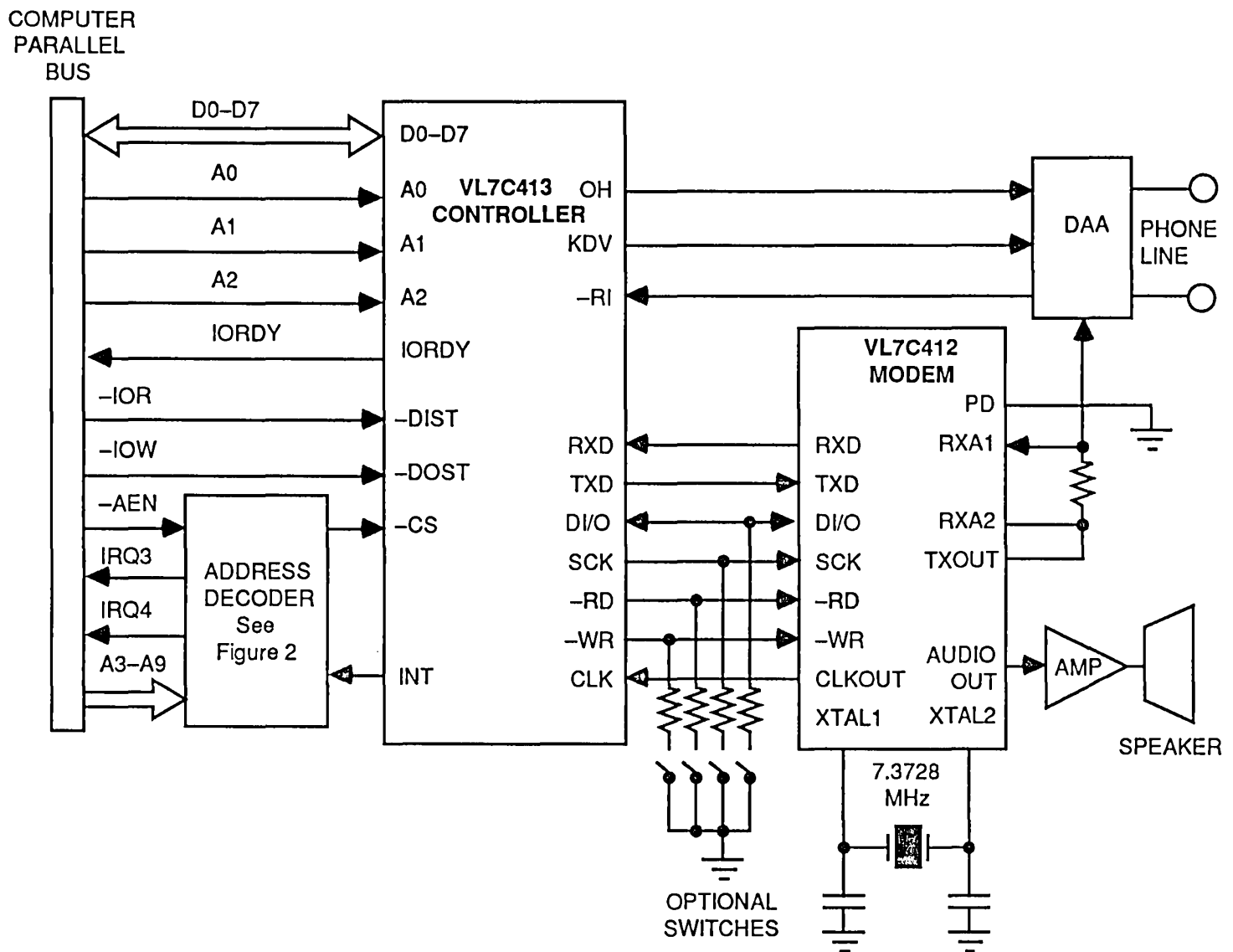
in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS: TA = 0 to +70 °C, VCC = 5 V ±10%

Symbol	Parameter	Min	Typ	Max	Units	Conditions
VCC	Positive Supply Voltage	4.5	5.0	5.5	V	
ICC	Operating Current		10.0		mA	@ VCC = 5 V
VIH	High Level Input Voltage	2.0			V	All pins except -RI
VIL	Low Level Input Voltage			0.8	V	All pins except -RI
VT+	Positive Hysteresis Threshold		2.5		V	-RI pin
VT-	Negative Hysteresis Threshold		1.8		V	-RI pin
VOH	High Level Output Voltage	VCC - 1.0			V	Digital signal pins D0 to D7 and INT @ IOH = -6 mA
		VCC - 1.0			V	All other output or I/O pins @ IOH = -2 mA
VOL	Low Level Output Voltage			0.4	V	Digital signal pins D0 to D7 and INT @ IOL = 6 mA
				0.4	V	All other output or I/O pins @ IOL = 2 mA
IL	Leakage Current (Note)		±1.0		μA	
FCLK	Clock Frequency	7.3721	7.3728	7.3735	MHz	

Note : This applies to all pins except TEST, which has an internal pull-down -WR, -RD, SCK, D/I/O and switch input pins which have internal pull-ups.

FIGURE 7. INTEGRAL SMART MODEM CONFIGURATION FOR PC BUS APPLICATIONS



VL7C414

STAND-ALONE MODEM INTERFACE CONTROLLER WITH AUTOMATIC MODEM POWER DOWN CONTROL

FEATURES

- Direct interface to VL7C412A single chip single-supply modems
- Complete Hayes AT command set in firmware
- Built-in UART for RS232C interface
- Two-micron CMOS process
- 28-pin DIP or PLCC package
- Complete intelligent modem in two ICs
- Compatible with industry-standard software
- Reduces board space and component count requirements
- Low power consumption
- Replacement for Sierra SC11028

DESCRIPTION

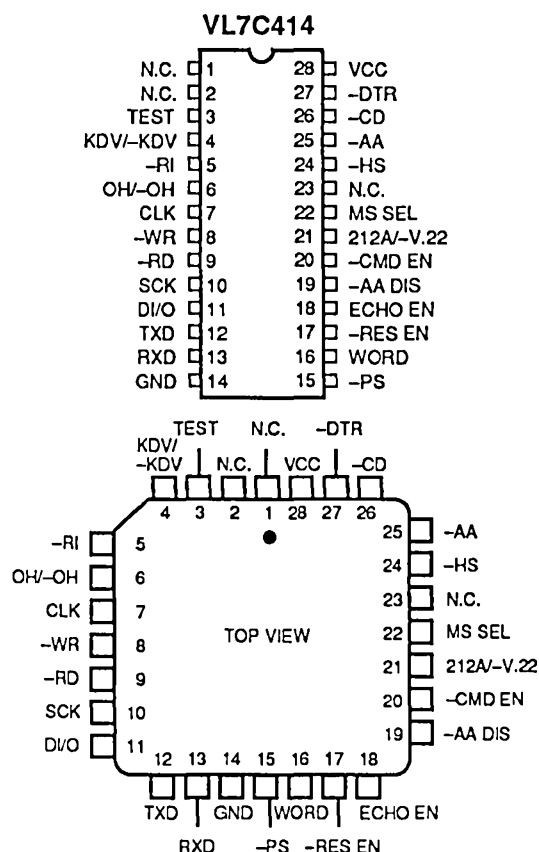
The VL7C414 Stand-Alone Modem Interface Controller is specifically designed to control the VL7C412A single-chip, 300/1200 bit-per-second modem. Built with an advanced two-micron CMOS process, the VL7C414 provides a highly cost effective solution for interfacing a modem IC to a computer's RS232C port. When connected to the VL7C412A, with the addition of a data access arrangement (DAA), the VL7C414 implements a Hayes-type smart modem for stand-alone modem applications. All of the popular communications software written for the IBM PC will work with the VL7C414/VL7C412A chip set. The

VL7C414 contains an 8-bit microprocessor, 8K by 8 bits of ROM and 128 by 8 bits of RAM. In order to support the stand-alone functionality of the device, an 8-bit switch input port allows immediate user access and manual control of the system. Either Bell 103 or CCITT V.22 may be selected in this manner.

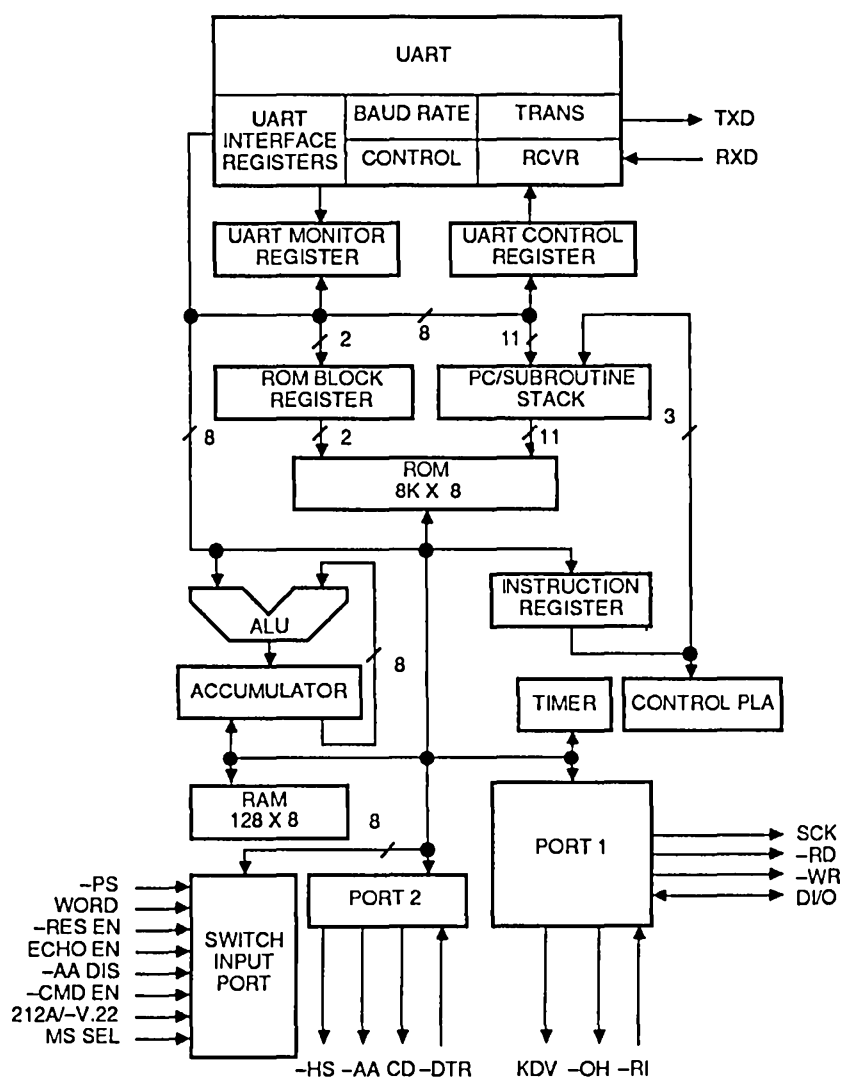
The VL7C414 automatically controls the power up/down feature of the VL7C412 to maintain lowest possible system power consumption.

For specific high volume applications, the control program can be modified by VLSI Technology, Inc. to include additional commands and functions.

PIN DIAGRAMS



BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Package
VL7C414-PC	Plastic DIP
VL7C414-QC	Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range is 0°C to +70°C.

SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Description
N.C.	1	No connection
N.C.	2	No connection
TEST	3	When the test input is high, the VL7C414 enters a test mode (used for factory testing only). For normal operation, this pin can be left open or connected to ground.
KDV/-KDV	4	This output controls the operation of the data/voice relay. The polarity of this output is selected by -PS pin. If -PS is connected to ground, this output is active high, i.e., it is low when modem is on hook, causing the data/voice relay to be off and the phone line is connected to the phone set. During a data call, this output goes high to operate the data/voice relay, disconnecting the phone set from the phone line. It may also be used to drive a relay for multi-line phone applications to close the A and A1 leads. If -PS pin is left open or connected to VCC, this output is active low, i.e., it is high when the modem is on hook and low when modem makes a data call.
-RI	5	The output of the ring detector in the DAA is connected to this input. A low level on this input indicates the "On" duration of the ring cycle. This is a Schmitt-trigger input, allowing for slow rising and falling signals on this pin.
OH/-OH	6	This output controls the operation of the hookswitch relay in the DAA. The polarity of this output is selected by -PS pin. If -PS pin is connected to ground, this output is active high, i.e., it is low when the modem is on hook. During a data call, it goes high to operate the hookswitch relay and seize the phone line. During rotary dialing, the VL7C414 pulses this output at a rate of 10 pulses per second with appropriate Mark/Space ratio depending on 212A or V.22 mode. If -PS pin is left open or connected to VCC, this output is active low, i.e., it is high when the modem is on hook and low during data call.
CLK	7	A 7.3728 MHz clock signal must be connected to this input. Normally, the CKOUT pin of the VL7C412A modem is connected to this pin. All internal timing is derived from this clock.
-WR	8	This pin is used to initiate writing of data to the VL7C412A modem.
-RD	9	This pin is used to initiate reading of data from the VL7C412A modem.
SCK	10	The VL7C414 supplies a shift clock on this pin to the VL7C412A modem for reading or writing data.
DI/O	11	The VL7C414 shifts data serially out of this pin to VL7C412A during a write operation and shifts data serially into this pin during a read operation from the VL7C412A.
TXD	12	The VL7C414 outputs serial data in asynchronous start/stop format at the data rate selected by the terminal. This data is either echo of commands received from the terminal or result codes generated by the controller during processing of the commands. This output is normally high and should be "AND"ed with the RXD output of the VL7C412A to form RXD data to the terminal.
RXD	13	The VL7C414 receives command data from the terminal on this pin. The UART in the controller connects the serial asynchronous start/stop data into a parallel byte for processing by the controller.
GND	14	Ground reference (0 V).
-PS	15	This input controls the polarity of KDV and OH outputs. When left open or connected to VCC, it forces the KDV and OH outputs to be active low. If this input is connected to ground, KDV and OH outputs are active high.
WORD	16	When the input is open or connected to VCC, the VL7C414 sends result codes as words. When this input is low, result codes are sent as digits. This setting can also be changed by entering the V command.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Description
-RES EN	17	When this input is low, the VL7C414 sends result codes. When this input is high or left open, commands received from the terminal are performed but result codes are not sent. This setting can also be changed by entering the Q command.
ECHO EN	18	When this input is high or left open, the VL7C414 echoes characters received from the terminal in the command state. When this input is low, the VL7C414 will not echo characters unless it is set for half duplex and it is on line. This setting can also be changed by entering the E command.
-AA DIS	19	When this input is low, the VL7C414 will not answer incoming calls. When this input is high or left open, the VL7C414 automatically answers incoming calls on the first ring. This function can also be enabled/disabled by writing to the S0 register.
-CMD EN	20	When this input is low, the VL7C414 recognizes command sent to it. For some applications such as unattended answering operation it is better to disable this function by leaving this input open or connecting it to VCC.
212A-V.22	21	When this input is open or connected to VCC, the VL7C414 supports Bell 103 and 212A modes. When this input is low, the VL7C414 supports the CCITT V.22 and V.21 modes. This setting can also be changed by entering the B command.
MS SEL	22	When this input is open or connected to VCC, the Mark/Space ratio is U.S. standard, 40/60 Make/Break. When it is low, the Mark/Space ratio is European standard, 33/67 Make/Break.
N.C.	23	No connection
-HS	24	This output, when low, indicates that the modem is in the high speed (1200 bps) mode. When high, it indicates that it is in the low speed (300 bps) mode. This output can be directly connected to a light emitting diode through a 330 Ω resistor.
-AA	25	This output is low when the VL7C414 is set for auto-answer mode, either by switch input -AA DIS (pin 19) or register S0. The output goes high during each ring. If the device is not set to answer the phone (pin 19 is low or S0 = 0), this output goes low each time the phone rings. A light emitting diode through a 330 Ω resistor can be directly connected to this output.
-CD	26	This output goes low when the VL7C414 detects a carrier signal from the remote modem. If the connection is broken or never established, it remains high. A light emitting diode can be directly connected to this output through a 330 Ω resistor.
-DTR	27	When this input is low, the VL7C414 executes data call commands. If during a data call, this input goes high, the VL7C414 terminates the data call, hangs up the phone line and returns to command state.
VCC	28	Positive supply (+5 V).

TABLE 1. VL7C414 SOFTWARE REGISTERS

Register	Range/Units	Description	Default
S0	0-255 Rings	Ring to answer telephone on	0
S1	0-255 Rings	Number of rings	0
S2	0-127 ASCII	Escape code character	43 (+)
S3	0-127 ASCII	Character recognized as carriage return	13 (CR)
S4	0-127 ASCII	Character recognized as line feedback	10 (LF)
S5	0-32, 127 ASCII	Character recognized as back space	8 (BS)
S6	2-255 sec.	Wait time for dial tone	2
S7	1-255 sec.	Wait time for carrier	30
S8	0-255 sec.	Pause time (caused by comma)	2
S9	1-255 1/10 sec.	Carrier detect response time	6
S10	1-255 1/10 sec.	Delay between loss of carrier and hang up	7
S11	50-255 millisec.	Duration and spacing of Touch-Tones	70
S12	20-255 1/50 sec.	Escape code guard time	50
S13	bit mapped	UART status register	-
S14	bit mapped	Option register	-
S15	bit mapped	Flag register	-
S16	0, 1, 2, 4	Test modes	0

TABLE 2. COMMAND SUMMARY
PREFIX, REPEAT AND ESCAPE COMMANDS

Command	Description (Notes 1 & 2)
AT	Attention prefix: precedes all command lines except + + + (escape) and A/(repeat) commands
A/	Repeat last command line (A/ is not followed by carriage return)
+ + +	Escape code: go from on-line state to command state (one second pause before and after escape code entry; ; + + + is not followed by carriage return)

DIALING COMMANDS

Command	Description (Notes 1 & 2)	Command	Description (Notes 1 & 2)
D	Dial	/	Wait for 1/8 second
P	Pulse*	@	Wait for silence
T	Touch-Tone	W	Wait for second dial tone
,	Pause	;	Return to command state after dialing
!	Flash	R	Reverse mode (to call originate-only modem)

OTHER COMMANDS

Commands	Description (Notes 1 & 2)	Commands	Description (Notes 1 & 2)
A	Answer call without waiting for ring	M1	Speaker on until carrier detected*
B/B0	CCITT V.22 mode (Note 3)	M2	Speaker always on
B1	Bell 103 and 212A mode*	O	Go to on-line state
C/C0	Transmit carrier off	O1	Remote digital loopback off*
C1	Carrier on*	O2	Remote digital loopback request
E/E0	Characters not echoed	Q/Q0	Result codes displayed*
E1	Characters echoed*	Q1	Result codes not displayed
F/F0	Half duplex	Sr?	Requests current value of register r
F1	Full duplex*	Sr = n	Sets register r to value of n
H/H0	On hook (hang up)	V/V0	Digit result codes
H1	Off hook; line and auxiliary relay	V1	Word result codes*
H2	Off hook; line relay only	X/X0	Compatible with Hayes-type 300 modems*
I/I0	Request product ID code (130)	X1	Result code CONNECT 1200 enabled
I1	Firmware revision number	X2	Enables dial tone detection
I2	Test internal memory	X3	Enables busy signal detection
L/L1	Low speaker volume	X4	Enables dial tone and busy signal detection
L2	Medium speaker volume	Y/Y0	Long space disconnect disabled*
L3	High speaker volume	Y1	Long space disconnect enabled
M/M0	Speaker always off	Z	Software reset: restores all default settings

- Notes:**
1. Default modes are indicated by *.
 2. Commands entered with null parameters assume 0 - X is the same as X0.
 3. When the ATB command is used in the answer mode, the VL7C412A is placed in either the V.21 or the V.22 mode, depending on the response from the remote modem. In the originate mode, the VL7C414 will sense if the baud rate is set at 300 or 1200 bits per second and will adjust the VL7C412A accordingly.

TABLE 3. RESULT CODES

Digit Code	Word Code	Description
0	OK	Command executed
1	Connect	Connected at 300 or 1200 bps Connected at 300 bps, if result of X1, X2, X3, or X4 command
2	Ring	Ringing signal detected (Note)
3	No Carrier	Carrier signal not detected or lost
4	Error	Illegal command Error in command line Command line exceeds buffer (40 characters, including punctuation) Invalid character format at 1200 bps
5	Connect 1200	Connected at 1200 bps. Results from X1, X2, X3, or X4 commands only
6	No Dialtone	Dialtone not detected and subsequent commands not processed Results from X2 or X4 commands only
7	Busy	Busy signal detected and subsequent commands not processed Results from X3 or X4 commands only
8	No Answer	Silence not detected and subsequent commands not processed Results from @ command only

Note : When the VL7C414 detects a ringing on the telephone line, it sends a RING result code. However, the VL7C414 will answer the call only if it is in auto-answer mode or is given an A command.

ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature 0°C to +70°C
 Storage Temperature -65°C to +150°C
 Supply Voltage to Ground Potential +6 V
 Applied Input Voltage -0.6 V to VCC + 6 V
 Power Dissipation 500 mW

Stresses above those listed may cause permanent damage to the device.
 These are stress ratings only, functional operation of this device at these or any other conditions above those indicated

in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS: TA = 0 to +70 °C, VCC = 5 V ±10%

Symbol	Parameter	Min	Typ	Max	Units	Conditions
VCC	Positive Supply Voltage	4.5	5.0	5.5	V	
ICC	Operating Current		10.0		mA	@ VCC = 5 V, outputs unloaded
VIH	High Level Input Voltage	2.0			V	All pins except -RI
VIL	Low Level Input Voltage			0.8	V	All pins except -RI
VT+	Positive Hysteresis Threshold		2.5		V	-RI pin
VT-	Negative Hysteresis Threshold		1.8		V	-RI pin
VOH	High Level Output Voltage	VCC - 1.0			V	@ IOH = -2 mA
VOL	Low Level Output Voltage			0.4	V	@ IOL = 2 mA
IL	Leakage Current (Note)		±1.0		μA	
FCLK	Clock Frequency	7.3721	7.3728	7.3735	MHz	

Note : This applies to all pins except TEST, which has an internal pull-down -WR, -RD, SCK, DI/O, and switch input pins 15 thru 21 which have internal pull-ups.

Note: Schematics are for illustration purposes only. Operational systems may require modifications.



FEATURES

- Supports T1, T1C, and CEPT data rates
- AMI, B8ZS, HDB3 format
- Meets AT&T Technical Advisory #34 for DSX1 and DSX1C interface standards, publication 43802 standard for jitter tolerance, and jitter standard for digital channel bank
- Meets CCITT recommendation G.703 for 1.544M bps and 2.048M bps
- Input frequency memory
- Jitter smoothing FIFO
- Loopback and data path configurable
- Bipolar violation detection & flagging
- AIS, LOS, Overrun/Underrun detection and flagging
- Microprocessor compatible interface
- Low power CMOS technology

DESCRIPTION

The VL80C75 is a general purpose PCM Line Interface circuit. It is designed to provide a bipolar interface according to T1 (1.544M bps), T1C (3.152M bps), or CEPT (2.048M bps) specifications. It is capable of sending (encoding) and receiving (decoding) AMI, B8ZS or HDB3 data formats.

The incorporation of on-chip voltage comparators and adaptive reference levels allows direct interface to the analog line signal. Sensitivity is optimized by monitoring the incoming bipolar signal.

An injection locking divider permits clock recovery from the incoming serial data stream. A 32-bit long FIFO (elastic buffer) may be used in either the decoder or the encoder path to smooth clock jitter. A DC output signal is provided to facilitate the control of an external VCO.

The VL80C75 will indicate the presence of bipolar violation in the input data as well as a FIFO underflow/overflow.

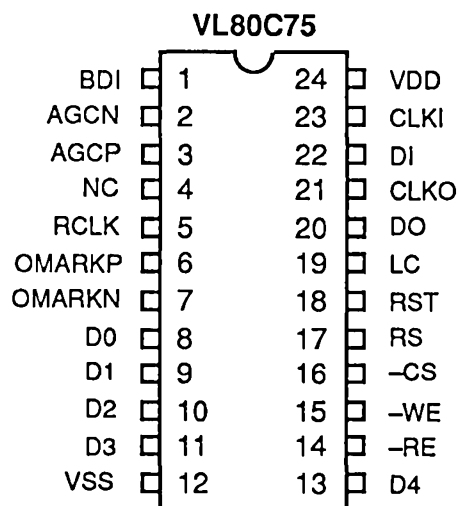
Interfacing to the external bipolar line driver is facilitated by the provision of 50% duty cycle drive pulses.

The system interface is microprocessor compatible. The internal control and status registers may be accessed by a parallel interface.

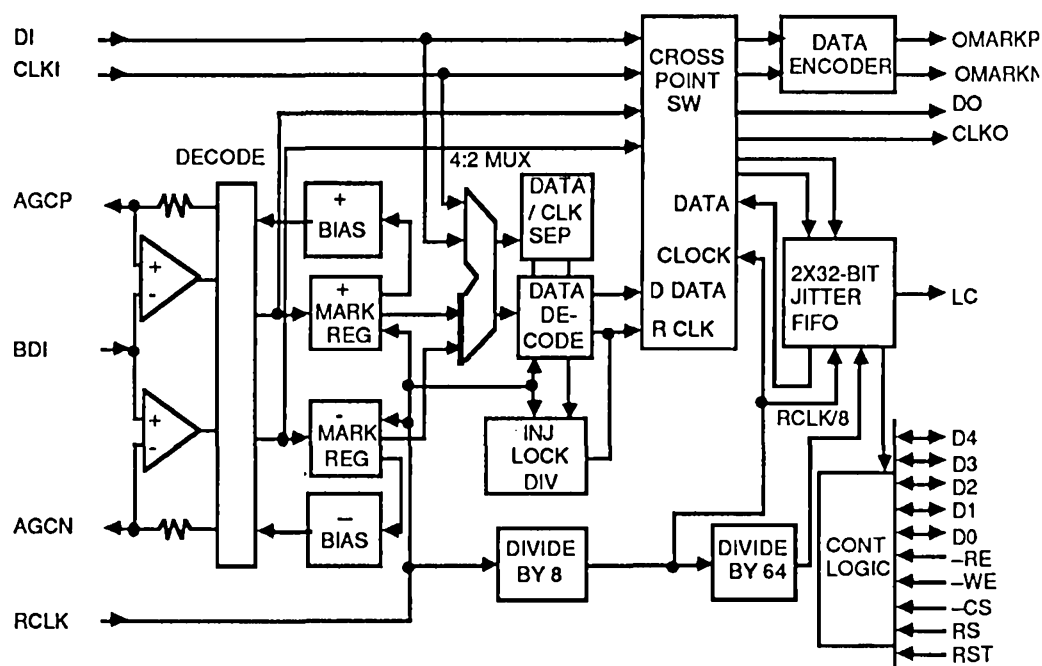
System test is assisted by the provision of a loopback feature which operates in both directions.

The VL80C75 is fabricated in a double metal, n-well, two micron silicon gate CMOS process and is housed in a 24-pin 300 mil DIP or ceramic package.

PIN DIAGRAM



BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Package
VL80C75-PC	Plastic DIP
VL80C75-CC	Ceramic DIP

Note: Operating temperature range is 0 C to +70 C.

Signal Descriptions

Signal Name	Pin Number	Signal Name
BDI	1	Bipolar Data Input - The received analog line signal is capacitively coupled to this high impedance input.
AGCN	2	Automatic Gain Control Output (Negative) - This output is used to provide an automatically adjusted threshold voltage to the analog input comparators. A 0.1 μ F capacitor to VSS, a 1 M Ω resistor to pin 3, and a 4.7 M Ω resistor to VDD should be attached to this pin.
AGCP	3	Automatic Gain Control Output (Positive) - See AGCN. A 4.7 M Ω resistor to VSS instead of VDD should be used, however.
RCLK	5	Reference Clock - This TTL input should have a clock which is 8 times the line frequency (T1: 12.352 MHz, T1C: 25.216 MHz, CEPT: 16.284 MHz). This clock is used internally to recover the clock from the incoming received analog signal and is used to clock data out of the jitter smoothing FIFO.
OMARKP	6	Output Mark (Positive) - Encoded data for driving positive line pulses appear at this output.
OMARKN	7	Output Mark (Negative) - Encoded data for driving negative line pulses appear at this output.
D0 - D4	8-11,13	Data I/O - Configuration and status data is input or output on these bidirectional pins.
VSS	12	Negative Power Supply - Normally ground.
-RE	14	Read Enable - A low on this input enables the IC to output either the present configuration control data or the alarm status data on the D0-D4 data pins depending on the state of RS.
-WE	15	Write Enable - A low on this input enables the writing of configuration data on the D0-D4 data pins. This pin must not be low at the same time as the -RE pin.
-CS	16	Chip Select - A low on this pin enables the reading or writing of data into the IC.
RS	17	Read Select - A high on this input selects the configuration data to output during a read while a low selects the alarm status data to be output.
RST	18	Reset - A logic high on this input initializes the internal configuration registers, resets the alarm status bits, and initializes the jitter filter.
LC	19	Loop Control - This output is used to control an external VCO or VXO to provide a stable RCLK signal. The duty cycle will be 50% if the write clock to the jitter smoothing FIFO is centered. The duty cycle will shorten or increase in proportion to the FIFO fill status.
DO	20	Data Output - Decoded and received data is normally output on this pin.
CLKO	21	Clock Out - Data on the DO pin is output on the rising edges of this clock signal.
DI	22	Data In - NRZ Data on this input is normally encoded and output at the OMARKP and OMARKN pins.
CLKI	23	Clock In - This input is used to clock the data on the DI pin into the IC on rising edges of this signal. Nominally a 50% duty cycle signal.
VDD	24	Positive Power Supply - Normally, +5 V.

FUNCTIONAL DESCRIPTION

The VL80C75 consists of two separate sections, the line receiver and the line transmitter.

The receiver accepts a bipolar (ternary) input signal and converts it into a decoded data stream. A clock signal is extracted from the incoming data stream.

The transmitter converts a digital input data stream into two output drive pulses; these pulses drive external transistors which, in turn, drive the transmission lines through line build out circuits, or directly via a transformer. Data zeros are represented by the absence of a pulse in the output and ones are represented by a pulse from one or the other transistor. The polarity of these pulses typically alternate so that the DC content of the signal equals zero.

Voltage Comparators

The function of these comparators is to convert the incoming bipolar data stream into two logic signals which correspond to a positive or negative pulse on the input line.

Mark Registers and Bias Drivers

The VL80C75 samples the comparator outputs, and stores the pulses in the mark registers. Should the input data pulse width deviate from 50%, the AGC signals (AGCP and AGCN) will alter the reference voltage of the comparators in such a way that the output pulse width from the comparators will drive the recovered pulses' duty cycle towards 50%.

Data and Clock Recovery

This circuit extracts the clock from the input stream by means of an injection lock divider. The divider responds to the leading edge of the recovered pulses by resetting an internal divider to zero. If there is no "mark" on the input then the divider will operate in its free running mode and generate a square wave clock. If a pulse is detected, the leading edge of the recovered clock is reset.

Data Decoder

The decoder converts input data format of either AMI, B8ZS or HDB3 code into NRZ data. This circuit also detects bipolar format violations on the input data. The VL80C75 operates using either AMI, B8ZS, or HDB3 coding formats. AMI (Alternate Mark Inversion)- In this mode a positive "mark" is always

followed by a negative "mark" and vice-versa. This process ensures that no DC component exists in the signals. Zeros are represented by the absence of pulses. Consecutive zeros exceeding 15 bits are usually not allowed since clock information is not present in this condition. However, the 80C75 will always maintain a recovered clock based on the last received mark position.

B8ZS (Bipolar 8 Zeros Suppression)

In this coding format, the input data pattern follows the AMI code except that a B8ZS code is substituted for each block of eight consecutive zeros. This assures steady clock updates regardless of the data pattern. The B8ZS format is 000VB0VB, where B stands for an AMI pulse and V is a pulse which violates that rule.

HDB3 (High Density Bipolar 3 code)

This format obeys the AMI rule except that a HDB3 filling sequence is inserted for each block of four consecutive zeros. The filling sequences are shown below.

Previous Mark (B, V)	Previous Violation (V)	Filling Sec.
+	+	- 0 0 -
-	+	0 0 0 -
+	-	0 0 0 +
-	-	+ 0 0 +

Data Encoder

The encoder transforms the NRZ input data into coded bit pattern of either AMI, B8ZS or HDB3 format depending on the bit code C0 and C1. The output signals (OMARKP, OMARKN) are used to drive the transmission lines via external transistors.

FIFO (First-In First-Out Register)

This circuit has 32 stages and is 2 bits wide and is used to eliminate jitter. 5 bit access counters in the FIFO provide the data read and write addresses. The read count is offset by 16 bits with respect to the write count when initialized.

The write clock (normally the recovered data clock) transfers data into the FIFO. The read clock (normally RCLK + 8 which comes from an external VCO and does not contain jitter) transfers data out the FIFO, normally 16 bits of delay later.

The frequency of the external VCO is controlled by signal Loop Control, LC, of the FIFO. If the write clock runs faster or slower than the read clock, the resultant DC voltage of LC will cause the VCO to raise or lower its frequency and thereby correspondingly changing the read frequency.

The range in which the read clock can track the write clock is dependent on the loop gain and the external crystal oscillator.

Overflow or underflow occurs when the read and write counts are equal. When this condition is detected it is flagged and the FIFO is reinitialized.

Cross Point Switch

This switch enables the internal signals of the VL80C75 to be routed to allow various configurations of the jitter filter and data paths.

Divide by 8 Counter

This is a 3-bit binary up counter. The counter divides the incoming reference clock, RCLK, by a factor of eight. The RCLK frequency is of either 8 x T1 rate (12.352 MHz), 8 x T1C rate (25.216 MHz) or 8 x CEPT rate (16.384 MHz). The MSB output of this counter serves as the read clock for the FIFO.

Zeros and Ones Detect

This circuit detects the receipt of a string of 63 consecutive zeros (implying the line is disconnected) or 1023 consecutive ones ("Blue Alarm" or AIS) on the input ternary data stream and flags these conditions in a status register.

PROGRAMMING

The VL80C75 may be configured for several modes of operation. Control data is written into the VL80C75 via the D0-D4 pins when -CS and -WE pins transition from low to high, while the alarm status or present control data may be read out on these pins when -CS and -RE are low. The encode/decode mode and the internal configuration of the 80C75 are controlled by the data written on the D0-D4 pins according to Table 1.

The control data or alarm status is output on the D0-D4 pins when -CS and -RE are low according to Table 2.

FIGURE 1. VL80C75 EVALUATION CIRCUIT

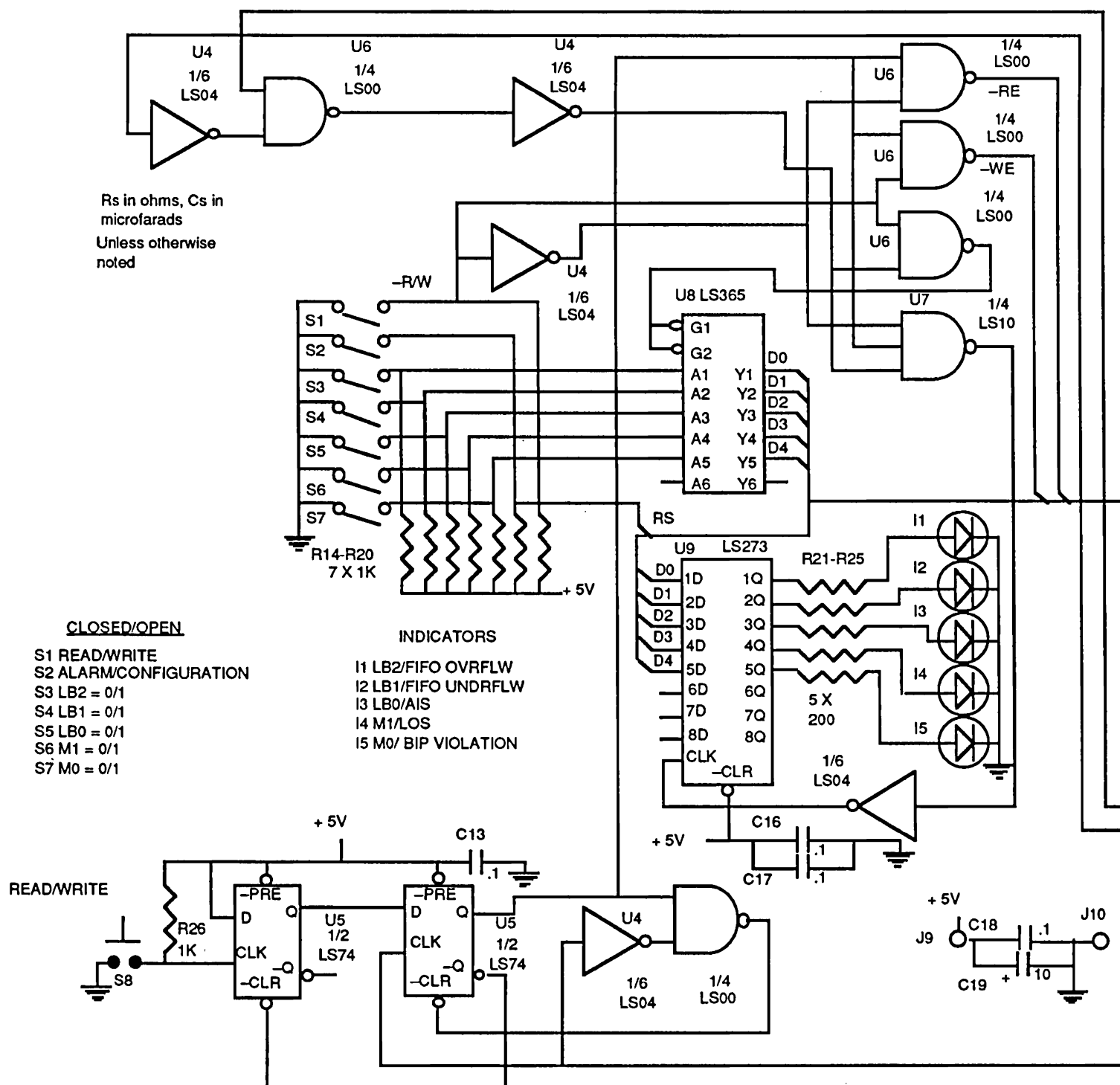


TABLE 1. WRITE DATA

Control Bit Name / Data Line					Operating Mode
LB2 / D0	LB1 / D1	LB0 / D2	C1 / D3	C0 / D4	
X	X	X	0	0	AMI Coding
X	X	X	0	1	B8ZS Coding
X	X	X	1	0	HDB3 Coding
0	0	0	X	X	Jitter Filter in Transmit Path: DI to Jitter to OMARKN/P; BPI to DO
0	0	1	X	X	Jitter Filter in Receive Path: DI to OMARKN/P; BPI to Jitter to DO
0	1	0	X	X	Loopback, Jitter Filter in TX: DI to Jitter to DO; BPI to OMARKN/P
0	1	1	X	X	Loopback, Jitter Filter in RX: DI to DO; BPI to Jitter to OMARKN/P
1	0	0	X	X	Loopback: DI to DO; BPI to OMARKN/P
1	0	1	X	X	No Jitter Filter: DI to OMARKN/P; BPI to DO

TABLE 2. READ DATA

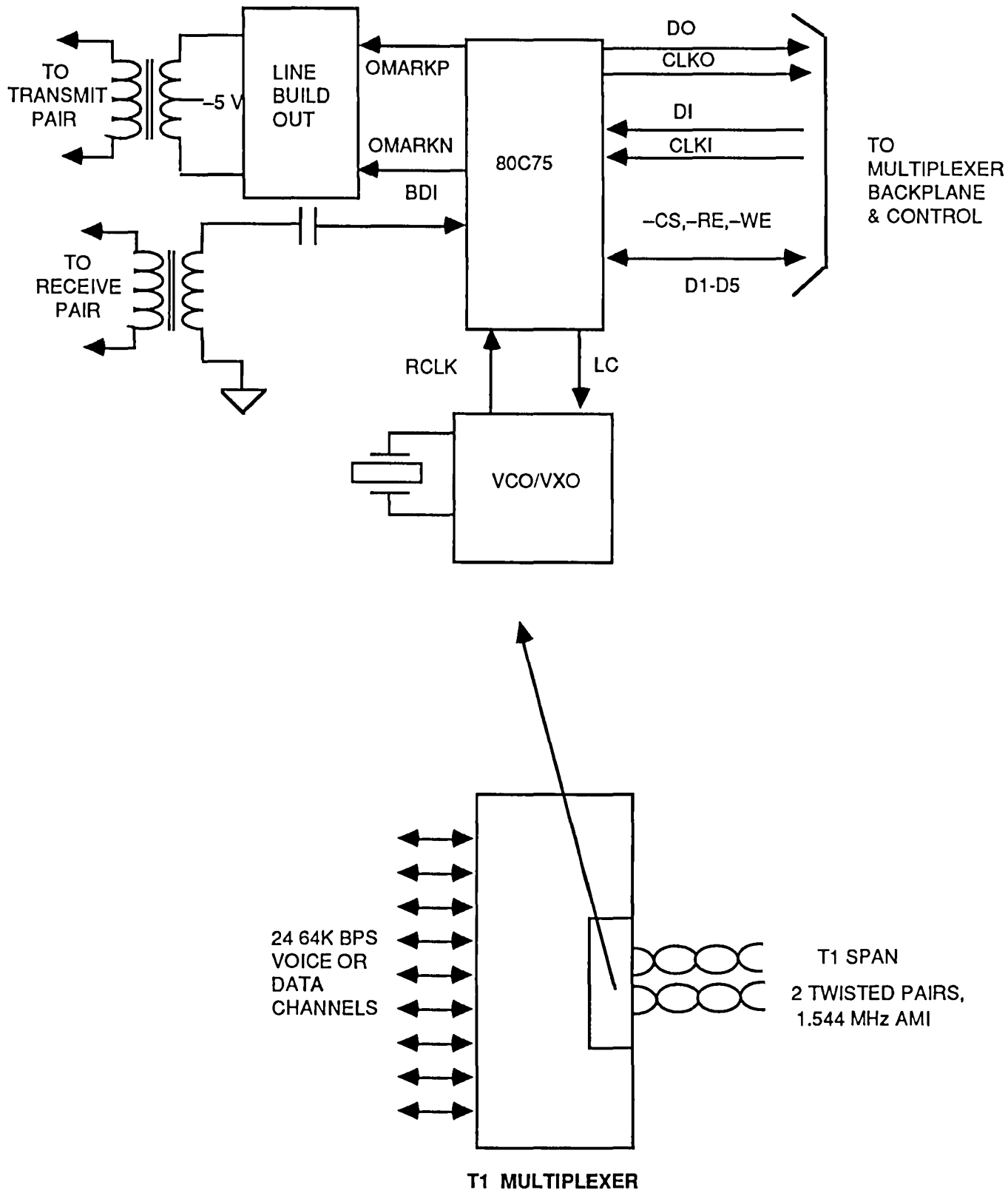
Bit	RS = 0	RS = 0
D0	FIFO Overflow	LB2
D1	FIFO Underflow	LB1
D2	AIS, > 1023 Consecutive Ones	LB0
D3	LOS, > 63 Consecutive Zeros	C1
D4	Bipolar Violation	C0

Note: Alarm bits reset after read.

EVALUATION CIRCUIT

A typical evaluation circuit is shown in Figure 1. This circuit provides the ability to read and write data into the VL80C75 and provides a simple interface to the twisted pair. Line build out circuitry is not included in this schematic but can be easily added for a given application. A typical T1 Multiplexer applications is shown in Figure 2.

FIGURE 2. TYPICAL APPLICATION

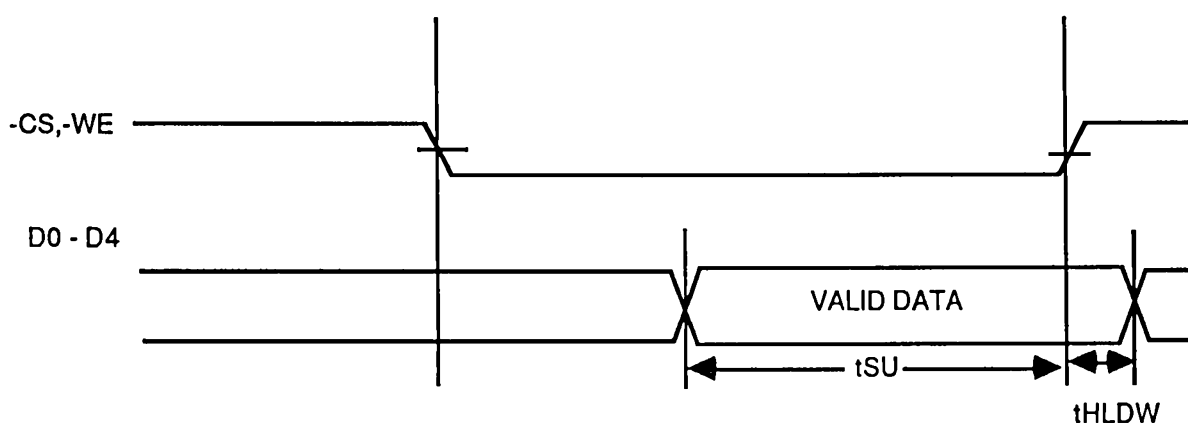
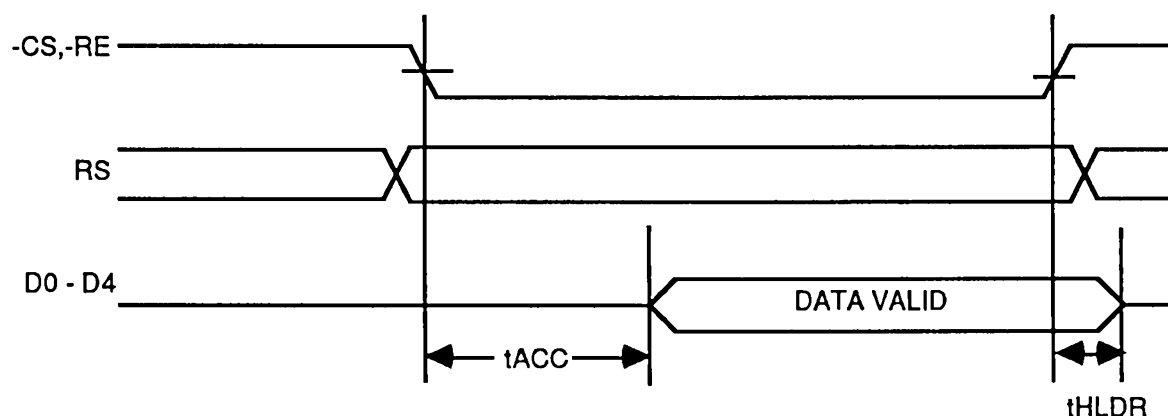


AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0 V
Input Rise and Fall Times	10 ns
Input Timing Levels	1.5 V
Output Reference Levels	1.5 V

AC CHARACTERISTICS: $T_A = 0$ to 70°C , $V_{DD} = 5\text{ V } 10\%$, unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Units	Condition
t_{ACC}	Access Time			75	ns	
t_{SU}	Setup Time	50			ns	
t_{HLDW}	Hold Time Write	0			ns	
t_{HLDR}	Hold Time Read	5			ns	
t_{RCLK}	Clock Frequency			25.216	MHz	
	BPI Sensitivity below DSX-1		-13		dB	



ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	-10 to +80°C
Storage Temperature	-65 to +150°C
Supply Voltage to Ground Potential	-0.5 to +7.0 V
Applied Output Voltage	-0.5 to +7.0 V
Applied Input Voltage	-0.5 to +7.0 V
Power Dissipation	1.0 W

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in

the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS: TA = 0 to +70 °C, VCC = 5 V ±10%, unless otherwise noted.

Symbol	Parameter	Limits			Units	Conditions
		Min	Typ	Max		
VIL	Input Low Voltage	-0.5		0.8	V	
VIH	Input High Voltage	2.0		5.0	V	
VOL	Output Low Voltage			0.4	V	IOL = 4.0 mA
VOH	Output High Voltage	3.9			V	IOH = -4.0 mA
ZIN	BPI Input Impedance		50		kΩ	
VREF	BPI Reference Level		2.5		V	
IIH	Input Load Current	-5.0		5.0	μA	VIN = 5.5 V
OLH	Output Leakage			10.0	μA	VOUT = 5.5 V
ILHB	BPI Input Current	45		80	μA	VIN = 5.5 V
ICC	Operating Current		40	50	mA	Outputs Unloaded

CAPACITANCE: TA = 25 °C, f = 1.0 MHz

Symbol	Parameter	Typ	Max	Unit	Condition
CI	Input Capacitance		5	pF	VOUT = 0 V, Note
CO	Output Capacitance		7	pF	VOUT = 0 V, Note

Note: This parameter is periodically sampled only.

IBM PS/2® MODEL 30-COMPATIBLE SYSTEM CONTROLLER

FEATURES

- Controls 8086 CPU speed at 8 MHz or 10 MHz
- Generates programmable fast and normal timing for memory and I/O
- Supports 256k- or 1M-bit DRAMS
- Supports up to 8M bytes of additional memory
- Arbitrates the system bus among the CPU, DMA, math coprocessor, and DRAM memory refresh cycle
- Provides four channels of DMA as well as burst mode

DESCRIPTION

The CMOS VL82C031/OTI-031 is the System Controller device in the three-chip VLSI/OTI PS/2 Model 30-compatible chip set. the other two devices are

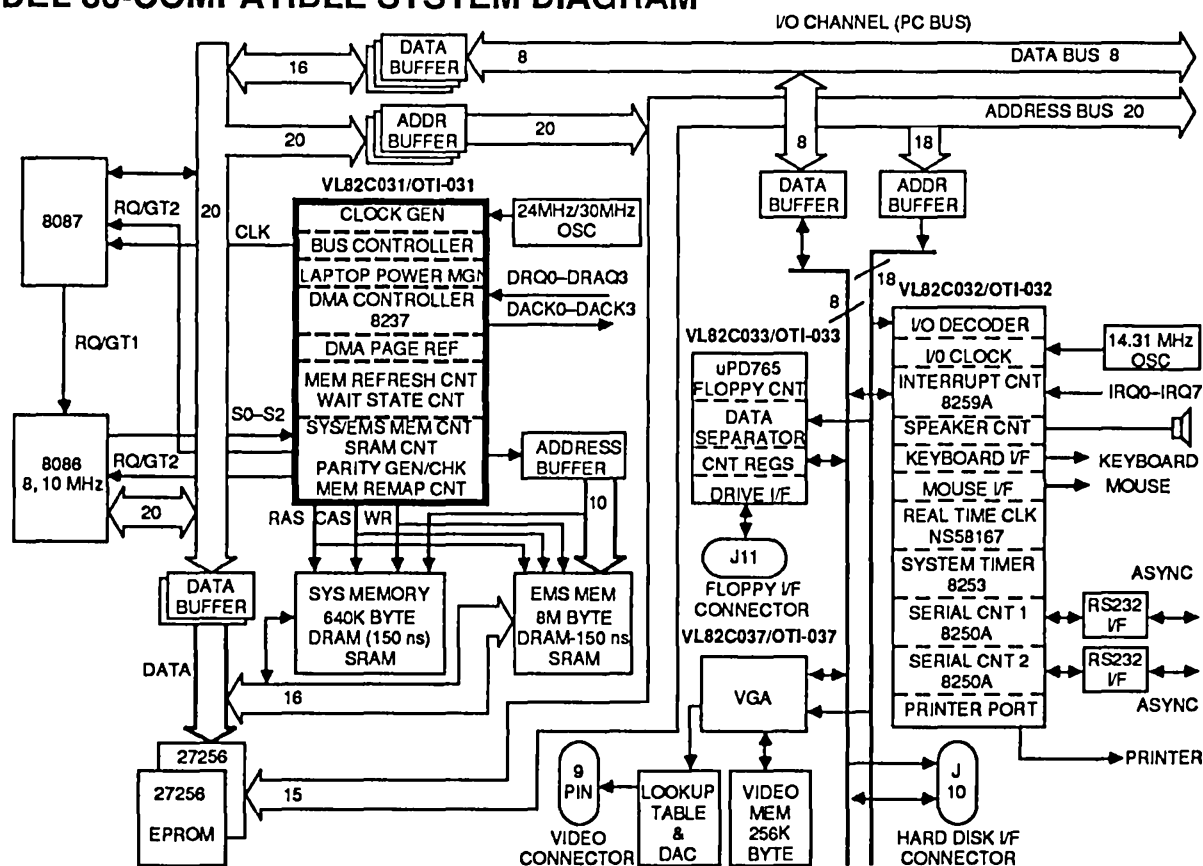
the VL82C032/OTI-032 I/O Controller and the VL82C033/OTI-033 Floppy Disk Controller and Data Separator.

The chip set integrates logic and functions on PS/2 Model 30-compatible systems to the point of reducing the printed circuit board device count by half, when memories are excluded. Further, while offering complete compatibility with the PS/2 Model 30-compatible system, the VLSI/OTI chip set improves system performance by allowing 10 MHz operation with no "wait states" (using 150 ns DRAMS), supports an additional 8M-bytes of memory using EMS (Expanded Memory Specification) 4.0, and controls system speed as necessary for optimum performance.

A fourth device, the VL82C037/OTI-037 VGA Video Graphics Controller is also used in the PS/2 Model 30-compatible system and provides high resolution graphics of 800 x 600 elements with 256 colors. Graphic capabilities of this resolution are usually found only on more expensive systems.

The VL82C031/OTI-031 provides the PS/2 Model-30 compatible system with the dual speed control, 8 MHz or 10 MHz, necessary to operate the system at peak performance. The device also controls memory, I/O, parity, address paths, data paths as well as handling four channels of direct memory access. The VL82C031/OTI-031 is available from both VLSI Technology Inc. and Oak Technology, Inc. in an industry-standard plastic 100 pin flat pack.

PS/2 MODEL 30-COMPATIBLE SYSTEM DIAGRAM



ORDER INFORMATION

Part Number	Package
VL82C031-FC	Plastic Flat Pack

PLEASE CONSULT DATA SHEET FOR DETAILED INFORMATION

Notes: Operating temperature range is 0°C to +70°C.
IBM PS/2® is a registered trademark of IBM Corp.

IBM PS/2® MODEL 30-COMPATIBLE I/O CONTROLLER
FEATURES

- Controls Model 30-compatible system keyboard and mouse
- Integrates the following functions on a single device:
 - 8253-compatible timer/counter
 - Dual 8250-compatible serial communications controller
 - Parallel port controller
 - 8259-compatible interrupt controller
 - 58167-compatible real-time clock
- Decodes subsystems for floppy disk, hard disk, and video
- Provides chip select logic for serial/parallel ports, disk controllers, video controllers, and real time clock.

DESCRIPTION

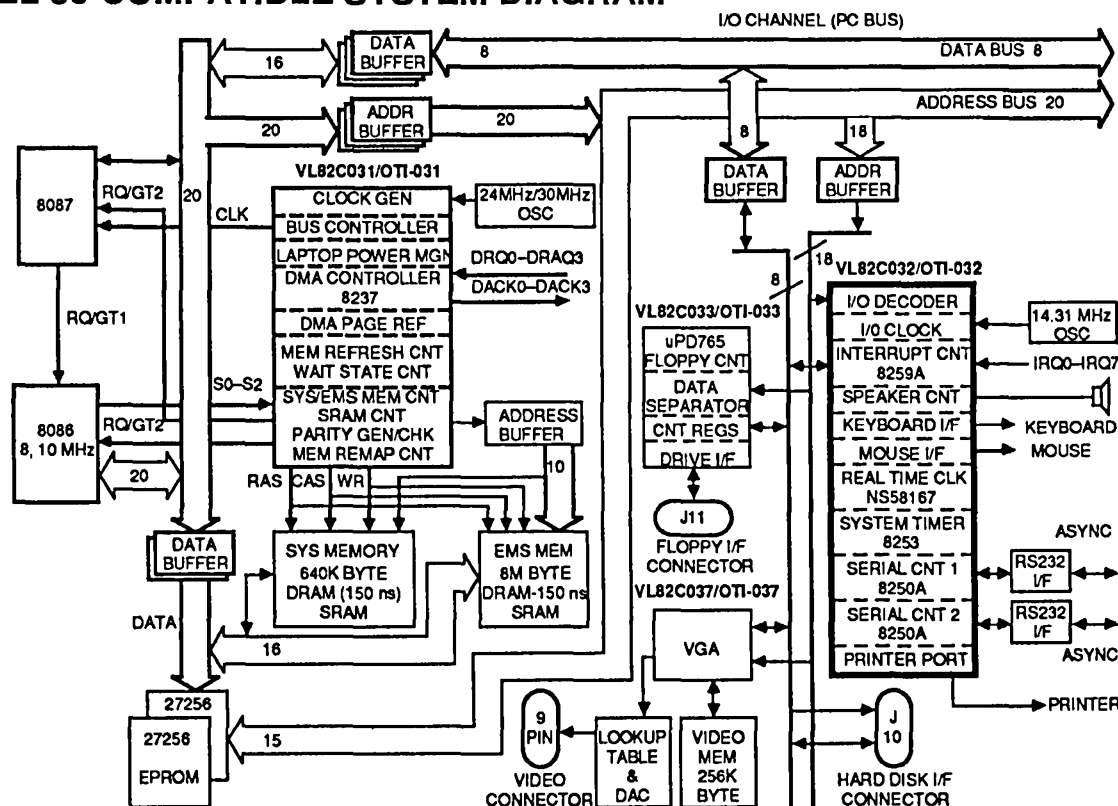
The CMOS VL82C032/OTI-032 is the Input/Output Controller device in the three-chip VLSI/OTI PS/2 Model 30-

compatible chip set. the other two devices are the VL82C031/OTI-031 System Controller and the VL82C033/OTI-033 Floppy Disk Controller and Data Separator.

The chip set integrates logic and functions on PS/2 Model 30-compatible systems to the point of reducing the printed circuit board device count by half, when memories are excluded. Further, while offering complete compatibility with the PS/2 Model 30-compatible system, the VLSI/OTI chip set improves system performance by allowing 10 MHz operation with no "wait states" (using 150 ns DRAMS), supports an additional 8M-bytes of memory using EMS (Expanded Memory Specification) 4.0, and controls system speed as necessary for optimum performance.

A fourth device, the VL82C037/OTI-037 VGA Video Graphics Controller is also used in the PS/2 Model 30-compatible system and provides high resolution graphics of 800 x 600 elements with 256 colors. Graphic capabilities of this resolution are usually found only on more expensive systems.

The VL82C032/OTI-032 provides the PS/2 Model-30 compatible system with control of both the keyboard and the pointing device ("mouse"), control of two serial communication channels, a real-time clock, as well as controlling both the disk storage and display functions. It also provides the chip select logic for the functions it controls. The VL82C032/OTI-032 is available from both VLSI Technology Inc. and Oak Technology, Inc. in an industry-standard plastic 100 pin flat pack.

PS/2 MODEL 30-COMPATIBLE SYSTEM DIAGRAM

ORDER INFORMATION

Part Number	Package
VL82C032-FC	Plastic Flat Pack

PLEASE CONSULT DATA SHEET FOR DETAILED INFORMATION

Notes: Operating temperature range is 0°C to +70°C.
IBM PS/2® is a registered trademark of IBM Corp.

IBM PS/2[®] MODEL 30-COMPATIBLE FLOPPY DISK CONTROLLER AND DATA SEPARATOR

FEATURES

- Provides a μ PD765A-compatible floppy disk controller
- Contains a precision analog data separator
- Integrates an internal phase comparator, and voltage controlled oscillator (VCO)
- Provides the system with three data rates:
 - 250K bits-per-second
 - 300K bits-per-second
 - 500K bits-per-second

DESCRIPTION

The VL82C033/OTI-033 is the Floppy Disk Controller and Data Separator device in the three-chip VLSI/OTI PS/2 Model 30-compatible chip set. The other two devices are the VL82C031/OTI-031 System Controller and the VL82C032/OTI-032

OTI-032 I/O Controller.

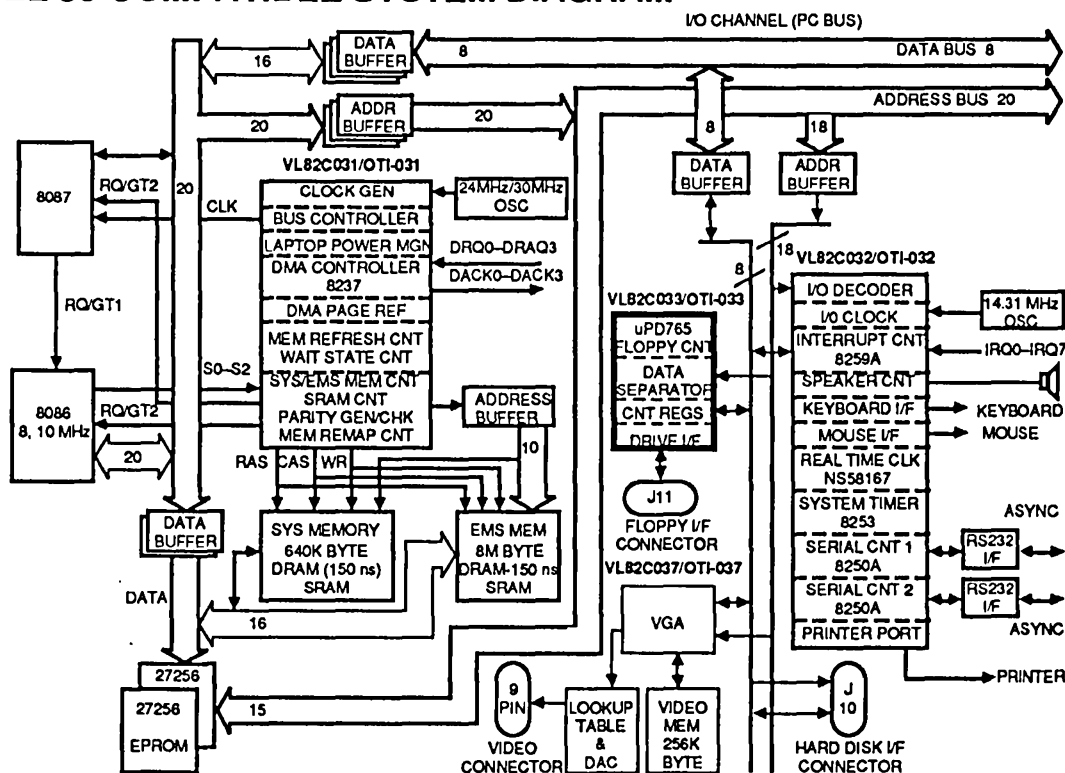
The chip set integrates logic and functions on PS/2 Model 30-compatible systems to the point of reducing the printed circuit board device count by half, when memories are excluded. Further, while offering complete compatibility with the PS/2 Model 30-compatible system, the VLSI/OTI chip set improves system performance by allowing 10 MHz operation with no "wait states" (using 150 ns DRAMS), supports an additional 8M-bytes of memory using EMS (Expanded Memory Specification) 4.0, and controls system speed as necessary for optimum performance.

A fourth device, the VL82C037/OTI-037 VGA Video Graphics Controller is also used in the PS/2 Model 30-compatible

system and provides high resolution graphics of 800 x 600 elements with 256 colors. Graphic capabilities of this resolution are usually found only on more expensive systems.

The VL82C033/OTI-033 provides the PS/2 Model-30 compatible system with a μ PD 765A-compatible floppy disk controller function, a precision analog data separator, an internal phase comparator, the required filters, as well as a voltage controlled oscillator (VCO). The VL82C033/OTI-033 provides the system with three floppy disk data rates: 250K bits-per-second, 300K bits-per-second, and 500K bits-per-second. The VL82C033/OTI-033 is available from both VLSI Technology Inc. and Oak Technology, Inc. in an industry-standard plastic 48 pin DIP.

PS/2 MODEL 30-COMPATIBLE SYSTEM DIAGRAM



ORDER INFORMATION

Part Number	Package
VL82C033-PC	Plastic DIP

PLEASE CONSULT DATA SHEET FOR DETAILED INFORMATION

Notes: Operating temperature range is 0°C to +70°C.
IBM PS/2[®] is a registered trademark of IBM Corp.

IBM VGA®-COMPATIBLE VIDEO GRAPHICS CONTROLLER

FEATURES

- Single-chip VGA video graphics device that is completely compatible in the following systems:
 - IBM PC/AT-compatible
 - IBM PC/XT-compatible
 - IBM PS/2-compatible
- Fully compatible with IBM VGA in all modes
- Fully compatible with IBM basic input/output system (BIOS)
- Provides 800 x 600 element high-resolution graphics with 256 colors
- Flicker-free operation in all video modes
- Hardware mouse cursor feature

DESCRIPTION

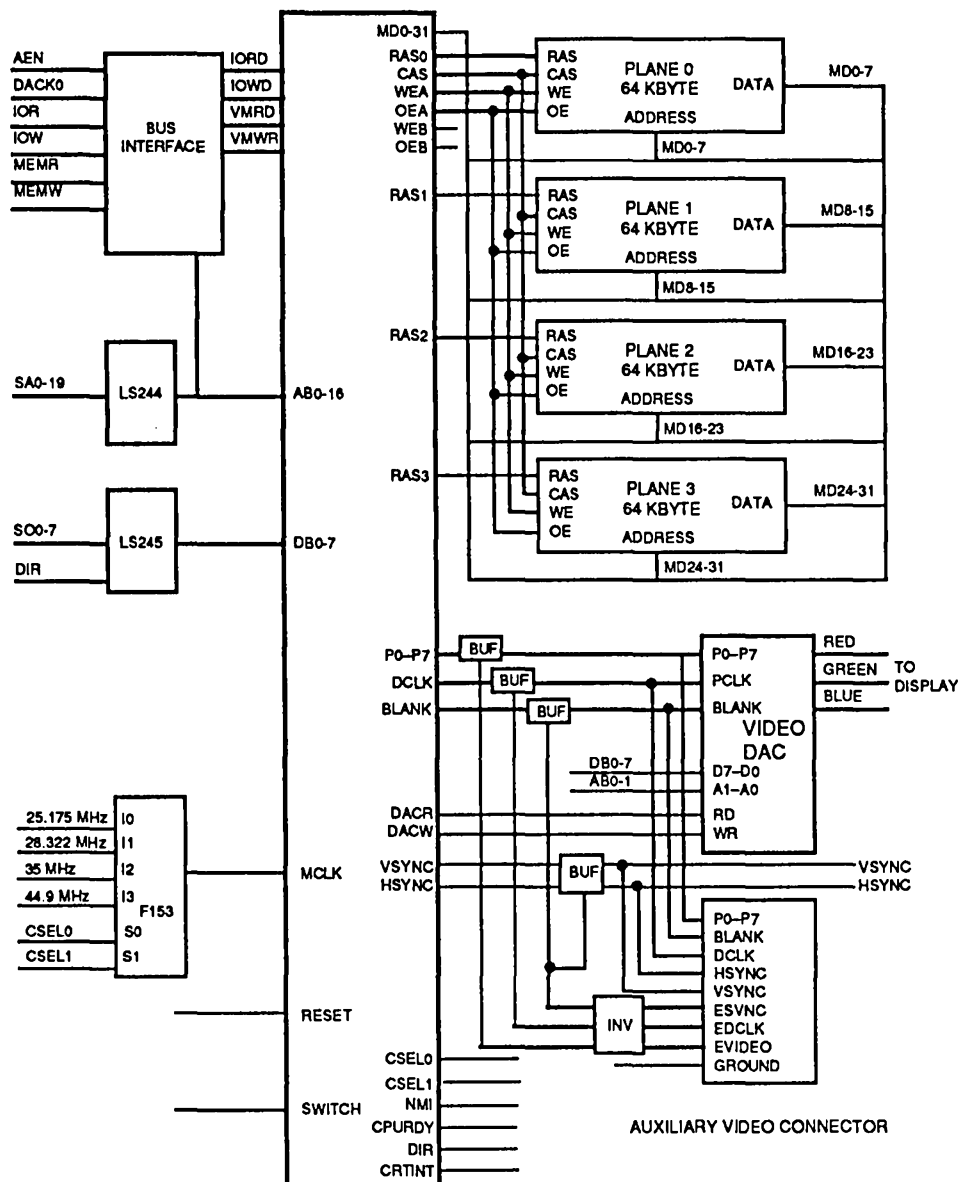
The VL82C037/OTI-037 VGA-compatible Video Graphics Controller is a single-chip, high-integration, high resolution graphics device intended for use in IBM PS/2® Model 30-compatible systems as well PC/AT- and PC/XT-compatible systems. It provides high resolution graphics of 800 x 600 elements with 256 colors.

The VL82C037/OTI-037 is fully compatible with IBM VGA in all modes, as well as being fully compatible with Hercules graphics. VL82C037/OTI-037 compatibility also extends to IBM EGA BIOS® (basic input/output system),

CGA and MDA. The VL82C037/OTI-037 automatically switches among the CGA, MDA, and Hercules graphic protocols.

The VLSI/OTI VGA-compatible device allows split-screen operation with independent scrolling and panning. It is also flicker-free in all modes. It supports an external digital-to-analog lookup table as well as additional video memory for high resolution operation with 256 colors. The VL82C037 is available from both VLSI Technology Inc. and Oak Technology, Inc. in an industry-standard plastic 100 pin flat pack.

SYSTEM BLOCK DIAGRAM



PLEASE CONSULT DATA SHEET FOR DETAILED INFORMATION

ORDER INFORMATION

Part Number	Package
VL82C037-FC	Plastic Flat Pack

Notes: Operating temperature range is 0°C to +70°C.
 IBM PS/2®, IBM VGA®, and IBM BIOS® are registered trademarks of IBM Corp.

PC/AT-COMPATIBLE PERIPHERAL CONTROLLER

FEATURES

- Fully compatible with IBM PC/AT-type designs
- Replaces 19 logic devices
- Supports 12 MHz processor clock
- Device is available as "cores" for user-specific designs
- Seven DMA channels
- 14 external interrupt requests
- Three timer/counter channels
- Designed in CMOS for low power consumption

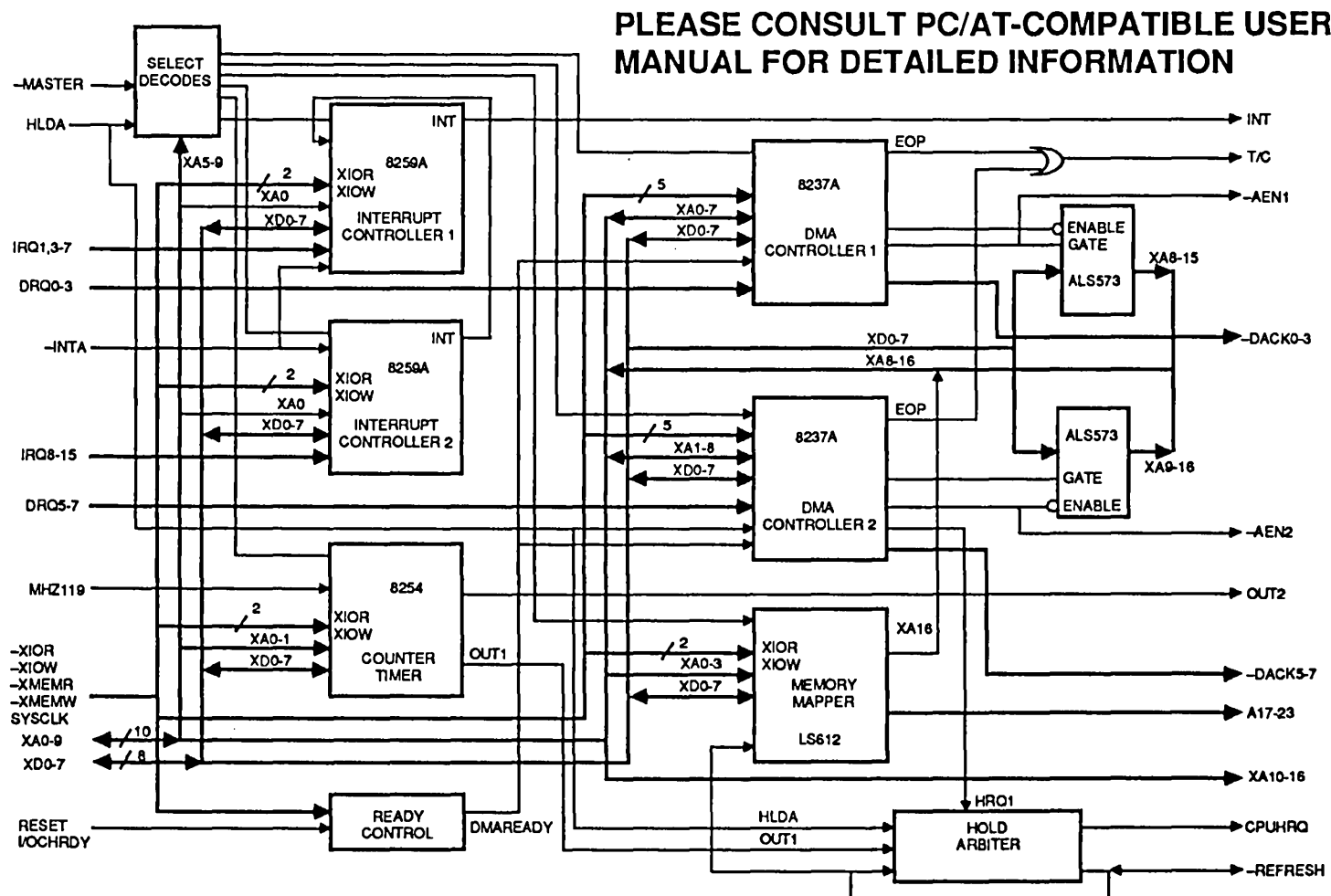
DESCRIPTION

The VL82C100 PC/AT-Compatible Peripheral Controller replaces two 82C37A Direct Memory Access Controllers, two 82C59A Interrupt Controllers, an 82C54 Programmable Counter, a 74LS612 AT Memory Mapper, two 74ALS573 Octal Three-State Latches, a 74ALS138 3-to-8 Decoder, and five other less-complex integrated circuits. Using this internal functionality, the VL82C100 provides all 24 address bits for 16M bits of DMA address space. It also interfaces directly to the CPU to handle all

interrupts. Timing for refresh cycles, and arbitration, between refresh and DMA hold requests, are also controlled by the VL82C100.

The device is manufactured with VLSI's advanced high-performance CMOS process and is available in JEDEC-standard 84-pin plastic leaded chip carrier (PLCC) package. The VL82C100 is individually available, or may be purchased as part of the complete five-device IBM PC/AT-compatible kit.

BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Package
VL82C100-QC	Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range is 0°C to +70°C

PC/AT-COMPATIBLE SYSTEM CONTROLLER
FEATURES

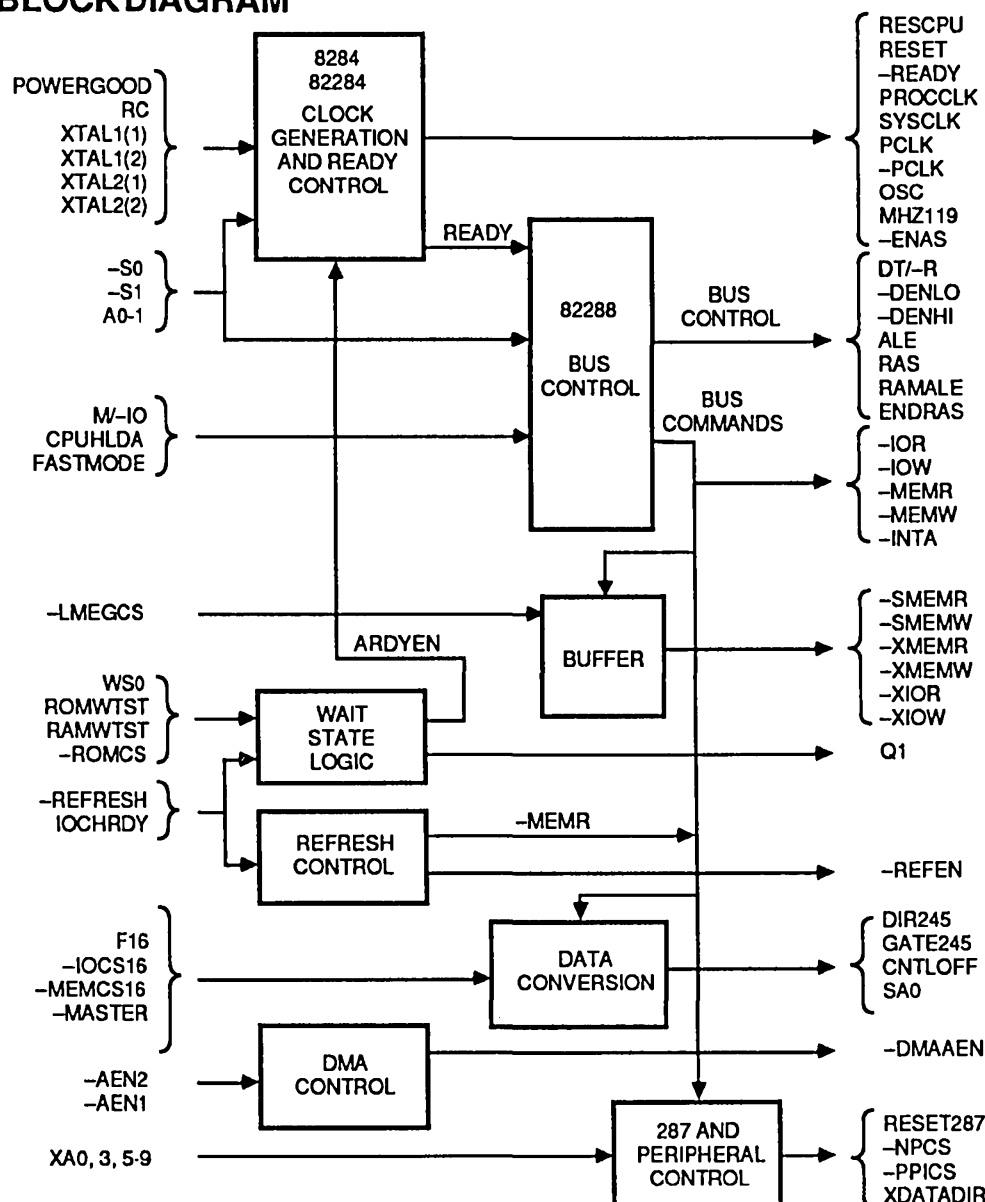
- Fully compatible with IBM PC/AT-type designs
- Replaces 36 integrated circuits on the PC/AT-type board
- Supports 12 MHz processor clock
- Device is available as "cores" for user-specific designs
- Sink 20 mA on slot driver outputs
- Designed in CMOS for low power consumption

DESCRIPTION

The VL82C101A PC/AT-Compatible System Controller replaces an 82C284 Clock Controller and 82C288 Bus Controller (both are used in '86-based systems), an 82C84A Clock Generator and Driver, two PAL16L8 devices (used for memory decode), and approximately ten other less complex integrated circuits used as Wait State logic. When used in 12 MHz systems utilizing 80 ns DRAMs, the device provides the required one wait state for a "write" operation, and zero wait states for a "read" operation. A 12 MHz system using 120 ns DRAMs will be provided with one wait state for "write" and one

wait state for "read". The device accepts both the 24 MHz crystal to control the system clock as well as the 14.318 MHz crystal to control the video clock. It also supplies reset and clock signals to the I/O slots.

The device is manufactured with VLSI's advanced high-performance CMOS process and is available in a JEDEC-standard 84-pin plastic leaded chip carrier (PLCC) package. The VL82C101A is individually available, or may be purchased as part of the complete five-device IBM PC/AT-compatible kit.

BLOCK DIAGRAM

ORDER INFORMATION

Part Number	Package
VL82C101A-QC	Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature is 0°C to +70°C

PLEASE CONSULT PC/AT-COMPATIBLE USERS MANUAL FOR DETAILED INFORMATION

PC/AT-COMPATIBLE MEMORY CONTROLLER

FEATURES

- Fully compatible with IBM PC/AT-type designs
- Completely performs memory control function in IBM PC/AT-compatible systems
- Replaces 20 integrated circuits on PC/AT-type motherboard
- Support 12 MHz processor clock
- Device is available as "cores" for user-specific designs
- Designed in CMOS for low power consumption

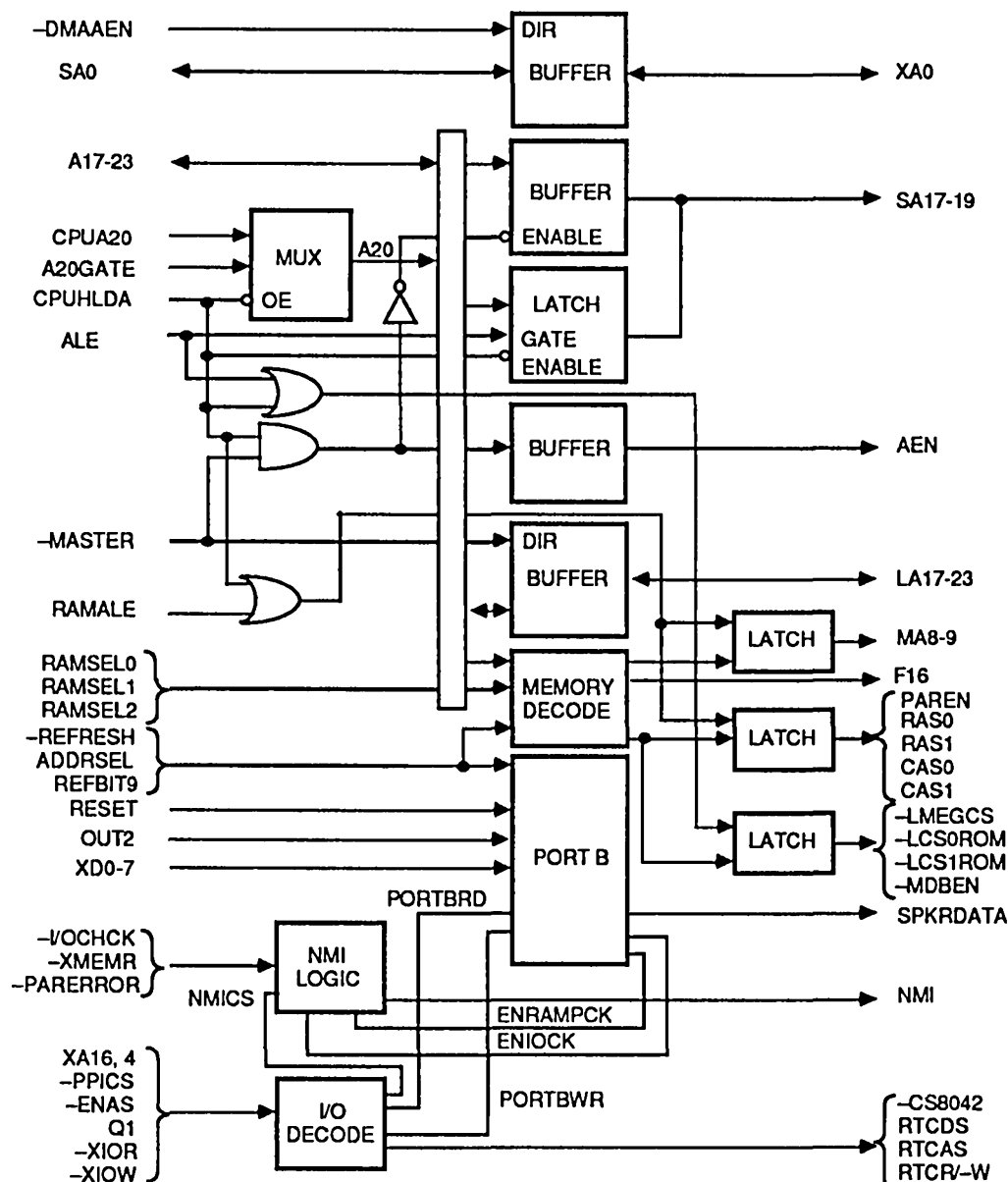
DESCRIPTION

The VL82C102A PC/AT-Compatible Memory Controller generates the row address strobe (RAS) and column address strobe (CAS) necessary to support the dynamic RAMs used in PC/AT-type systems. In addition, the device allows five motherboard memory options for the user, up to a full 4M-byte system. Four of the five options allow a full 640k-bytes user area to support the disk operating system (DOS). In addition, the VL82C102A provides the upper addresses to the I/O slots, the chip select for the ROM and RAM

memory, and drives the system's speaker.

The device is manufactured with VLSI's advanced high-performance CMOS process and is available in a JEDEC-standard 84-pin plastic leaded chip carrier (PLCC) package. The VL82C102A is individually available, or may be purchased as part of the complete five-device IBM PC/AT-compatible kit.

BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Package
VL82C102A-QC	Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range is 0°C to +70°C

PLEASE CONSULT PC/AT-COMPATIBLE USERS MANUAL FOR DETAILED INFORMATION

PC/AT-COMPATIBLE ADDRESS BUFFER
FEATURES

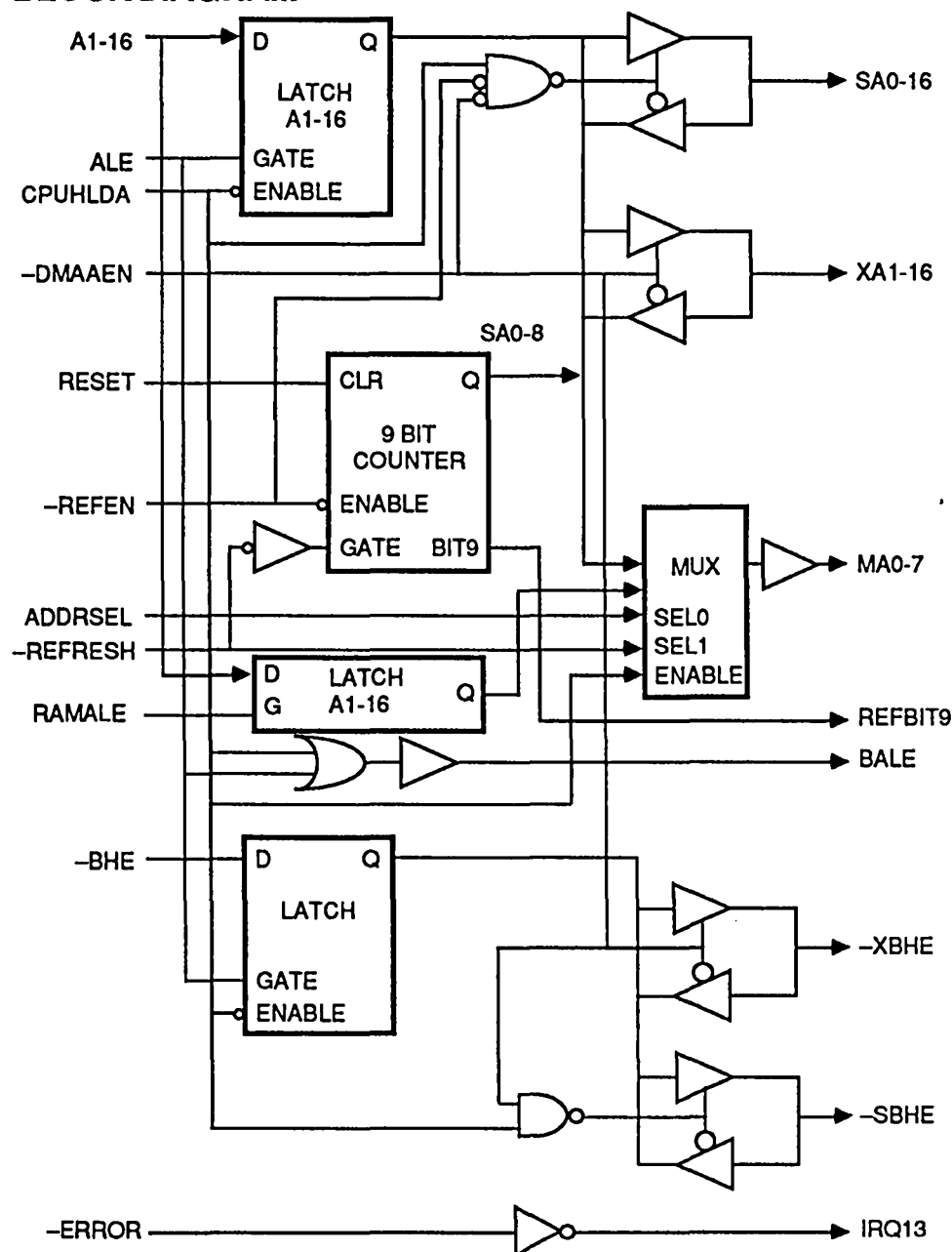
- Fully compatible with IBM PC/AT-type designs
- Completely performs address buffer function in IBM PC/AT-compatible systems
- Replaces several buffers, latches and other logic devices
- Supports 12 MHz processor clock
- Device is available as "cores" for user-specific designs
- Designed in CMOS for low power consumption

DESCRIPTION

The VL82C103 PC/AT-Compatible Address Buffer provides the system with a 16-bit address bus input from the CPU to 41 buffered drivers. The buffered drivers consist of 17 bidirectional system bus drivers, each capable of sinking 20 mA (50 'LS loads) of current and driving 200 pF of capacitance on the backplane; 16 bidirectional peripheral bus drivers, each capable of sinking 8 mA (20 'LS loads) of current; and eight memory bus drivers, also capable of sinking 8 mA of current. On-chip refresh circuitry supports both

256K-bit and 1M-bit DRAMs. The VL82C103 provides addressing for the I/O slots as well as the system.

The device is manufactured with VLSI's advanced high-performance CMOS process and is available in a JEDEC-standard 84-pin plastic leaded chip carrier (PLCC) package. The VL82C103 is individually available, or may be purchased as part of the complete five-device IBM PC/AT-compatible kit.

BLOCK DIAGRAM

ORDER INFORMATION

Part Number	Package
VL82C103-QC	Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range is 0°C to +70°C

PLEASE CONSULT PC/AT-COMPATIBLE USERS MANUAL FOR DETAILED INFORMATION

PC/AT-COMPATIBLE DATA BUFFER

FEATURES

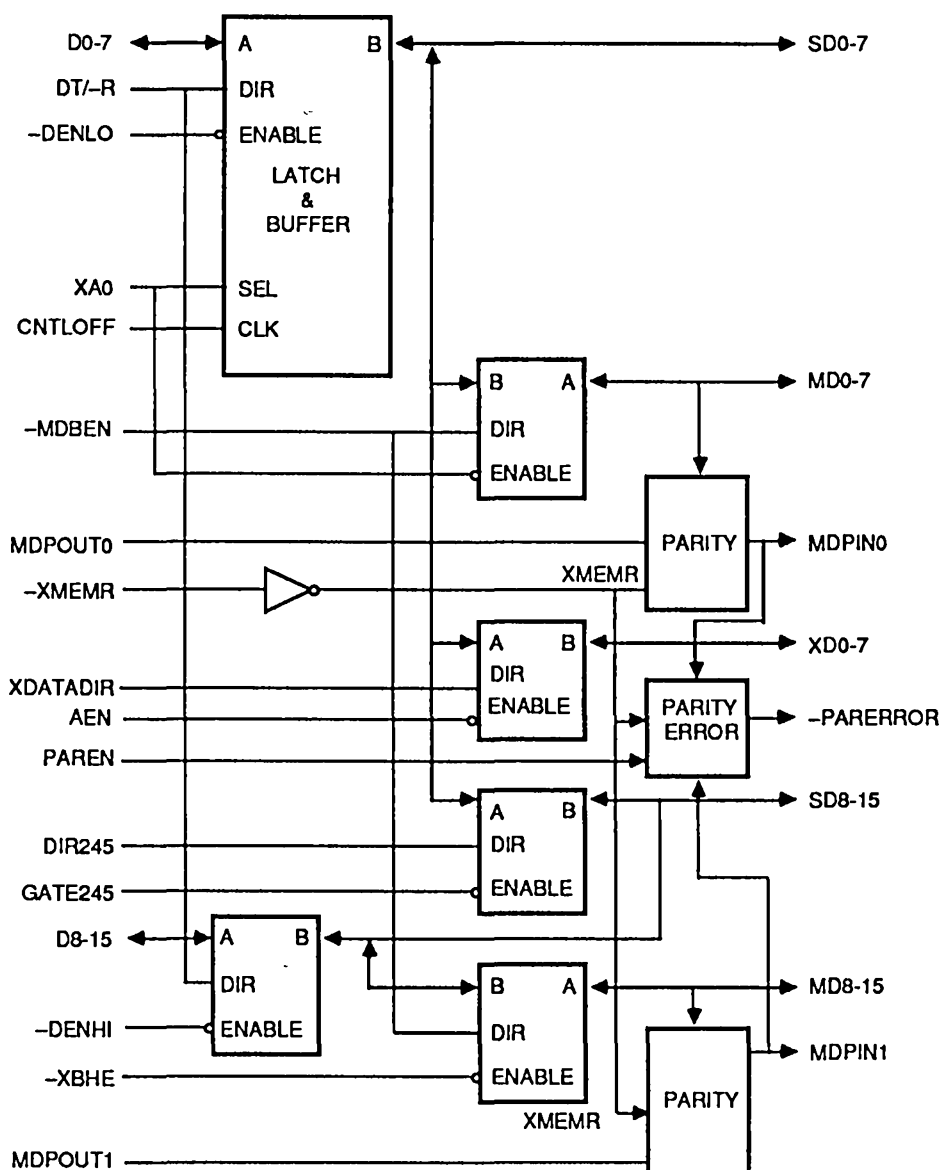
- Fully compatible with IBM PC/AT-type designs
- Completely performs data buffer function in IBM PC/AT-compatible systems
- Replaces several buffers, latches and other logic devices
- Supports 12 MHz processor clock
- Device is available as "cores" for user-specific designs
- Designed in CMOS for low power consumption

DESCRIPTION

The VL82C104 PC/AT-Compatible Data Buffer provides a 16-bit CPU data bus I/O as well as 40 buffered drivers. The buffered drivers consist of 16 bidirectional system data bus drivers, each capable of sinking 20 mA (50 'LS loads) of current; eight bidirectional peripheral bus drivers, each capable of sinking 8 mA (20 'LS loads) of current; and 16 memory data bus drivers, each capable of sinking 8 mA (20 'LS loads) of current. The VL82C104 also generates the parity error signal for the system.

The device is manufactured with VLSI's advanced high-performance CMOS process and is available in a JEDEC-standard 84-pin plastic leaded chip carrier (PLCC) package. The VL82C104 is individually available, or may be purchased as part of the complete five device IBM PC/AT-compatible kit.

BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Package
VL82C104-QC	Plastic Leaded Chip Carrier (PLCC)

Note: Operating Temperature range is 0°C to +70°C

PLEASE CONSULT PC/AT-COMPATIBLE USERS MANUAL FOR DETAILED INFORMATION

12 MHz AND 16 MHz PC/AT-COMPATIBLE SYSTEM CHIP SETS

FEATURES

- Fully compatible with IBM PC/AT-type designs
- High-integration five-chip set
- Reduces non-memory system device count from 110 to 16
- Devices are available as "cores" for user-specific designs
- All devices designed in CMOS for low power consumption
- Supports 12 MHz processor clock
- 16 MHz version of chip set with page mode memory access will be available in 1988

DESCRIPTION

The IBM PC/AT compatible chip set from VLSI Technology, Inc. supports 1-Megabit dynamic RAMs, and is utilized in systems with clock speeds up to 12 MHz. The chip set provides the IBM PC/AT compatible system with a completely compatible low-cost board design solution. Further, since the devices were designed using VLSI's design tools, the devices can be quickly modified for use as cores in user-specific designs.

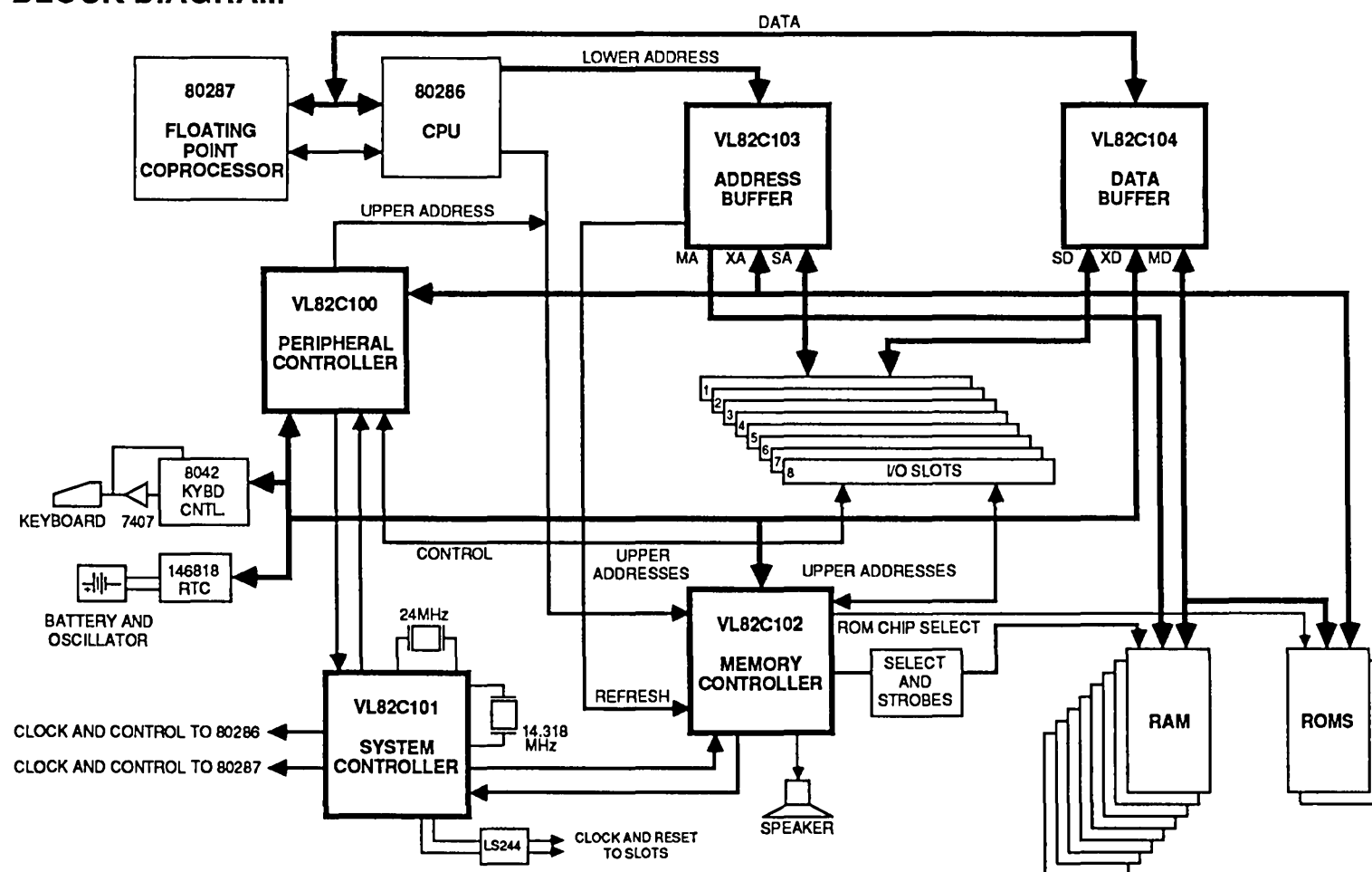
The five device chip set has been designed using the highest integration

consistent with economic and reliable system design. The VL82C103 Address Buffer and VL82C104 Data Buffer are offered in separate packages, although their circuit is relatively small. If they were offered as a single device, the pin count would be extremely high, or some performance degradation would occur.

The devices are manufactured with VLSI's advanced high-performance CMOS process and all five are available in a JEDEC-standard 84-pin plastic leaded chip carrier (PLCC) package.

BLOCK DIAGRAM

MOTHERBOARD BLOCK DIAGRAM



**PLEASE CONSULT THE
PC/AT-COMPATIBLE CHIP
SET USERS MANUAL FOR
DETAILED INFORMATION:**

**VL82CPCAT (12 MHz)
VL82CPCPM (16 MHz)**

ORDER INFORMATION

Part Number	Clock Frequency	Package
VL82CPCAT-QC	12 MHz	(5 Chips) Plastic Leaded Chip Carrier (PLCC)
VL82CPCPM-QC	16 MHz	(6 Chips) Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range is 0°C to +70°C

CMOS CLOCK GENERATOR AND INTERFACE

FEATURES

- Generates clock for Intel 286-type microprocessor-based systems
- External TTL source or crystal may be used as frequency source
 - On-board crystal oscillator
- Provides Local $\overline{\text{READY}}$ signal for system synchronization
- Generates system reset
- Schmitt-trigger reset input assures stability and noise immunity
- Low power consuming CMOS technology

DESCRIPTION

The VL82C284 is a clock generator and driver that provides clock and interface signals to Intel 286-type microprocessor-based systems. All device output signals are synchronized to the output clock signal.

The clock input and output frequencies are twice the frequency used internally by the microprocessor in the system. To avoid confusion, the clock frequency in the order information represents the internal system microprocessor clock frequency (e.g., the devices listed as 8 MHz would actually have an input

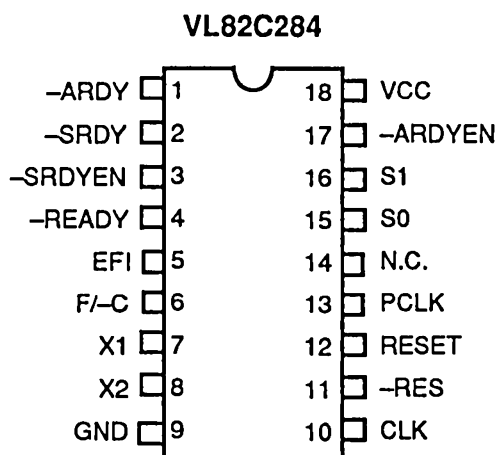
crystal or a TTL signal frequency of 16 MHz).

The VL82C284 also supplies the system with a high-noise-immunity reset, as well as a synchronous peripheral clock and a synchronous $\overline{\text{READY}}$ to indicate the completion of the current bus cycle.

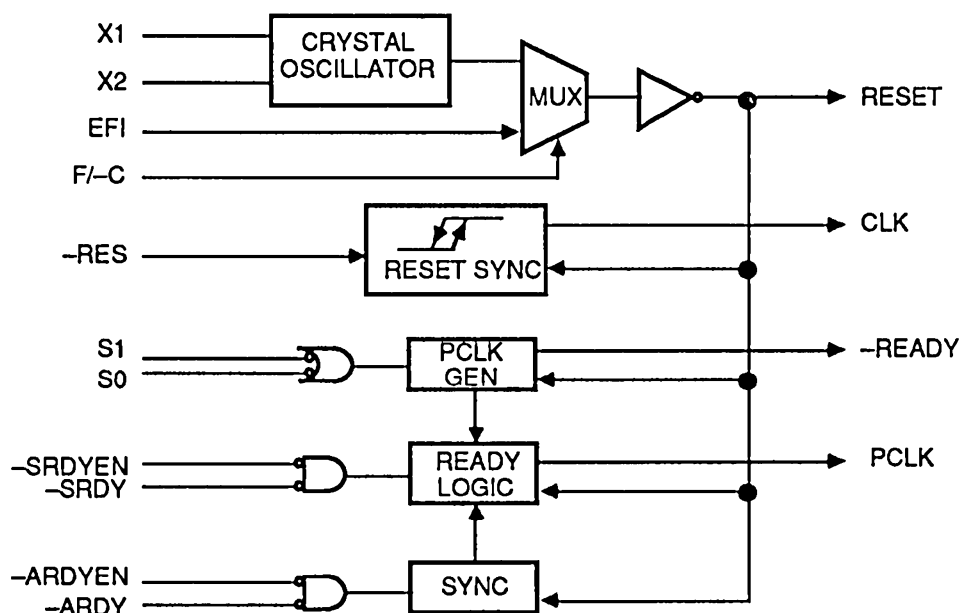
The peripheral clock is controlled by two status input signals, which may be left open if not used.

The VL82C284 is available in an 18-pin ceramic and plastic DIP, as well as in a plastic leaded chip carrier.

PIN DIAGRAM



BLOCK DIAGRAM



PLEASE CONSULT DATA SHEET FOR DETAILED INFORMATION

ORDER INFORMATION

Part Number	Clock Frequency	Package
VL82C284-08PC	8 MHz	Plastic DIP
VL82C284-08QC		Plastic Leaded Chip Carrier (PLCC)
VL82C284-08CC		Ceramic DIP
VL82C284-10PC	10 MHz	Plastic DIP
VL82C284-10QC		Plastic Leaded Chip Carrier (PLCC)
VL82C284-10CC		Ceramic DIP

Note: Operating temperature range is 0°C to +70°C.

VL82C288

CMOS BUS CONTROLLER

FEATURES

- Both local and system bus commands and control are provided
- Supports both Multibus® and high-speed bus cycle operating modes
- High-current output drivers
- Flexible command timing
- High degree of system configuration flexibility
- Low power consuming CMOS technology
- Single 5 V power supply

DESCRIPTION

The VL82C288 is a CMOS bus controller for use in Intel 286-type microprocessor-based systems. A mode select pin allows strapping the device for Multibus operation or for short bus cycles. The device also provides separate command outputs for memory and I/O devices. The data bus is controlled by separate data direction and data enable signals.

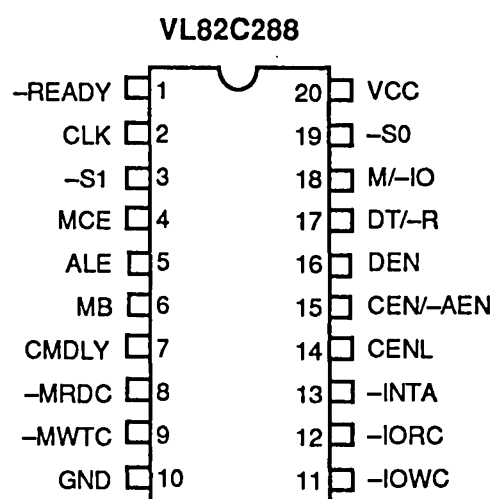
A system clock provides the timing control required by the microprocessor-based system. The device clock input is

twice the system clock speed. To avoid confusion, the clock frequency listed in the order information is the system clock frequency (e.g., the devices listed as 8 MHz Clock Frequency, would have an input clock of 16 MHz).

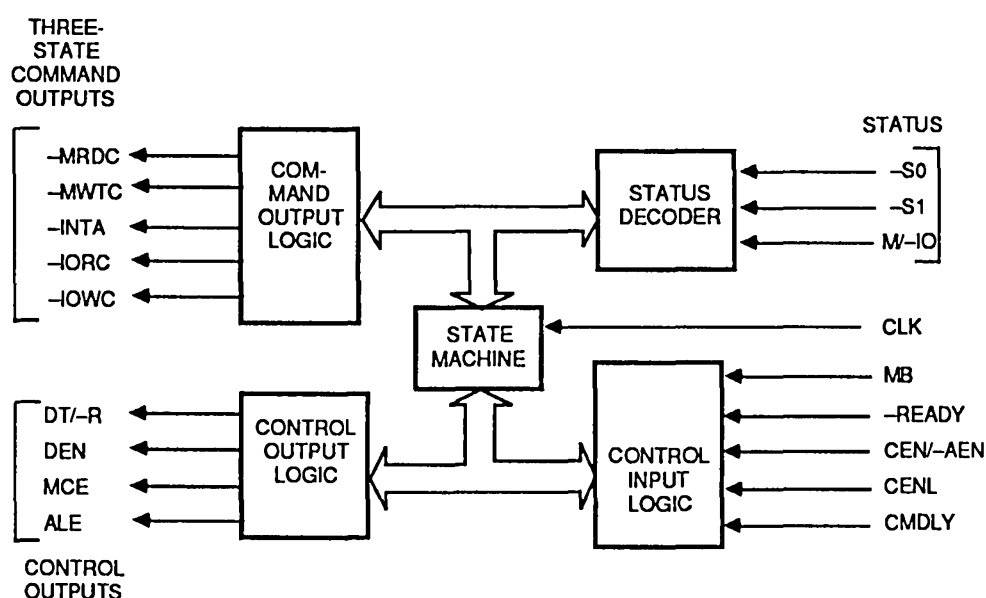
The VL82C288 meets the timing and drive requirements to satisfy the IEEE-796 standard for Multibus.

The VL82C288 is available in a 20-pin ceramic or plastic DIP, as well as in a plastic leaded chip carrier.

PIN DIAGRAM



BLOCK DIAGRAM



PLEASE CONSULT DATA SHEET FOR DETAILED INFORMATION

ORDER INFORMATION

Part Number	Clock Frequency	Package
VL82C288-06PC VL82C288-06QC VL82C288-06CC	6 MHz	Plastic DIP Plastic Leaded Chip Carrier (PLCC) Ceramic DIP
VL82C288-08PC VL82C288-08QC VL82C288-08CC	8 MHz	Plastic DIP Plastic Leaded Chip Carrier (PLCC) Ceramic DIP

Note: Operating temperature range is 0°C to +70°C.

CMOS DIRECT MEMORY ACCESS (DMA) CONTROLLER

FEATURES

- Low-power CMOS version of popular 8237A DMA controller
- Four DMA channels
- Individual enable/disable control of DMA requests
- Directly expandable to any number of channels
- Independent auto-initialize feature for all channels
- High performance 8 MHz version available
- Transfers may be terminated by end-of-process input
- Software controlled DMA requests
- Independent polarity control for DREQ and DACK signals

DESCRIPTION

The VL82C37A Direct Memory Access (DMA) Controller serves as a peripheral interface circuit for microprocessor systems, and is designed to improve system performance by allowing external devices to directly transfer information from the system memory. Memory-to-memory transfer capability is also provided. The VL82C37A DMA Controller offers many programmable control features that enhance data throughput and system performance. Dynamic reconfiguration is permitted under program control.

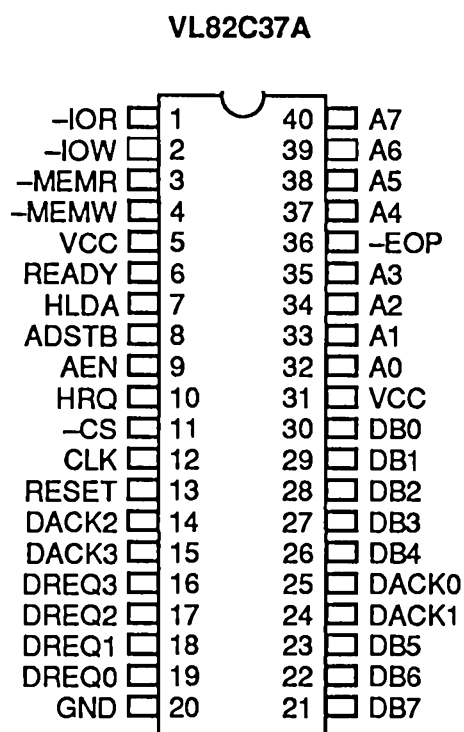
The VL82C37A is designed to be used with an external 8-bit address register

such as the 8282. In addition to the four independent channels, the VL82C37A is expandable to any number of channels by cascading additional controller devices.

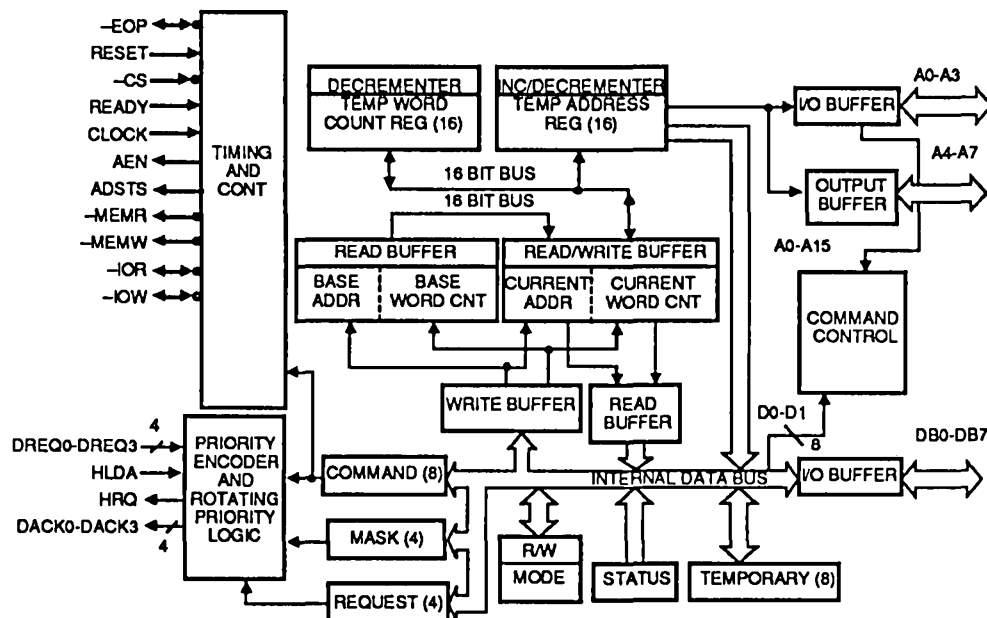
Three basic transfer modes allow the user to program the types of DMA service. Each channel can be individually programmed to auto-initialize to its original condition following an end-of-process (EOP) input. Each channel also has a 64K address and word count handling ability.

The VL82C37A DMA Controller is available in 5 MHz and 8 MHz clock frequencies.

PIN DIAGRAM



BLOCK DIAGRAM

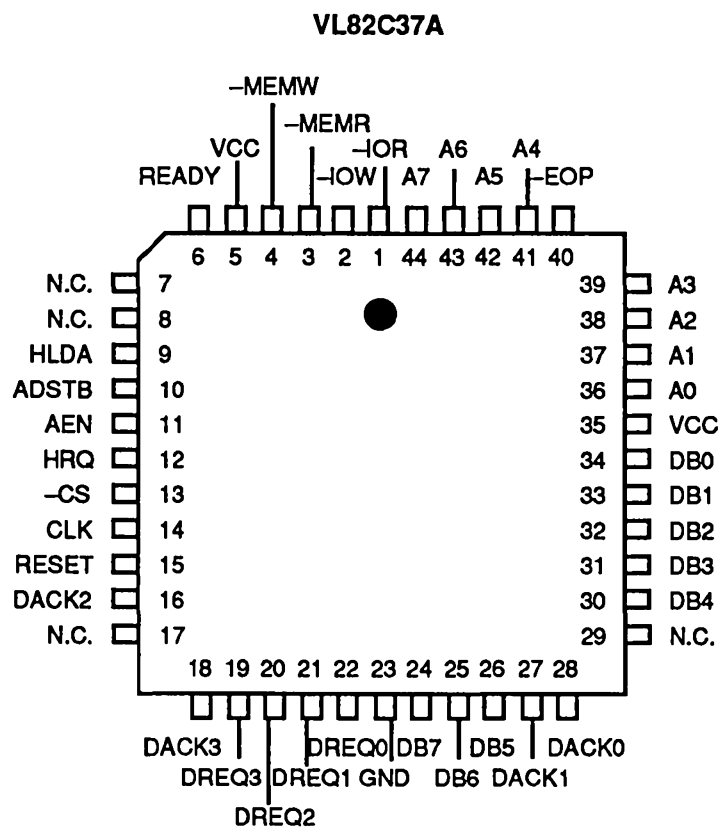


ORDER INFORMATION

Part Number	Clock Frequency	Package
VL82C37A-05PC	5 MHz	Plastic DIP
VL82C37A-05CC		Ceramic DIP
VL82C37A-05QC		Plastic Leaded Chip Carrier (PLCC)
VL82C37A-08PC	8 MHz	Plastic DIP
VL82C37A-08CC		Ceramic DIP
VL82C37A-08QC		Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range is 0°C to +70°C.

PIN DIAGRAM



SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Description
CLK	12	Clock Input: Controls the internal operations of the VL82C37A DMA Controller and its rate of data transfers. This input may be driven at up to 4 MHz for the standard VL82C37A-04 and up to 8 MHz for the VL82C37A-08.
-CS	11	Chip Select: An active low input used to select the VL82C37A as an I/O device during the idle cycle, allows CPU communication on the data bus.
RESET	13	Reset: An active high input that clears the Command, Request, and Temporary Registers, clears the first/last flip-flop, and sets the Mask Register. The device is in the idle cycle following a Reset signal.
READY	6	Ready: An input that extends the memory read and write pulses from the VL82C37A accommodating slow memories or I/O peripheral devices. During its specified setup/hold time, READY must not make transitions.
HLDA	7	Hold Acknowledge: This active high signal from the CPU indicates that it has relinquished control of the system busses.
DREQ0-DREQ3	19 - 16	DMA Request: These lines are individual asynchronous channel request inputs. Peripheral circuits use these lines to obtain DMA service. In fixed Priority, DREQ0 has the highest priority and DREQ3 has the lowest priority. Activating the DREQ line of a channel generates a request. DACK then acknowledges the recognition of DREQ signal. Polarity of DREQ is programmable. Reset initializes these lines to active high. DREQ must be sustained until the corresponding DACK becomes active.
DB0 - DB7	30 - 26, 23 - 21	Data Bus: These lines are bidirectional, three-state signals that connect to the system data bus. The outputs are enabled in the program condition during the I/O read to output the contents of an Address Register, a Status Register, the Temporary Register, or a Word Count Register to the CPU. The outputs are disabled and the inputs are read during an I/O Write cycle when the CPU is programming the VL82C37A control registers. During DMA cycles the most significant eight bits of the address are sent onto the data bus and are strobed into an external latch by ADSTB. In memory-to-memory operations, data from the memory comes into the VL82C37A on the data bus during the read-from-memory transfer. In the write-to-memory transfer, the data bus outputs determine the placement of the data, not the new memory location.
-IOR	1	I/O Read: This is a bidirectional, active low, three-state line. In the idle cycle, it is an input control signal used by the CPU to read the control registers. In the active cycle, it is an output control signal used by the VL82C37A to access data from a peripheral during a DMA Write transfer.
-IOW	2	I/O Write: This signal is a bidirectional active low, three-state line. It is used by the CPU to load information into the VL82C37A DMA Controller. In the active cycle, it is used as an output control signal used by the VL82C37A to load data to the peripheral during a DMA read transfer.
-EOP	36	End of Process: This is an active low bidirectional signal, which provides data on the completion of DMA services and is available at the bidirection -EOP pin. The VL82C37A allows an external signal to terminate an active DMA service, by pulling the -EOP input low with an external -EOP signal. The VL82C37A also generates a pulse when the terminal count (TC) for any channel is achieved. This generates an -EOP signal that is active on the -EOP Line. When -EOP is received, either internally or externally, it will cause the VL82C37A to terminate the service, reset the request, and, if auto-initialize is enabled, to write the base registers to the current registers of that channel. The mask bit and TC bit in the status word will be set for the currently active channel by -EOP, unless the channel is programmed for auto-initialize. In that case, the mask bit remains unchanged. During memory-to-memory transfers, -EOP will be output when the TC for channel 1 occurs. To prevent erroneous end-of-process inputs, -EOP should be tied high with a pull-up resistor if it is not used.

**SIGNAL DESCRIPTIONS (CONT.)**

Signal Name	Pin Number	Signal Description
A0 - A3	32 - 35	The four least significant address lines: These lines are bidirectional three-state signals. In the idle cycle, they are inputs used by the CPU to address the register to be loaded or read. In the active cycle they are outputs that provide the lower four bits of the output address to the system.
A4 - A7	37 - 40	The four most significant address lines: These lines are three-state outputs that provide four bits of address. They are enabled only during the DMA service.
HRQ	10	Hold Request: This is the hold request to the CPU. It is used to request control of the system bus. If the corresponding mask bit is clear, the presence of any valid DREQ causes the VL82C37A to issue the HRQ signal. After HRQ is asserted, at least one clock cycle (TCY) must occur before HLDA can be valid.
DACK0 - DACK3	25, 24, 14, 15	DMA Acknowledge: This signal is used to notify an individual peripheral when it has been granted a DMA cycle. The sense of these lines is programmable; Reset initializes them to an active low.
AEN	9	Address Enable: This active high line enables the 8-bit latch containing the upper eight address bits onto the system address bus. It can also be used to disable other system bus drivers during DMA transfers.
ADSTB	8	Address Strobe: This active high is used to strobe the upper address byte into an external latch.
-MEMR	3	Memory Read: This active low signal is a three-state output used to access data from a selected memory location during a DMA read or memory-to-memory transfer.
-MEMW	4	Memory Write: This signal is an active low three-state output used to write data to a selected memory location during a DMA write or memory-to-memory transfer.
VCC	5, 31	+5 V \pm 5% power supply.
GND	20	Ground.

TABLE 1. INTERNAL REGISTERS

Name	Size	Number
Base Address Registers	16 bits	4
Base Word Count Registers	16 bits	4
Current Address Registers	16 bits	4
Current Word Count Registers	16 bits	4
Temporary Address Register	16 bits	1
Temporary Word Count Register	16 bits	1
Status Register	8 bits	1
Command Register	8 bits	1
Temporary Register	8 bits	1
Mode Registers	6 bits	4
Mask Register	4 bits	1
Request Register	4 bits	1

FUNCTIONAL DESCRIPTION

The internal registers and major logic blocks of the VL82C37A are shown in the block diagram. Data interconnection paths are also shown, but the various control signals between the blocks are not. The VL82C37A contains 344 bits of internal register memory. Figure 3 describes these registers and shows them by size. A complete description of the registers and their functions can be found in the Register Descriptions section.

The VL82C37A contains three basic control logic blocks. The Timing Control block generates internal timing and external control signals for the VL82C37A. The program command control block decodes the various commands given to the VL82C37A by the microprocessor before servicing a DMA Request. Further, it decodes the mode control word used to select the type of DMA during the servicing. The priority encoder block settles priority contention between DMA channels requesting service at the same time.

The external clock drives the timing control block. In most VL82C37A systems, this clock will usually be the $\varnothing 2$ TTL clock from an VL82C84A. For 8085AH-2 systems above 3.9 MHz, the 8085 CLK(OUT) will not meet VL82C37A-05 (5 MHz) clock low and high time requirements. In this case, an external clock should be used to drive the VL82C37A-05.

DMA OPERATION

The VL82C37A is designed to operate in two major cycles: the idle and active. Several states are contained in each device cycle. The VL82C37A supports seven separate states, each being one full clock period. State I (SI), the inactive state, is entered when the VL82C37A has no valid DMA requests pending. While in SI, the DMA controller is inactive but may be in the program condition, being programmed by the processor. State 0 (S0) is the first state of a DMA service. The VL82C37A has requested a hold, but the processor has not yet responded with an acknowledge. The VL82C37A may still be programmed until it receives HLDA from the CPU. An acknowledge from the CPU

signals that DMA transfers may begin. S1, S2, S3 and S4 are the functional states of the DMA service. If more time is needed to complete a transfer than is available with normal timing, wait states (WS) can be placed between S2 or S3 and S4 by using the Ready line on the VL82C37A. The data is transferred directly from the I/O device to memory (or vice versa) with -IOR and -MEMW (or -MEMR and -IOW) being active simultaneously. The data is not read into or driven out of the VL82C37A during I/O-to-memory or memory-to-I/O DMA transfers.

To complete memory-to-memory transfers requires a read-from and a write-to-memory. The states, which resemble the normal working states, use two-digit numbers for identification. Eight states are needed for each transfer: the first four states (S11, S12, S13, S14), are used for read-from-memory and the last four states (S21, S22, S23, S24), for the write-to-memory of the transfer.

IDLE CYCLE

When no channels are requesting service, the VL82C37A enters the idle cycle and performs SI states, sampling the DREQ lines every clock cycle to determine if any channel is requesting a DMA service. The device also samples -CS , looking for an attempt by the microprocessor to write or read to the internal registers of the VL82C37A. When -CS is low and HLDA is low, the VL82C37A initiates the program condition. The CPU now establishes, changes or inspects the internal definition of the part by reading from or writing to the internal register. Address lines A0-A3 are inputs to the device. They select registers that will be read or written. The -IOR and -IOW lines are used to select and time reads or writes. Because of the number and size of the internal registers, an internal flip-flop is used to generate one more bit of address. This bit is used to determine the upper or lower byte of the 16-bit address and Word Count Registers. This flip-flop can be reset by a separate software command.

Special software commands executed in the VL82C37A during the program condition are decoded as sets of addresses with the -CS and -IOW signals. The commands do not use the data bus. Clear First/Last Flip-Flop and Master Clear instructions are included.

ACTIVE CYCLE

When the VL82C37A is in the idle cycle and a nonmasked channel requests a DMA service, the device outputs an HRQ to the microprocessor and then enters the active cycle. During this cycle the DMA service takes place, in one of four modes.

In the single transfer mode, the device is programmed to make only one transfer. The word count is decremented and the address decremented or incremented, following each transfer. When the word count is completed from zero to FFFFH, a Terminal Count (TC) causes an auto-initialize if the channel has been so programmed.

The DREQ signal must be held active until DACK becomes active, in order to be recognized. If DREQ is held active for the entire single transfer, HRQ will become inactive and release the bus to the system. It again goes active and, upon receipt of a new HLDA, another single transfer is performed. In 8080A, 8085AH, 8088, or 8086 systems this insures one full machine cycle execution between DMA transfers. Details of timing between the VL82C37A and other bus control protocols depends upon the characteristics of the microprocessor involved.

In the block transfer mode, the device is activated by the DREQ signal to continue making transfers during the service until a TC, caused by word count going to FFFFH, or an external end of process (-EOP) is encountered. DREQ need only be held active until DACK becomes active. An auto-initialization will occur at the end of the service, if the channel has been programmed for it.

In the demand transfer mode the device is programmed to continue making transfers until a TC or external -EOP is encountered or until the DREQ signal goes inactive. Transfers may continue



until the I/O device has exhausted its data capacity. After the I/O device has caught up, the DMA service is re-established by a DREQ signal. During the interval between services, when the microprocessor is operating, the intermediate values of address and word count are stored in the VL82C37A Current Address and Current Word Count Registers. Only an -EOP can cause an auto-initialize at the end of the service. EOP is generated either by TC or by an external signal.

The fourth mode cascades multiple VL82C37As together for easy system expansion. The HRQ and HLDA signals from additional VL82C37As are connected to the DREQ and DACK signals of a channel of the primary VL82C37A. This permits the DMA requests of the additional device to propagate through the priority network circuitry of the preceding device. The priority chain is not broken, and the new device waits for its turn to acknowledge requests. As the cascade channel of the primary VL82C37A is used only to prioritize the additional device, it does not produce any address or control signals of its own, which could conflict with the outputs of the active channel in the added device. The VL82C37A responds to the DREQ and DACK signal, but all other outputs except HRQ are disabled.

Figure 8 shows two devices cascaded into a primary device using two of the previous channels. This forms a two-level DMA system. More VL82C37A's could be added at the second level by using the remaining channels of the first level. More devices can also be cascaded into the channels of the second-level devices, forming a third level.

TRANSFER TYPES

Each of the three modes of active transfer can perform three different types of transfers: read, write and verify. Write transfers move data from an I/O device to the memory by activating -MEMW and -IOR; read transfers move data from memory to an I/O device by activating -MEMR and -IOW.

Verify transfers are pseudo routines: the VL82C37A DMA Controller operates as in read or write transfers generating addresses, and responding to -EOP,

and other operations. The memory and I/O control lines remain inactive. The verify mode is not permitted during memory-to-memory operation.

To perform block moves of data from one memory address space to another with a minimum of programming, the VL82C37A includes a memory-to-memory transfer feature. Programming a bit in the Command Register selects channels 0 and 1 to operate as memory-to-memory transfer channels. The transfer is initiated by setting the software DREQ for channel 0. The VL82C37A requests a DMA device as usual. After HLDA is true, the device, using eight-state transfers in block transfer mode, reads data from the memory. The channel 0 Current Address Register is the source for the address, and is decremented or incremented as usual. The data byte read from the memory is then stored in the VL82C37A internal Temporary Register. Channel 1 writes the data from the Temporary Register to memory using the address in its Current Address Register and incrementing or decrementing it as usual. The channel 1 current word count is decremented. When the word count goes to FFFFH, a TC is generated causing an -EOP output terminating the service.

Channel 0 may be programmed to hold the same address for all transfers, which permits a single word to be written to a block of memory.

The VL82C37A responds to external -EOP signals during memory-to-memory transfers. In block search schemes data comparators may use this input on finding a match. The timing of memory-to-memory transfers is shown in Figure 10. Memory-to-memory operations can be detected as an active AEN signal with no DACK outputs.

A channel may be set up to auto-initialize by setting a bit in the Mode Register. During initialization, the original values of the Current Address and Current Word Count Registers are automatically restored from the Base Address and Base Word Count Registers of that channel following -EOP. The base registers and the current registers are loaded at the same time. They remain unchanged throughout the

DMA service. The mask bit is not set when the channel is in auto-initialize. Following auto-initialize, the channel is prepared to perform another DMA service, without CPU action, as soon as a valid DREQ is detected.

The VL82C37A has two types of priority encoding available as software-selectable options. The fixed priority option sets the channels in priority order based upon the descending value of their number. The channel with the lowest priority is 3, then 2, 1 and the highest priority channel is 0. After recognizing any one channel for service, the other channels are prevented from interfering with that service until it is completed.

In the rotating priority option, the last channel to get service becomes the lowest priority channel with the others rotating in order.

Rotating priority allows a single chip DMA system. Any device requesting service is guaranteed to be recognized after no more than three higher priority services have occurred. This prevents any one channel from dominating the system.

To achieve even greater throughput where system characteristics permit, the VL82C37A DMA Controller can compress the transfer time to two clock cycles. State S3 is used to extend the access time of the read pulse. By removing state S3, the read pulse width is made equal to the write pulse width, and a transfer consists only of state S2 to change the address and state S4 to perform the read/write. S1 state still occurs when A8-A15 need updating (see the Address Generation section.)

To reduce pin count, the VL82C37A multiplexes the eight higher order address bits on the data lines. State S1 is used to output the higher order address bits to an external latch, where they may be placed on the address bus. The falling edge of the Address Strobe (ADSTB) is used to load these bits from the data lines to the latch. Address Enable (AEN) is used to enable the bits onto the address bus through a three-state enable. The lower order address bits are directly sent by the VL82C37A. Lines A0-A7 are connected to the address bus.

During block and demand transfer mode services, including multiple transfers, the addresses generated will be in order. During a large number of transfers the data held in the external address latch will not change. This data will change when a carry or borrow from A7 to A8 takes place in the normal order of addresses. To expedite transfers, the VL82C37A DMA Controller executes S1 states only when needed to update A8-A15 in the latch. For long services, S1 states and address strobes may occur only once every 256 transfers, a savings of 255 clock cycles for each 256 transfers.

REGISTER DESCRIPTION

Current Address Register: Each channel has a 16-bit Current Address Register. This register holds the value of the address used during DMA transfers. The address is automatically incremented or decremented after each transfer and the intermediate values of the address are stored in the Current Address Register throughout the transfer. The microprocessor reads this register in successive 8-bit bytes. It may also be reinitialized by an auto-initialize to its original value which takes place only after an -EOP.

Current Word Register: Each channel has a 16-bit Current Word Count Register that determines the number of transfers to be performed. The actual number of transfers is one more than the number programmed in the Current Word Count Register; programming a count of 100 will result in 101 transfers. The word count is decremented after each transfer; the intermediate value of this word count is stored in the register during the transfer. When the value in the register goes from 0 to FFFFH, a TC is generated. The register is then loaded or read in successive 8-bit bytes by the microprocessor in the program condition. Following the end of a DMA service, it may also be reinitialized by an auto-initialization to its original value which occurs only on -EOP. If it is not auto-initialized, this register has a count of FFFFH after TC.

Base Address and Base Word Count Registers: Each channel has a pair of 16-bit Base Address and Base Word Count Registers that store the original value of their associated current

registers. Throughout auto-initialization these values are used to restore the current registers to their original values. The base registers are written at the same time with their corresponding current register in 8-bit bytes in the program condition by the microprocessor. These registers cannot be read by the microprocessor.

Command Register: This 8-bit register controls the operation of the VL82C37A, is programmed by the microprocessor in the program condition and is cleared by reset or a master clear instruction. Figure 2 lists and describes the function of the command bits.

Mode Register: All channels have a 6-bit Mode register. When the register is being written to by the microprocessor in the program condition, bits 0 to 1 determine which channel the Mode Register is to be written.

Request Register: The VL82C37A can respond to requests for DMA service that are initiated by software as well as by a DREQ signal. Each channel has a request bit associated with it in the 4-bit Request Register. These are non-maskable and can be prioritized by the priority encoder network.

Each register bit is set or reset separately under software control, or is cleared upon generation of a TC or external -EOP. The entire register is cleared by a Reset. To set or reset a bit, the software loads the correct form of the data word. Table 2 shows register address coding. To make a software request, the channel must be in block mode.

Mask Register: Each channel has an associated mask bit that can be set to disable the incoming DREQ signal. A mask bit is set when its associated channel produces an -EOP, if the channel is not programmed for auto-initialize. Any bit of the 4-bit Mask register may also be set or cleared separately under software control. The entire register is set by a reset, which disables all DMA requests until a clear Mask Register instruction allows them to occur. This instruction to separately set or clear the mask bits is similar in form to that used with the Request Register.

Status Register: The Status Register is available to be read out of the VL82C37A DMA Controller by the microprocessor and contains information about the status of the devices at this point. This information includes which channels have reached a terminal count and which channels have pending DMA requests.

Bits 0-3 are set each time a TC is reached by that channel or an external -EOP is applied and are cleared upon reset and on every status read. Bits 4 through 7 are set whenever their corresponding channel is requesting service.

Temporary Register: The Temporary Register is used to hold data during memory-to-memory transfers. The last word moved can be read by the microprocessor in the Program Condition following the completion of the transfers. The Temporary Register always contains the last byte transferred in the previous memory-to-memory operation, unless cleared by a reset.

Software Commands: These additional special software commands can be executed in the program condition and do not depend on any specific bit pattern on the data bus.

The clear first/last flip-flop command is executed prior to writing or reading new address or word count information to the VL82C37A. This initializes the flip-flop to a known state so that subsequent accesses to register contents by the microprocessor will address upper and lower bytes in the correct sequence.

The Master Clear software instruction has the same effect as the hardware reset. The Command, Status, Request, Temporary, and Internal First/Last Flip-Flop Registers are cleared and the Mask Register is set. The VL82C37A enters an idle cycle.

The Clear Mask Register command clears the mask bits of all four channels, enabling them to accept DMA requests.

PROGRAMMING

The VL82C37A DMA Controller accepts programming from the host processor any time that HLDA is inactive, even if the HRQ signal is active. The host must assure that programming and HLDA are

mutually exclusive. A problem can occur if a DMA request occurs, on an unmasked channel while the VL82C37A is being programmed.

For example, the CPU may be starting to reprogram the two-byte Address Register of a channel when that channel receives a DMA request. If the

VL82C37A is enabled (bit 2 in the command register is 0) and that channel is unmasked, a DMA service will occur after one byte of the Address Register has been reprogrammed. This can be avoided by disabling the controller - setting bit 2 in the command register - or masking the channel before

programming another registers. Once the programming is complete, the controller can be enabled (unmasked).

After power-up all internal locations, including the Mode registers, should be loaded with a valid value. This should be done to unused channels as well.

APPLICATION

Figure 1 shows a convenient method for configuring a DMA system with the VL82C37A DMA Controller and an 8080A/8085AH microprocessor system. Whenever there is at least one valid DMA request from a peripheral device, the multimode VL82C37A DMA Controller issues a HRQ to the processor.

When the processor replies with a HLDA signal, the VL82C37A takes control of the address, data, and control buses. The address for the first transfer operation is output in two bytes - the least significant eight bits on the eight address outputs, and the most significant eight bits on the data bus. The contents of the data bus are then

latched into the 8282 8-bit latch to complete the full 16 bits of the address bus. The 8282 is a high-speed, 8-bit, three-state latch in a 20-pin DIP package. After the initial transfer takes place, the latch is updated only after a carry or borrow is generated in the least significant address byte. Four DMA channels are available when one VL82C37A DMA Controller is used.

FIGURE 1. SYSTEM INTERFACE

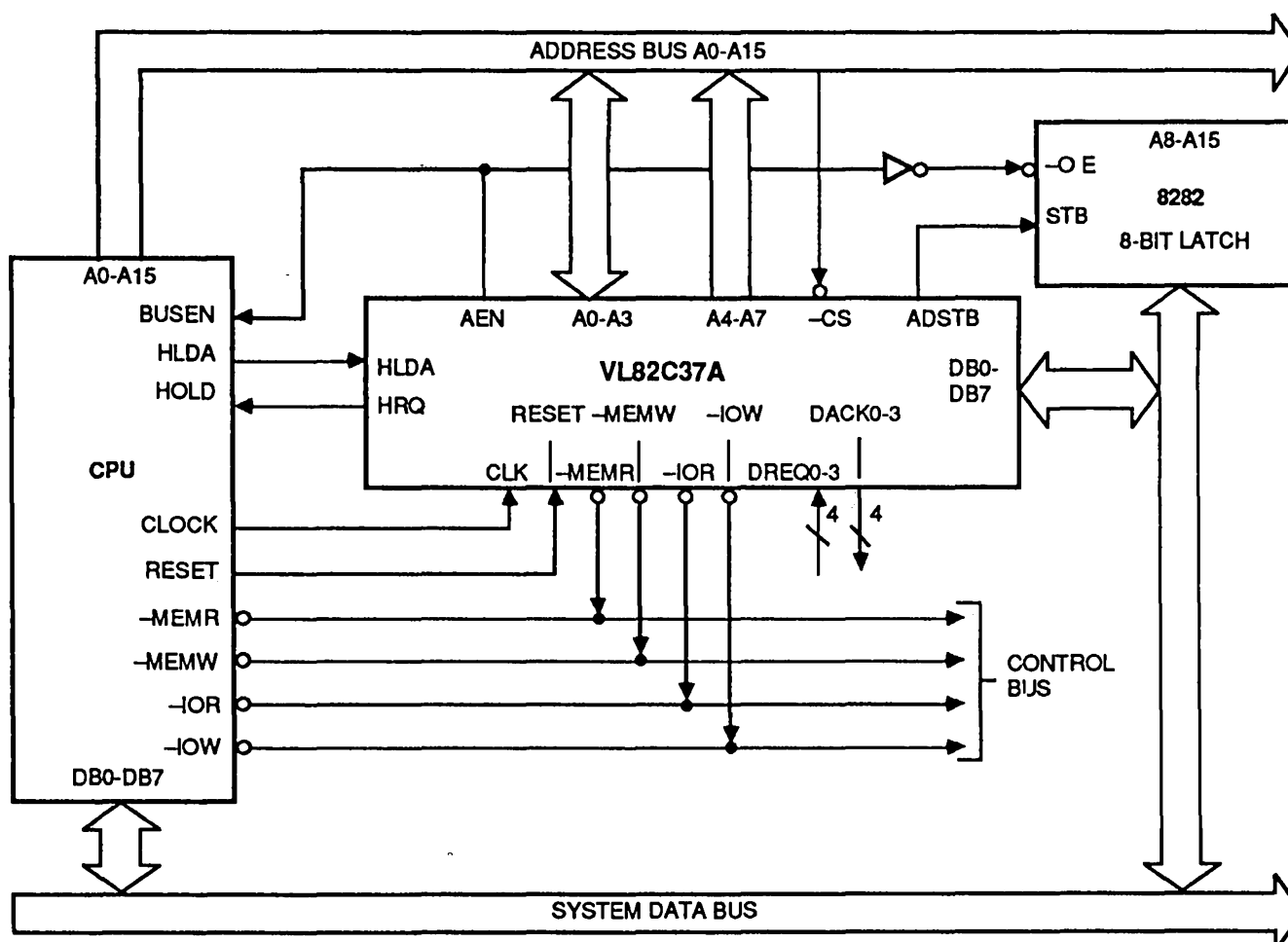


FIGURE 2. COMMAND REGISTER

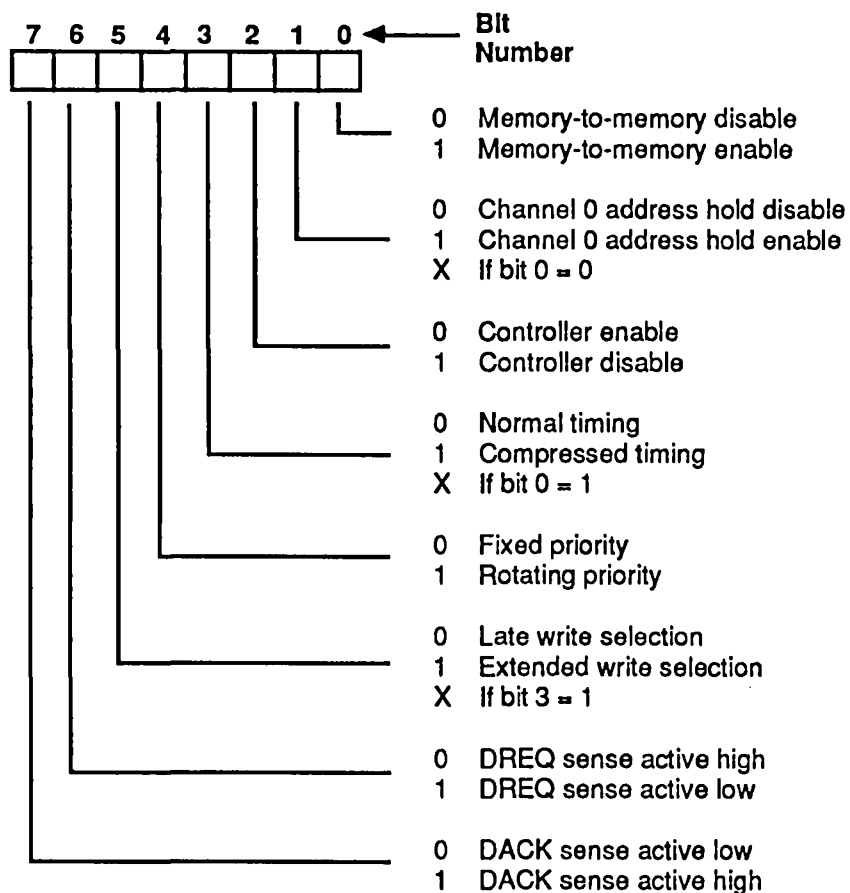


FIGURE 3. MODE REGISTER

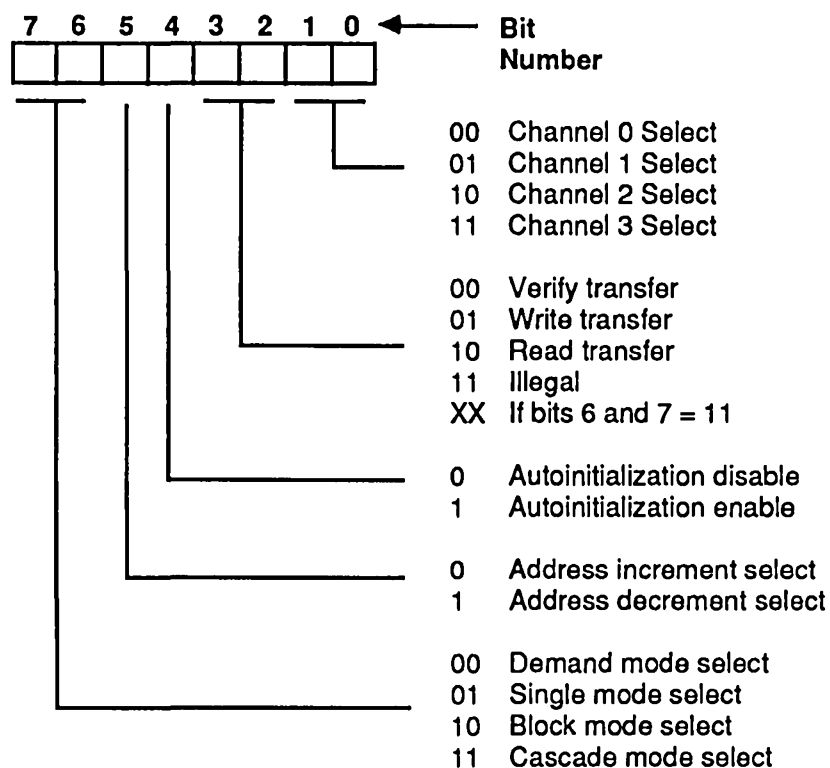


FIGURE 4. REQUEST REGISTER

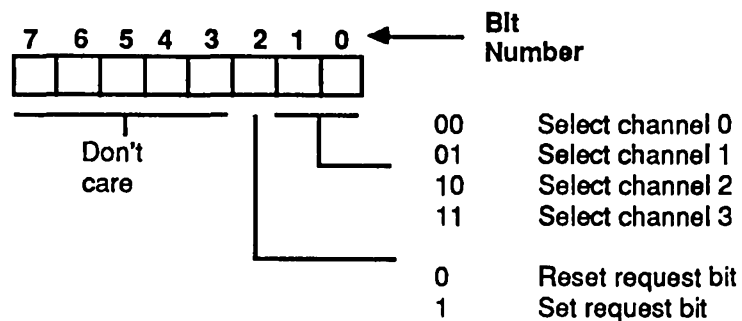


FIGURE 6. MASK REGISTER (SELECT MODE)

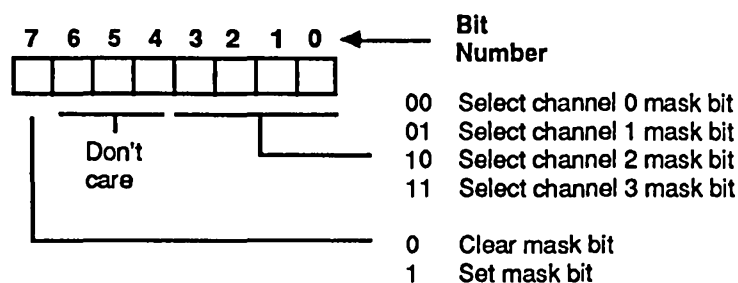


FIGURE 5. STATUS REGISTER

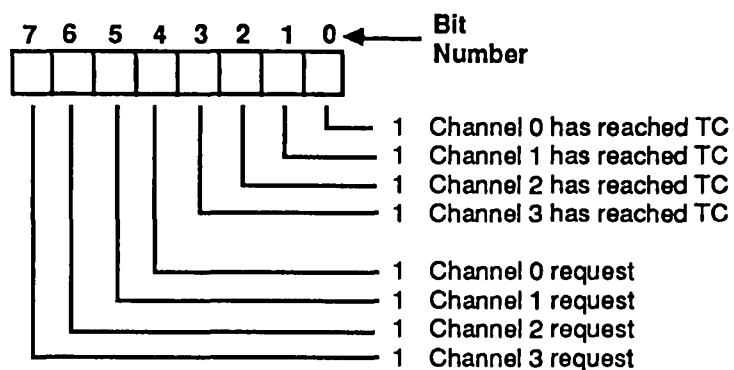


FIGURE 7. MASK REGISTER (MASK MODE)

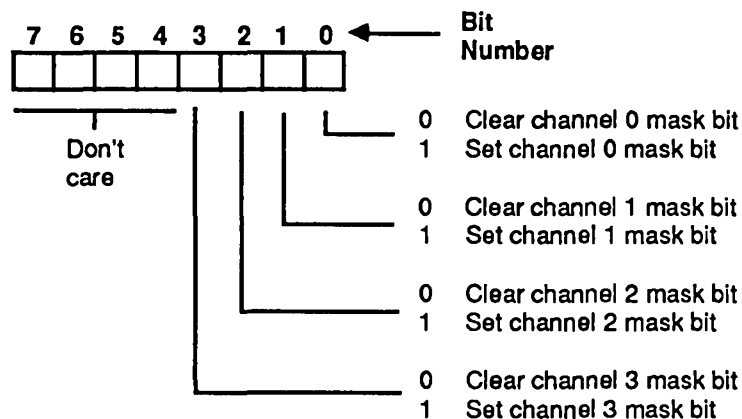


TABLE 2. REGISTER CODES

Register	Operation	Signals						
		-CS	-IOR	-IOW	A3	A2	A1	A0
Command	Write	0	1	0	1	0	0	0
Mode	Write	0	1	0	1	0	1	1
Request	Write	0	1	0	1	0	0	1
Mask	Set/Reset	0	1	0	1	0	1	0
Mask	Write	0	1	0	1	1	1	1
Temporary	Read	0	0	1	1	1	0	1
Status	Read	0	0	1	1	0	0	0

TABLE 3. SOFTWARE COMMAND CODES

Signals						Operation
A3	A2	A1	A0	-IOR	-IOW	
1	0	0	0	0	1	Read Status Register
1	0	0	0	1	0	Write Command Register
1	0	0	1	0	1	Illegal
1	0	0	1	1	0	Write Request Register
1	0	1	0	0	1	Illegal
1	0	1	0	1	0	Write Single Mask Register Bit
1	0	1	1	0	1	Illegal
1	0	1	1	1	0	Write Mode Register
1	1	0	0	0	1	Illegal
1	1	0	0	1	0	Clear Byte Pointer Flip/Flop
1	1	0	1	0	1	Read Temporary Register
1	1	0	1	1	0	Master Clear
1	1	1	0	0	1	Illegal
1	1	1	0	1	0	Clear Mask Register
1	1	1	1	0	1	Illegal
1	1	1	1	1	0	Write All Mask Register Bits

FIGURE 8. CASCADED VL82C37A CONTROLLERS

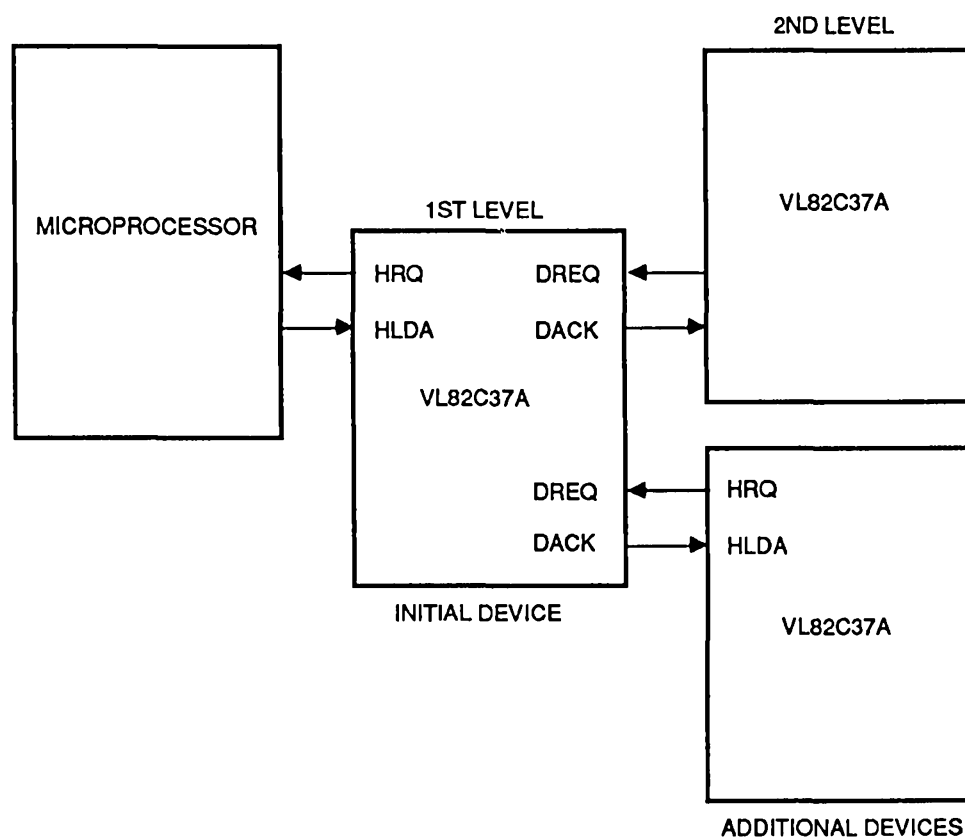


TABLE 4. WORD COUNT AND ADDRESS REGISTER COMMAND CODES

Channel	Register	Operation	Signals							Internal Flip-Flop	Data Bus DB0-DB7
			-CS	-IOR	-IOW	A3	A2	A1	A0		
0	Base and Current Address	Write	0	1	0	0	0	0	0	0	A0-A7
			0	1	0	0	0	0	0	1	A8-A15
	Current Address	Read	0	0	1	0	0	0	0	0	A0-A7
			0	0	1	0	0	0	0	1	A8-A15
	Base and Current Word Count	Write	0	1	0	0	0	0	1	0	W0-W7
			0	1	0	0	0	0	1	1	W8-W15
	Current Word Count	Read	0	0	1	0	0	0	1	0	W0-W7
			0	0	1	0	0	0	1	1	W8-W15
1	Base and Current Address	Write	0	1	0	0	0	1	0	0	A0-A7
			0	1	0	0	0	1	0	1	A8-A15
	Current Address	Read	0	0	1	0	0	1	0	0	A0-A7
			0	0	1	0	0	1	0	1	A8-A15
	Base and Current Word Count	Write	0	1	0	0	0	1	1	0	W0-W7
			0	1	0	0	0	1	1	1	W8-W15
	Current Word Count	Read	0	0	1	0	0	1	1	0	W0-W7
			0	0	1	0	0	1	1	1	W8-W15
2	Base and Current Address	Write	0	1	0	0	1	0	0	0	A0-A7
			0	1	0	0	1	0	0	1	A8-A15
	Current Address	Read	0	0	1	0	1	0	0	0	A0-A7
			0	0	1	0	1	0	0	1	A8-A15
	Base and Current Word Count	Write	0	1	0	0	1	0	1	0	W0-W7
			0	1	0	0	1	0	1	1	W8-W15
	Current Word Count	Read	0	0	1	0	1	0	1	0	W0-W7
			0	0	1	0	1	0	1	1	W8-W15
3	Base and Current Address	Write	0	1	0	0	1	1	0	0	A0-A7
			0	1	0	0	1	1	0	1	A8-A15
	Current Address	Read	0	0	1	0	1	1	0	0	A0-A7
			0	0	1	0	1	1	0	1	A8-A15
	Base and Current Word Count	Write	0	1	0	0	1	1	1	0	W0-W7
			0	1	0	0	1	1	1	1	W8-W15
	Current Word Count	Read	0	0	1	0	1	1	1	0	W0-W7
			0	0	1	0	1	1	1	1	W8-W15

TABLE 5. DMA MODE AC CHARACTERISTICS

Symbol	Parameter	VL82C37A-04		VL82C37A-05		VL82C37A-08		Unit
		Min	Max	Min	Max	Min	Max	
TAEL	AEN High from CLK Low (S1) Delay Time		225		200		105	ns
TAET	AEN Low from CLK High (S1) Delay Time		150		130		80	ns
TAFAB	ADR Active to Float Delay from CLK High		120		90		55	ns
TAFC	Read or Write Float from CLK High		120		120		75	ns
TAFDB	DB Active Float Delay from CLK High		190		170		135	ns
TAHR	ADR from Read High Hold Time	TCY-100		TCY-100		TCY-75		ns
TAHS	DB from ADSTB Low Hold Time	40		30		20		ns
TAHW	ADR from Write High Hold Time	TCY-50		TCY-50		TCY-50		ns
TAK	DACK Valid from CLK Low Delay Time (Note 7)		220		170		105	ns
	–EOP High from CLK High Delay Time (Note 10)		190		170		105	ns
	–EOP Low from CLK High Delay Time		190		170		105	ns
TASM	ADR Stable from CLK High		190		170		105	ns
TASS	DB to ADSTB Low Setup Time	100		100		65		ns
TCH	Clock High Time (Transitions ≤ 10 ns)	100		80		55		ns
TCL	Clock Low Time (Transitions ≤ 10 ns)	110		68		43		ns
TCY	CLK Cycle Time	250		200		125		ns
TDCL	CLK High to Read or Write Low Delay (Note 4)		200		190		120	ns
TDCTR	Read High from CLK High (S4) Delay Time (Note 4)		210		190		115	ns
TDCTW	Write High from CLK High (S4) Delay (Note 4)		150		130		80	ns
TDQ1	HRQ Valid from CLK High Delay Time (Note 5)		120		120		75	ns
TDQ2			190		120		75	ns
TEPS	–EOP Low from CLK Low Setup Time	45		40		25		ns
TEPW	–EOP Pulse Width	225		220		135		ns
TFAAB	ADR Float to Active Delay from CLK High		190		170		100	ns
TFAC	Read or Write Active from CLK High		150		150		90	ns
TFADB	DB Float to Active Delay from CLK High		225		200		110	ns
THS	HLDA Valid to CLK High Setup Time	75		75		45		ns
TIDH	Input Data from –MEMR High Hold Time	0		0		0		ns
TIDS	Input Data to –MEMR High Setup Time	190		170		90		ns
TODH	Output Data from –MEMW High Hold Time	20		10		10		ns
TODV	Output Data Valid to –MEMW High	125		125		90		ns
TQS	DREQ to CLK Low (S1,S4) Setup Time	0		0		0		ns
TRH	CLK to READY Low Hold Time	20		20		20		ns
TRS	READY to CLK Low Setup Time	60		60		35		ns
TSTL	ADSTB High from CLK High Delay Time		150		130		110	ns
TSTT	ADSTB Low from CLK High Delay Time		110		90		65	ns

Explanatory notes follow DC Characteristics Table.

FIGURE 10. MEMORY-TO-MEMORY TRANSFER TIMING (SEE TABLE 5)

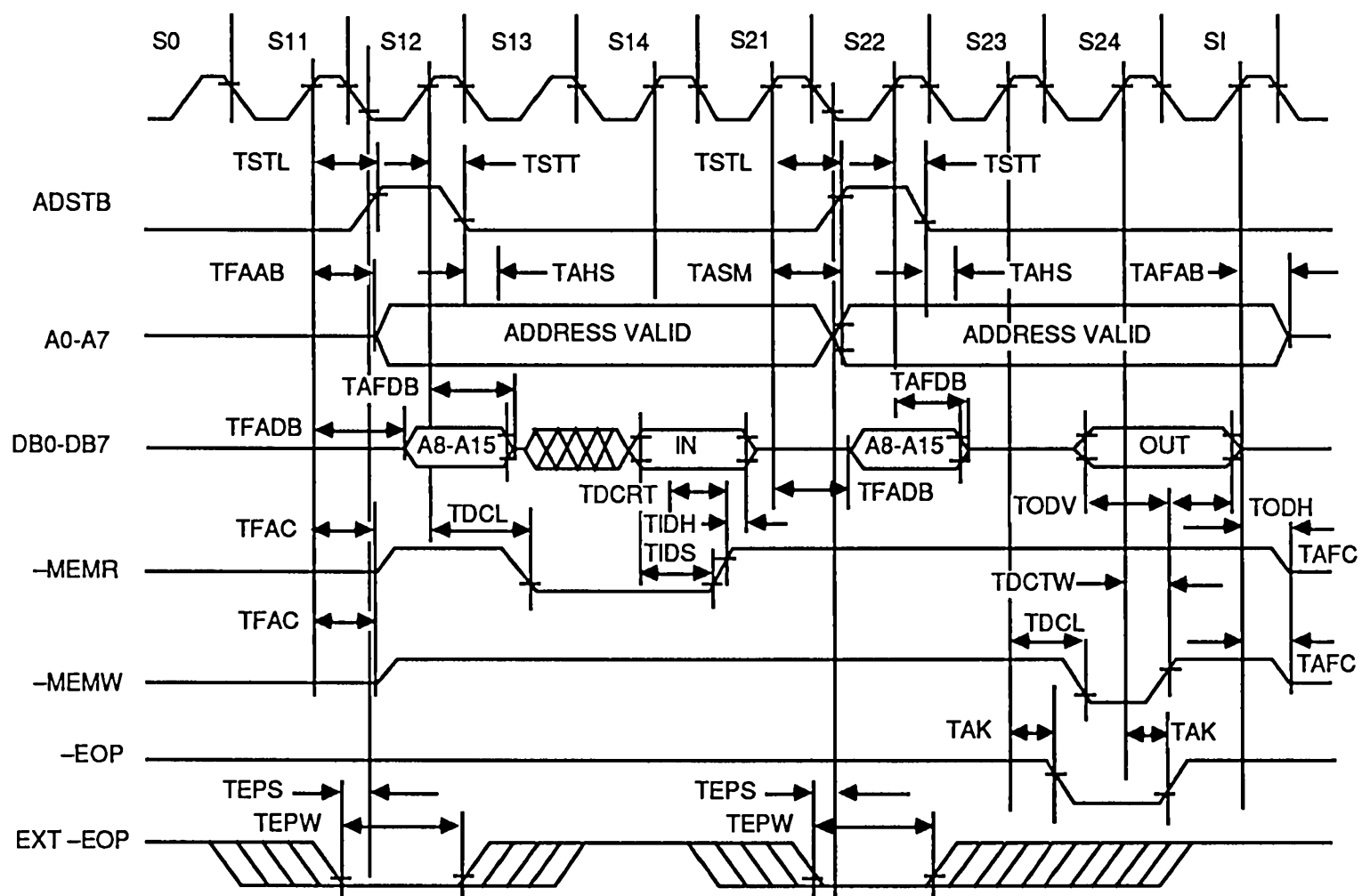


TABLE 6. PERIPHERAL MODE AC CHARACTERISTICS

Symbol	Parameter	VL82C37A-04		VL82C37A-05		VL82C37A-08		Unit
		Min	Max	Min	Max	Min	Max	
TAR	ADR Valid or $\overline{\text{CS}}$ Low to Read Low	50		50		30		ns
TAW	ADR Valid to Write High Setup Time	150		130		80		ns
TCW	CS Low to Write High Setup Time	150		130		80		ns
TDW	Data Valid to Write High Setup Time	150		130		80		ns
TRA	ADR or CS Hold from Read High	0		0		0		ns
TRDE	Data Access from Read Low (Note 3)		200		140		120	ns
TRDF	DB Float Delay from Read High	20	100	0	70	0	70	ns
TRSTD	Power Supply High to RESET Low Setup Time	500		500		500		ns
TRSTS	RESET to First $\overline{\text{IOW}}$	2TCY		2TCY		2TCY		ns
TRSTW	RESET Pulse Width	300		300		300		ns
TRW	Read Width	250		200		155		ns
TWA	ADR from Write High Hold Time	20		20		10		ns
TWC	CS High from Write High Hold Time	20		20		10		ns
TWD	Data from Write High Hold Time	30		30		20		ns
TWWS	Write Width	200		160		100		ns

Explanatory notes follow DC Characteristics Table.

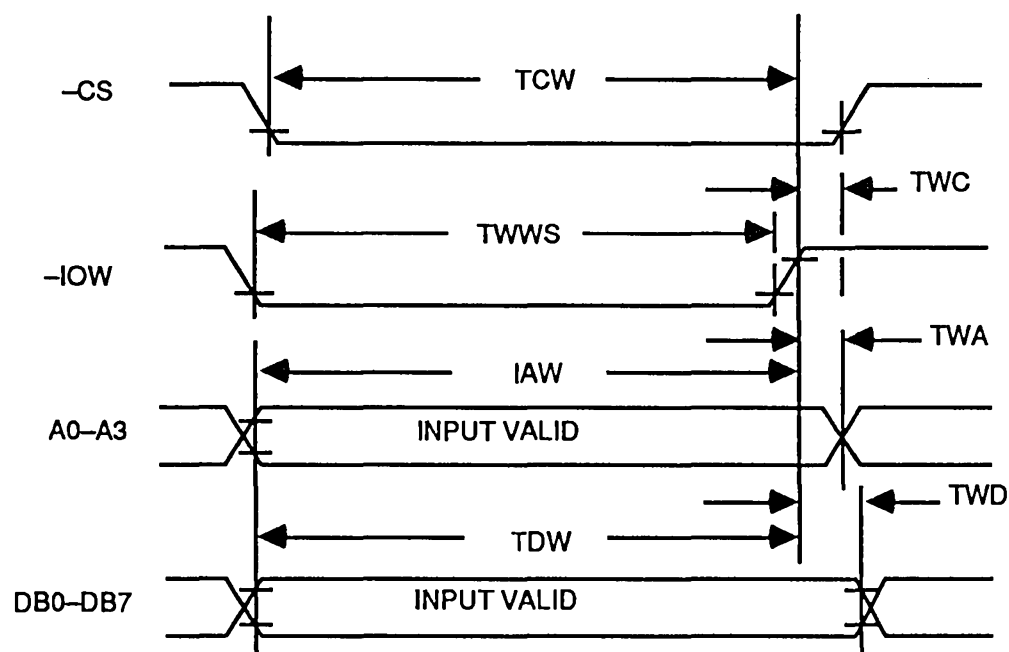
FIGURE 11. SLAVE MODE WRITE TIMING (SEE TABLE 6)


FIGURE 12. SLAVE MODE READ TIMING (SEE TABLE 6)

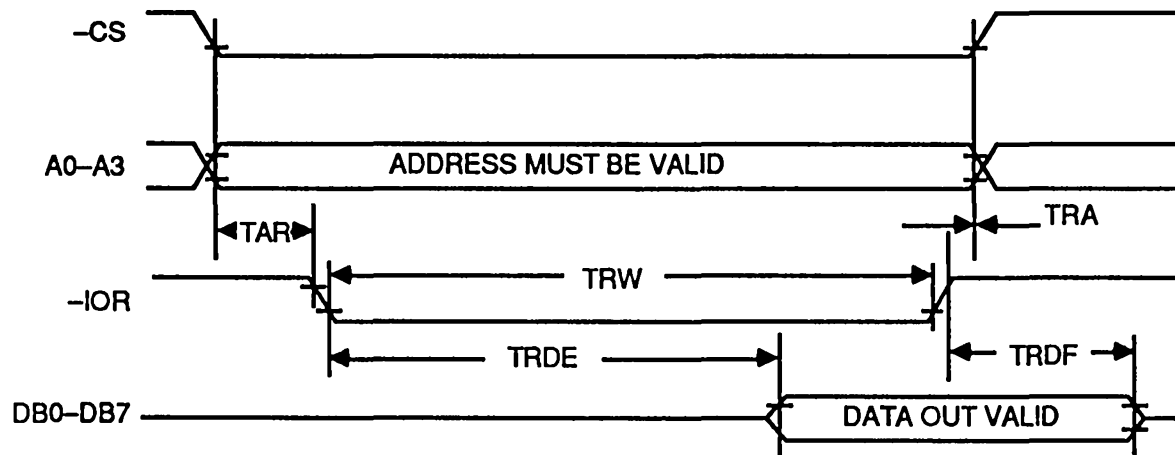


FIGURE 13. READY TIMING (SEE TABLE 5)

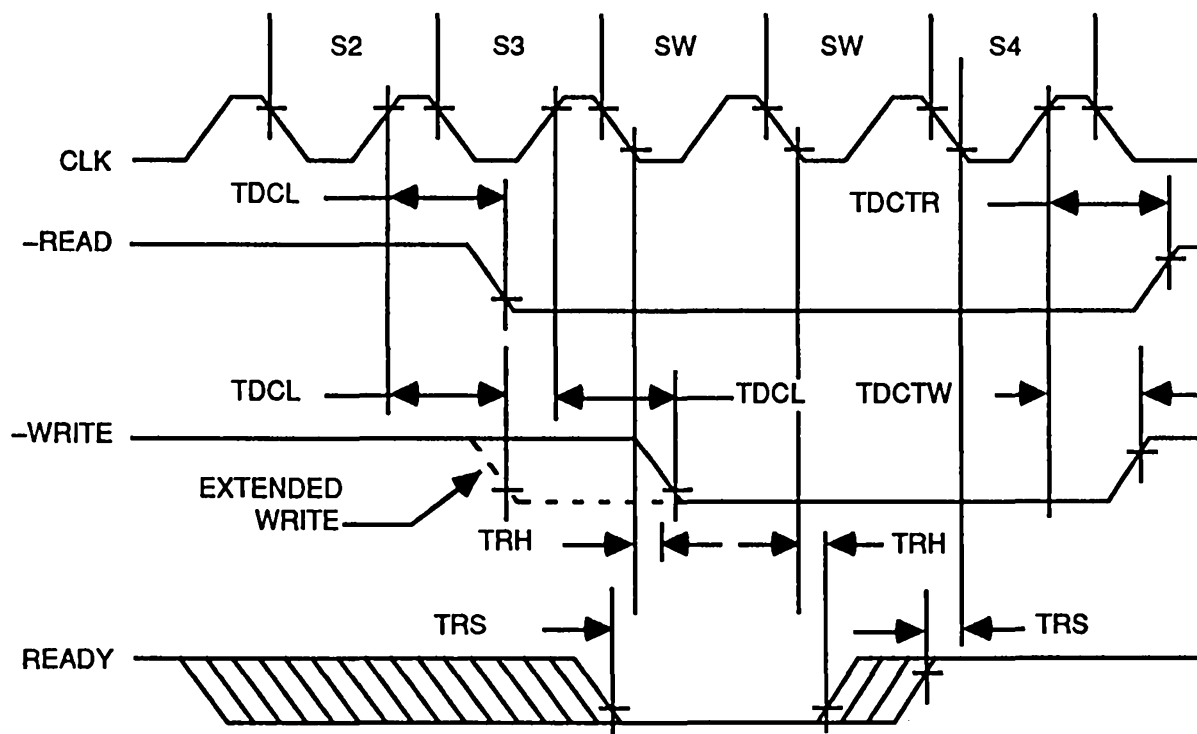


FIGURE 14. COMPRESSED TRANSFER TIMING (SEE TABLE 5)

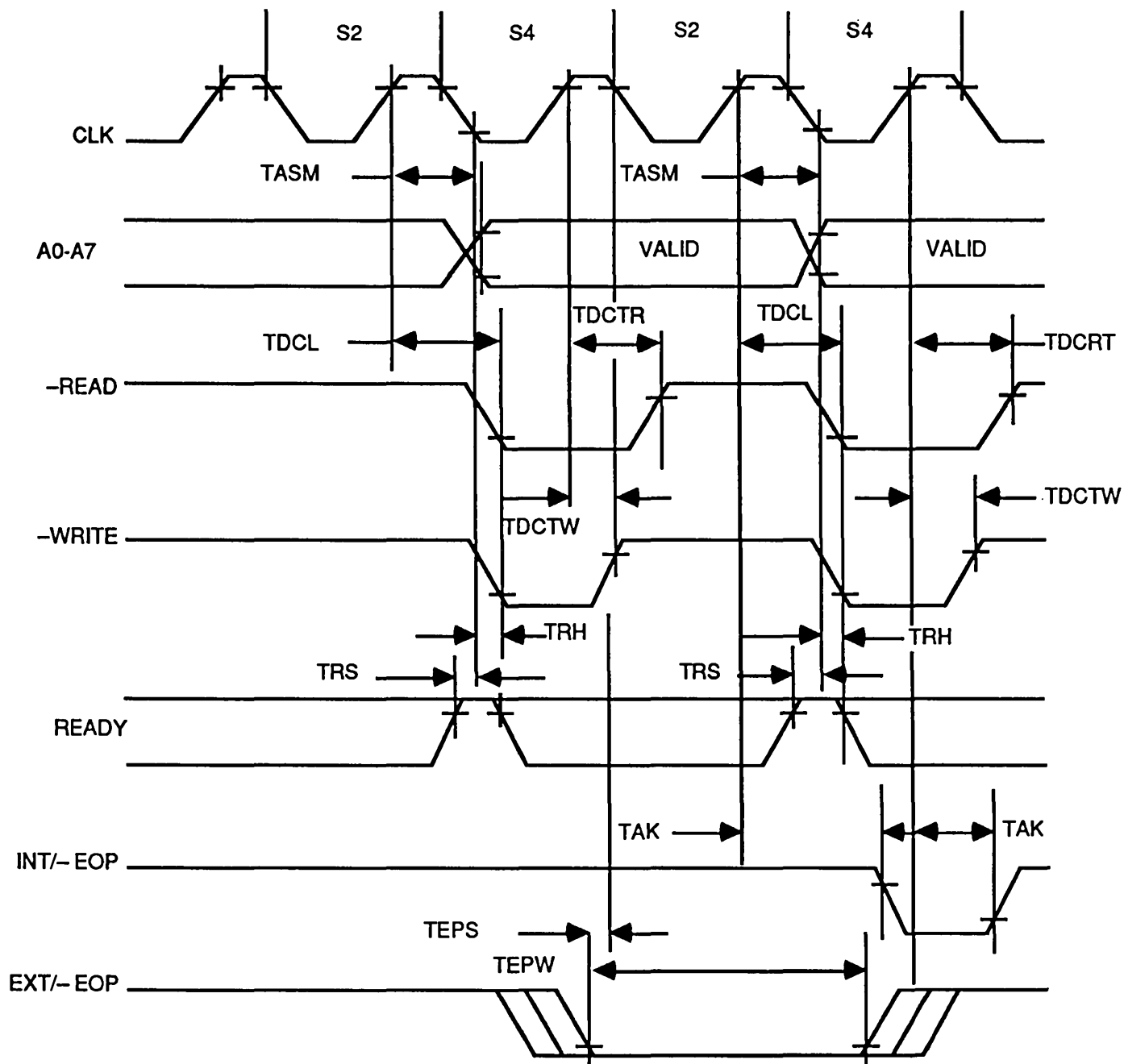
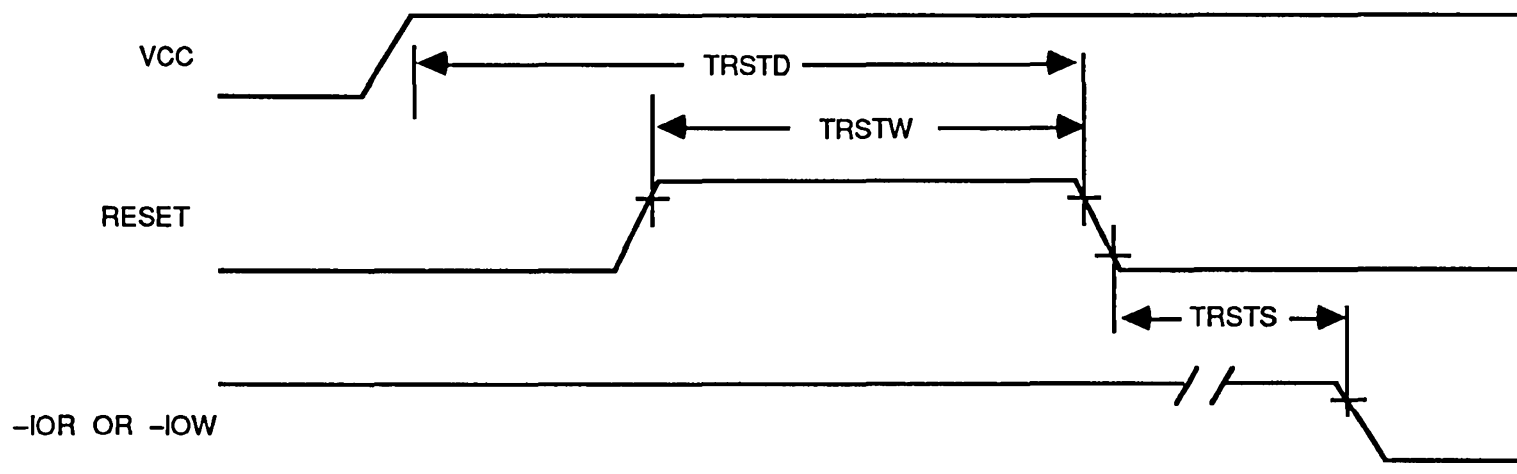


FIGURE 15. RESET TIMING (SEE TABLE 6)



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	−0.5 to 7.0 V	Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
Input Voltage	−0.5 to 5.5 V	
Output Voltage	−0.5 to 5.5 V	
Operating Temperature	0 °C to +150°C	
Storage Temperature	−65°C to +150°C	

DC CHARACTERISTICS:

Symbol	Parameter	Min	Typ (1)	Max	Unit	Test Conditions
VOH	Output High Voltage	2.4			V	IOH = −200 µA
		3.3			V	IOH = −100 µA (HRQ Only)
VOL	Output Low Voltage			450	mV	IOL = 2.0 mA (data bus) −EOP IOL = 3.2 mA (other outputs) (8) IOL = 2.5 mA (ADSTB) (8)
VIH	Input High Voltage	2.2		VCC + 0.5	V	
VIL	Input Low Voltage	−0.5		0.8	V	
ILI	Input Load Current			±10	µA	0 V ≤ VIN ≤ VCC
ILO	Output Leakage Current			±10	µA	0.45 V ≤ VOUT ≤ VCC
ICC	VCC Supply Current			30	mA	Clk. Freq. = 5 MHz, 8MHz
C0	Output Capacitance		4	8	pF	fC = 1.0 MHz, Inputs = 0 V
C1	Input Capacitance		8	15	pF	
C10	I/O Capacitance		10	18	pF	

AC and DC Characteristics Notes:

1. Typical values are for TA = 25°C, nominal supply voltage, and nominal processing parameters.
2. Input timing parameters assume transition times of 20 ns or less. Waveform measurement points for both input and output signals are 2.0 V for high and 0.8 V for low, unless otherwise noted.
3. Output loading is 1 TTL gate plus 150 pF capacitance, unless otherwise noted.
4. The net −IOW or −MEMW pulse width for normal write will be TCY-100 ns and for extended write will be 2TCY-100 ns. The net −IOR or −MEMR pulse width for normal read will be 2TCY-50 ns and for compressed read will be TCY-50 ns.
5. TDQ is specified for two different output high levels: TDQ1 is measured at 2.0 V, TDQ2 is measured at 3.3 V. The value for TDQ2 assumes an external 3.3 Kohm pull-up resistor connected from HRQ to VCC.
6. DREQ should be held active until DACK is returned.
7. DREQ and DACK signals may be active high or active low. Timing diagrams assume the active high mode.
8. Successive read and/or write operations, by the external processor, to program or examine the controller must be timed to allow at least 400 ns for the VL82C37A-05 and at least 250 ns for the VL82C37A-08, as recovery time between active read or write pulses.
9. −EOP is an open-collector output. This parameter assumes the presence of a 2.2 kΩ pull-up resistor to VCC.
10. Pin 5 is an input that should always be at a logic high level. An internal pull-up resistor will establish a logic high when the pin is left floating. It is recommended, however, that pin 5 be tied to VCC.

**MESSAGE-PASSING COPROCESSOR
MULTIBUS® II**
FEATURES

- Full-function, single-chip interface to Parallel System Bus (iPSB)
- Implements full message-passing protocol on iPSB bus
- Offloads managing iPSB bus arbitration, transfer and exception cycles from local CPU
- Maximizes performance on iPSB bus and local on-board bus
- Simplifies highly functional interconnect space implementations for both local and iPSB buses
- Processor-independent interface to iPSB bus
- Supports co-existence of dual-port and message-passing architectures

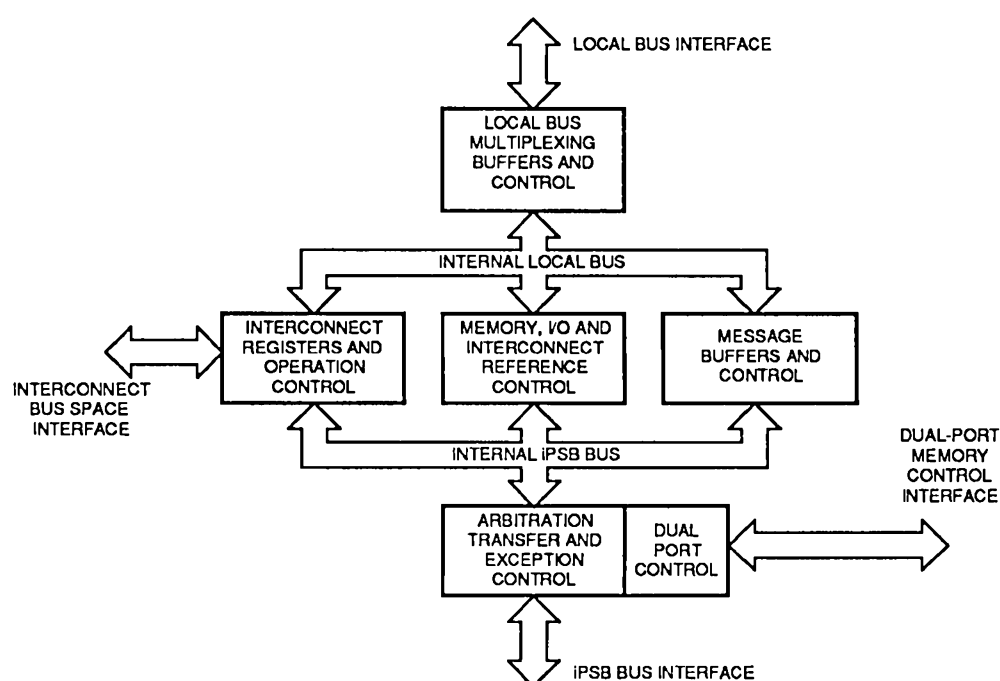
DESCRIPTION

The VL82C389 Message-Passing Coprocessor (MPC) provides a high-integration interface solution for the Parallel System Bus (iPSB) of the Multibus II architecture. The device integrates the logic necessary to implement a full bus interface solution, including support for message passing and interconnect spaces, as well as memory and I/O references on the iPSB bus. In addition, the MPC is designed to simplify implementation of dual-port memory functions for those designs that must co-exist with message passing.

The message address space in the Multibus II architecture has been defined to provide a high-performance interprocessor communication mechanism for multiprocessor systems. By performing the message space interface, the VL82C389 MPC offloads the interprocessor communication tasks from the local on-board CPU, which decouples the local bus activities from

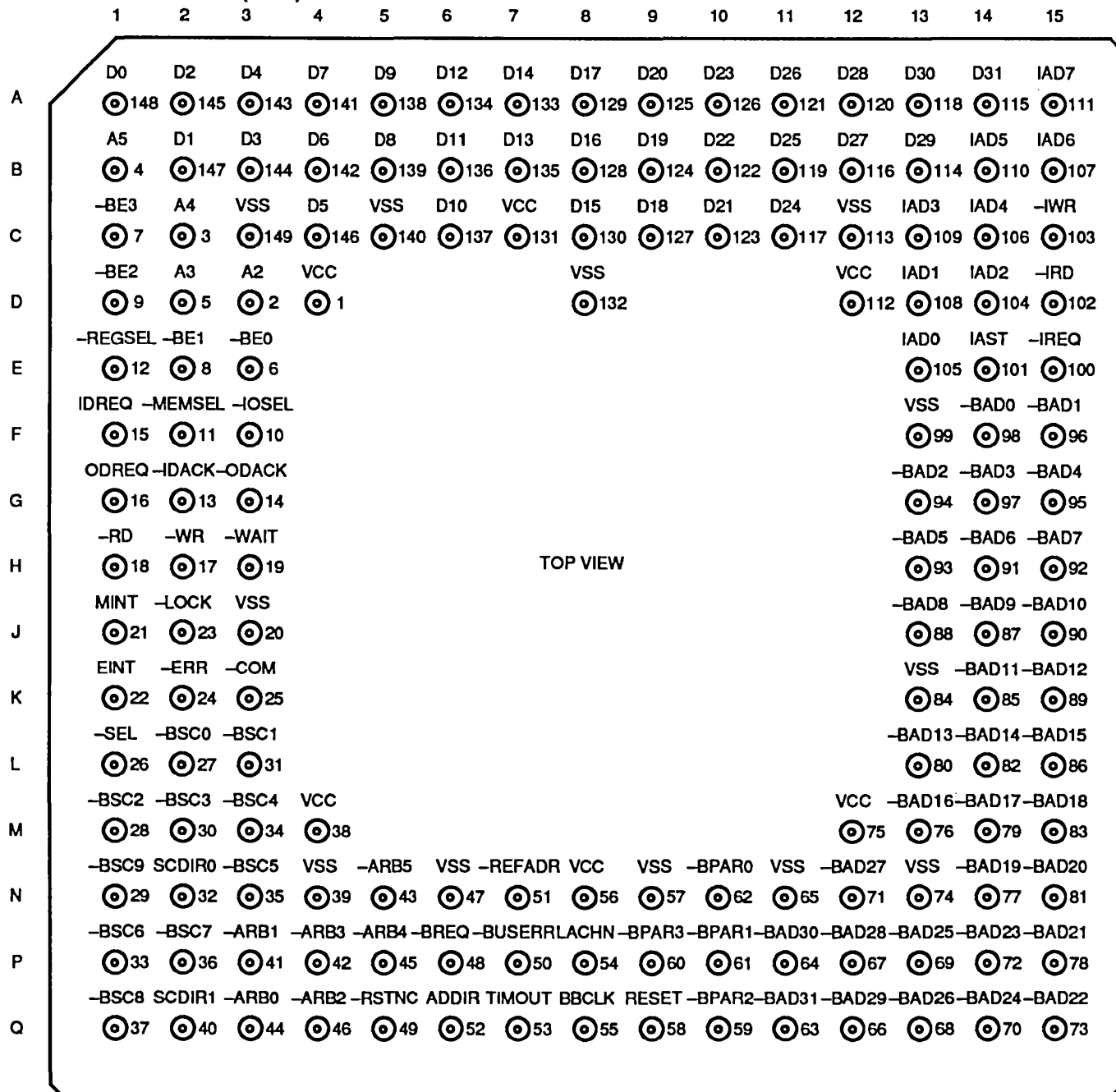
the iPSB bus activities. Decoupling these two functions eliminates an interface bottleneck present in traditional dual-port architectures. The bottleneck is a result of having a dual-port architecture that requires a tight coupling between a processor and some shared memory resource of limited size. Unfortunately, as the number of processors increases, the dual-port structure degrades system performance even more dramatically.

Using the MPC component to decouple these resources yields several enhancements to system performance. For example, resources on the local processor bus and Parallel System Bus are not held in wait states while arbitration for other resources is performed. In addition, each transfer can occur at the full bandwidth of the associated bus. The benefit of this is the increased overall system performance that results from processors being able to process other tasks in parallel, with message transfers being handled by the MPC component.

BLOCK DIAGRAM

ORDER INFORMATION

Part Number	Package
VL82C389-GC	Ceramic Pin Grid Array (PGA)

Note: Operating temperature range is 0°C to +70°C

PIN DIAGRAM
CERAMIC PIN GRID ARRAY (PGA)

FUNCTIONAL DESCRIPTION
Arbitration, Transfer, and Exception Cycle Protocol Support

The message-passing coprocessor implements the full arbitration, transfer, and exception cycle protocols required to interface to the iPSB bus. Arbitration is supported for both normal fairness mode and high priority mode.

The MPC performs the handshake protocols necessary to successfully complete iPSB transfer operations.

Transfer operations include access to memory, I/O, message and interconnect address spaces on the iPSB bus. During the transfer cycle, the device generates and checks parity on the system control (SC) lines and on the address/data (AD) lines. In addition, the MPC component recognizes agent errors and bus exceptions that are reported to the local CPU for recovery action.

INTERFACE DESCRIPTION

This section describes each interface noted in the block diagram on the front page. These interfaces include the local bus, the iPSB bus, the interconnect bus, and dual-port memory.

The Local Bus Interface

The local bus interface is used to provide a processor-independent path



from the on-board CPU to the iPSB bus. This interface supports direct references (memory, I/O, and interconnect address spaces) to the iPSB bus, references to local on-board interconnect space, and the full protocol for unsolicited and solicited message operations to and from the on-board CPU. Within the MPC component, local bus interface support consists of three logical interfaces: register, reference, and DMA. The register interface is used for message operations and access to interconnect address register on-board. These operations are completed fully asynchronous to the bus clock or interconnect bus operations. The reference interface is used to access resources asynchronous to the CPU (local interconnect space and memory, I/O, and interconnect address spaces on the iPSB bus). The DMA interface is used to transfer data for solicited message operations. This interface is designed to allow either two-cycle or single-cycle transfers. Single-cycle transfers allow direct transfer of data between the MPC and memory. To achieve higher performance via single-cycle transfers, the DMA interface is optimized for aligned data structures; however, operation on arbitrary byte strings is also supported.

iPSB Bus Interface

The iPSB bus interface implements a full 32-bit interface to the iPSB bus. This implementation includes arbitration, requestor control, replier control, and error handling functions. As a requestor, the MPC component supports references to memory, I/O, and interconnect spaces, as well as message packet transmission. As a replier, the MPC supports interconnect space and message packet reception. In addition, this interface provides significant management services for external dual port memory. These services include: address recognition, iPSB bus replier handshake, agent error checking, and bus parity generation and checking. Although this device handles the majority of errors, the dual-port memory controller is still responsible for generation and checking of memory data parity (not bus parity).

Interconnect Bus Support

Simply stated, the interconnect address space provides a physical rather than logical addressing mechanism for software initialization and configuration of system parameters (reduces jumper configuration) and system-level diagnostics. The interconnect bus provides a simple 8-bit path between the MPC and a user-defined design for the implementation of interconnect space. All references to interconnect space (either from the local bus or the iPSB bus) are routed through this path for service. In addition, this interconnect bus can be used for such non-reference-related activities as diagnostics. An example of a highly functional interconnect space implementation by the microcontroller implementation of Intel's iSBC 386/100. Further details of this implementation are available in the iSBC 386/100 Hardware Reference Manual (Intel order number: 146705-001).

Dual-Port Memory Support

Although the MULTIBUS II architecture has defined the message address space for optimized performance of inter-processor communication, more traditional designs can use dual-port memory implementations. The iPSB bus interface has been defined to allow co-existence of dual-port memory and message-passing architectures; however, it should be noted that the iPSB bus interface is optimized for message-passing architectures. The MPC is designed to support this co-existence. The device can be configured to recognize a range of addresses in memory space and act as an iPSB bus replier when appropriate. If an address match is detected, the MPC signals the external dual-port memory controller of the request. While the MPC provides an error detection and recovery mechanism for most agent errors and bus exceptions in a dual-port design, it is still the responsibility of the dual-port memory controller to generate and check memory data parity.

Single-Board Computer Configuration

The message passing coprocessor component provides a processor-independent iPSB bus interface solution for intelligent SBC boards. Examples include CPU boards, intelligent peripheral controllers, file servers, intelligent

data communications controllers, and graphics/image processors. This component is optimized for bus master or intelligent slave designs. Using the MPC reduces overall board real estate required for the iPSB bus interface. The MPC improves system reliability by performing the error checking and reporting protocols defined in the iPSB bus interface specification.

Message Support

The MPC provides full support for unsolicited and solicited messages. For solicited messages, the MPC supports a one-message-deep transmit FIFO and a four-message-deep receive FIFO. For solicited messages, the MPC supports one output channel and one input channel. Each channel has two packet buffers to allow pipelined operations on the local and iPSB buses. These features provide the required level of support necessary to implement the high-bandwidth message-passing facility defined in the Multibus II architecture.

Unsolicited Message Support

Unsolicited message support in the MPC is provided on the local bus via a register interface and on the iPSB bus with a packet transfer mechanism. An unsolicited message is initiated by the sending host CPU transferring a message to its local MPC. The transfer is performed as a series of register operations to the transmit FIFO. An unsolicited message may be from 4 to 32 bytes in length in four-byte increments.

Once the unsolicited message is transferred to the MPC, the sending host is free to discard the message in memory and process another task if it so chooses. In parallel, the MPC requests access to the iPSB bus for the pending transfer. Once the iPSB bus is obtained, the sending MPC transfers the message, as a single packet, to the receiving agent.

The receiving agent recognizes the incoming packet by its destination address field. If the MPC on the receiving agent detects a match between its message host ID and the destination address field, the packet is stored in a buffer and checks for error conditions. Any errors found are signaled to the sending MPC via the iPSB bus protocol.

Assuming the packet received is error-free, the receiving host CPU is informed of the message via an interrupt signal generated by the MPC. The host responds to this interrupt by performing a series of register operations to retrieve the message from the receive FIFO.

If an error occurs during the transfer of an unsolicited message over the iPSB bus, the sending MPC takes recovery action. If the error is a NACK, the MPC retries the message a predetermined number of times. All other errors are reported back to the sending host CPU for recovery actions. The host CPU is signaled via an interrupt and can retrieve the unsolicited message, with error status, through the error FIFO. Again, this operation is performed with a series of register operations.

Solicited Message Support

Solicited message transfers can be divided into three basic phases: negotiation, data transfer, and completion. The negotiation phase of the solicited transfer requires the exchange of two special unsolicited messages between the sending and receiving agents. The buffer request message is transferred from the sending agent to the receiving agent and the buffer grant is returned from the receiving agent to the sending agent. The MPC supports the transfer of these messages with the standard transfer protocol on the iPSB bus as previously described for the typical unsolicited message.

A solicited message transfer is initiated by the sending host CPU writing a buffer request message to the sending MPC transmit FIFO. The sending MPC recognizes the message as a buffer request and saves the following information. The destination and source addresses are saved for use in the data transfer phase. The request ID is saved for identification during completion or cancel operations. The transfer length is saved to determine the end of transfer and may contain any number of bytes.

The MPC pads the transfer to an even four-byte increment on the iPSB bus.

The sending MPC then assigns a sender liaison ID and transfers the buffer request message packet on the iPSB bus. The sender liaison ID is used to bind the buffer grant (or reject) to its corresponding buffer request when it is received back at the sending MPC. This allows the protocol to be extended to multiple concurrent transfers in the future.

The transfer phase is handled by the sending and receiving MPCs and their DMA controllers. Neither host CPU is involved in the transfer, and each may be processing other tasks during the transfer. At the sending agent, the transfer phase slightly overlaps the negotiation phase. As soon as the buffer request packet is sent error-free on the iPSB bus, the sending MPC prefetches up to two packets of data and prepares for transmission. Upon receiving the buffer grant and storing the necessary parameters, the data packet transfer is initiated. Data packets are then sent on the iPSB bus using full-bandwidth block transfers, at intervals defined by the duty cycle parameters, until the transfer is complete. The end of transfer is signaled to the receiving MPC by the last data packet. A solicited transfer may consist of from one to 32 packets. Packets are bound to 32 bytes plus header, with total transfers limited to 16M bytes.

At the receiving agent, the transfer phase begins after a buffer grant packet has been sent error-free on the iPSB bus. The receiving MPC then detects data packets, verifies the liaison ID, and stores the data. If the solicited input channel is not active (e.g., due to local cancel) or the liaison ID does not match, an agent error is signaled on the iPSB bus. Errors during the transfer phase are rare. Flow control using the duty cycle parameter prevents NACK problems, and the receiver has responded with a buffer grant guaranteeing its existence and ability to perform

the transfer. In the rare case that an error does occur, the MPC provides a retry algorithm for NACKs and reports exceptions or other agent errors immediately. The error is signaled to the host CPU by entering the completion phase. Errors generate an interrupt and provide error status.

The completion phase consists of a signal from the MPC to its corresponding host CPU. The signal consists of an interrupt followed by a series of register operations on the local bus. In all cases, the completion operation clears all states associated with the solicited operation in the MPC, allowing another operation to be initiated.

The MPC guarantees fail-safe operation for all aspects of the solicited message transfer, assuming the bus clock remains active (if the bus clock fails, all transfers cease, eliminating the need for recovery). This capability is provided by the error detection and reporting already discussed for bus-related problems and by two fail-safe counters that protect against fatal hardware or software errors on the sending or receiving agents. Recovery is provided to free a solicited message resource that would otherwise be tied up indefinitely, which eliminates the need for a fail-safe software timer.

It is important to note that the fail-safe counters are not intended for normal flow control. If a receiving host CPU accumulates a significant queue of buffer requests from its MPC, it should use unsolicited messages (and possibly rejects) to free channels in the system for other uses. The fail-safe counters are only intended to replace the need for a software timer to recover from otherwise fatal hardware and software errors.

For a more comprehensive explanation of the MPC function, please refer to the Intel document, Multibus II Message Passing Coprocessor External Product Specification (Engineering Document Number: 149300-001).

SIGNAL DESCRIPTIONS

The MPC signals can be classified into five interface groups: the iPSB bus, the dual-port RAM, the local bus, the interconnect bus and power/ground. This table describes the individual signals for each of these interfaces.

Signal Name	Pin Number	Signal Description																																																																
-BREQ	48	The bus request is a bidirectional, open-drain signal with high current drive. It connects directly to the iPSB bus. As an input, it indicates that there are agents awaiting access to the bus. In fair access mode, this inhibits the MPC from activating its own request. As an output, this signal is used to request bus access. Further details can be found in the iPSB bus specification.																																																																
-ARB0 - -ARB5	44, 41, 46, 42, 45, 43	The arbitration signals are bidirectional, open-drain signals with high current drive. They connect directly to the iPSB bus. These signals are used during normal operation to identify the mode and arbitration ID of an agent during arbitration cycles. During system initialization (while reset is active), these signals are used to initialize slot and arbitration IDs. Further details are available in the iPSB bus specification.																																																																
-BAD0- -BAD31	63, 64, 66-73, 77-83, 85-98	The address/data signals are bidirectional lines that connect to the iPSB bus -AD signals through 74F245 or equivalent transceivers. Further details are available in the iPSB bus specification.																																																																
<table><tr><td>-BAD31</td><td>-BAD30</td><td>-BAD29</td><td>-BAD28</td><td>-BAD27</td><td>-BAD26</td><td>-BAD25</td><td>-BAD24</td></tr><tr><td>63</td><td>64</td><td>66</td><td>67</td><td>71</td><td>68</td><td>69</td><td>70</td></tr><tr><td>-BAD23</td><td>-BAD22</td><td>-BAD21</td><td>-BAD20</td><td>-BAD19</td><td>-BAD18</td><td>-BAD17</td><td>-BAD16</td></tr><tr><td>72</td><td>73</td><td>78</td><td>81</td><td>77</td><td>83</td><td>79</td><td>76</td></tr><tr><td>-BAD15</td><td>-BAD14</td><td>-BAD13</td><td>-BAD12</td><td>-BAD11</td><td>-BAD10</td><td>-BAD9</td><td>-BAD8</td></tr><tr><td>86</td><td>82</td><td>80</td><td>89</td><td>85</td><td>90</td><td>87</td><td>88</td></tr><tr><td>-BAD7</td><td>-BAD6</td><td>-BAD5</td><td>-BAD4</td><td>-BAD3</td><td>-BAD2</td><td>-BAD1</td><td>-BAD0</td></tr><tr><td>92</td><td>91</td><td>93</td><td>95</td><td>97</td><td>94</td><td>96</td><td>98</td></tr></table>			-BAD31	-BAD30	-BAD29	-BAD28	-BAD27	-BAD26	-BAD25	-BAD24	63	64	66	67	71	68	69	70	-BAD23	-BAD22	-BAD21	-BAD20	-BAD19	-BAD18	-BAD17	-BAD16	72	73	78	81	77	83	79	76	-BAD15	-BAD14	-BAD13	-BAD12	-BAD11	-BAD10	-BAD9	-BAD8	86	82	80	89	85	90	87	88	-BAD7	-BAD6	-BAD5	-BAD4	-BAD3	-BAD2	-BAD1	-BAD0	92	91	93	95	97	94	96	98
-BAD31	-BAD30	-BAD29	-BAD28	-BAD27	-BAD26	-BAD25	-BAD24																																																											
63	64	66	67	71	68	69	70																																																											
-BAD23	-BAD22	-BAD21	-BAD20	-BAD19	-BAD18	-BAD17	-BAD16																																																											
72	73	78	81	77	83	79	76																																																											
-BAD15	-BAD14	-BAD13	-BAD12	-BAD11	-BAD10	-BAD9	-BAD8																																																											
86	82	80	89	85	90	87	88																																																											
-BAD7	-BAD6	-BAD5	-BAD4	-BAD3	-BAD2	-BAD1	-BAD0																																																											
92	91	93	95	97	94	96	98																																																											
-BPAR0, -BPAR1, -BPAR2, -BPAR3	62, 61, 59, 60	The byte parity signals are bidirectional lines that connect to the iPSB bus PAR signals through a 74F245 or equivalent transceiver. These signals are used to receive byte parity for incoming operations and to drive byte parity for outgoing operations. The MPC is responsible for parity generation and checking even if the address/data signals are driven from another source (e.g., dual-port memory data, address for reference). Further details are available in the iPSB bus specification.																																																																
ADDIR	52	The AD direction signal is an output used to control the direction of the 74F245 or equivalent transceivers for the -BAD0 through -BAD31 and -BPAR0 through -BPAR3 signals. Activating this signal drives data to the iPSB bus.																																																																
-REFADR	51	The reference address signal is an output from the MPC used to enable external address buffers for memory and I/O reference operations. Activating this signal drives the reference address onto the -BAD bus.																																																																
SCDIR0, SCDIR1	32, 40	The control/handshake direction signals are outputs used to control the direction of the 74F245 or equivalent transceivers for the -BSC signals. The SCDIR0 signal is used for -BSC0 - -BSC3 and -BSC9. The SCDIR1 signal is used for -BSC4 - -BSC8. Activating these signals drives data to the iPSB bus.																																																																
-BSC0- -BSC9	27-31, 33-37	The control/handshake signals are bidirectional lines that connect to iPSB bus -SC signals through 74F245 or equivalent transceivers. Details on the operation of these signals are available in the iPSB bus specification.																																																																
<table><tr><td colspan="6"></td><td>-BSC9</td><td>-BSC8</td></tr><tr><td colspan="6"></td><td>29</td><td>37</td></tr><tr><td>-BSC7</td><td>-BSC6</td><td>-BSC5</td><td>-BSC4</td><td>-BSC3</td><td>-BSC2</td><td>-BSC1</td><td>-BSC0</td></tr><tr><td>36</td><td>33</td><td>35</td><td>34</td><td>30</td><td>28</td><td>31</td><td>27</td></tr></table>									-BSC9	-BSC8							29	37	-BSC7	-BSC6	-BSC5	-BSC4	-BSC3	-BSC2	-BSC1	-BSC0	36	33	35	34	30	28	31	27																																
						-BSC9	-BSC8																																																											
						29	37																																																											
-BSC7	-BSC6	-BSC5	-BSC4	-BSC3	-BSC2	-BSC1	-BSC0																																																											
36	33	35	34	30	28	31	27																																																											

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Description
BBCLK	55	The bus clock input signal is a buffered version of the iPSB bus –BCLK signal. It is assumed that a 74AS1804A or equivalent buffer is used. This clock is used for all synchronous internal MPC timing.
TIMOUT	53	The time-out input signal is used to detect a time out condition signalled by the central services module (CSM). This signal is connected to the iPSB bus through a 74AS1804A or equivalent buffer.
LACHN	54	The latch signal is an input used during initialization of slot and arbitration IDs. When the RESET signal is active, this signal indicates when slot and arbitration IDs are available. This signal is connected to the iPSB bus through a 74AS1804A or equivalent buffer. Further details on initialization are available in the iPSB bus specification.
RESET	58	The RESET signal is an input used to put the MPC in a known state. Only the parts of the MPC involved with initialization of slot and arbitration IDs remain unaffected. This signal is buffered from the iPSB bus by a 74AS1804A or equivalent buffer connected to the –RST signal.
–BUSERR	50	The bus error signal is a bidirectional, open-drain line with high current drive. It connects directly to the iPSB bus. As an input, it is used to detect bus errors signalled by other agents. As an output it is used to signal parity errors detected on either the –AD or –SC signal lines, handshake protocol violations, or for extending exception recovery of a replier.
–RSTNC	49	The reset not complete signal is a bidirectional, open-drain line with high current drive. It connects directly to the iPSB bus. As an input, this signal inhibits the MPC from initiating iPSB bus operations. As an output, it is used to prevent iPSB bus operation until an agent is finished with on-board initialization. This signal is activated by the RESET signal going active. It is deactivated by the microcontroller after the RESET signal is deactivated and initialization is complete.
–SEL	26	The –SEL signal is activated by the MPC to indicate a dual-port access. This signal is used to initiate the dual-port operation and may be used to enable the dual-port data buffers onto the BAD* bus. When the MPC completes the iPSB bus handshake on the iPSB bus, or an exception is detected, this signal deactivates.
–COM	31	The –COM signal is activated by the dual-port memory controller to indicate that it is ready to complete the operation. This signal is assumed to be synchronous with the bus clock. The MPC activates replier ready on the iPSB bus on the next bus clock. This signal may not be deactivated until the EOT handshake is complete on the iPSB bus.
–ERR	24	The –ERR signal is activated by the dual-port memory controller to signal a memory data parity error. It must be stable at all times when the –COM signal is active. The MPC responds to this signal by completing the replier handshake on the iPSB bus using a "data error" agent error code. This signal may be asynchronous with the bus clock since it is qualified by the –COM signal.
D0 - D31	114-130, 133-139, 141-148	The data bus is a bidirectional group of signals used to transfer data between the host CPU and the MPC. Control is provided to allow operation of this bus with 8-, 16-, or 32-bit processors.

D31	D30	D29	D28	D27	D26	D25	D24
115	118	114	120	116	121	119	117
D23	D22	D21	D20	D19	D18	D17	D16
126	122	123	125	124	127	129	128
D15	D14	D13	D12	D11	D10	D9	D8
130	133	135	134	136	137	138	139
D7	D6	D5	D4	D3	D2	D1	D0
141	142	146	143	144	145	147	148

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Description
A2, A3, A4, A5	2, 5, 3, 4	The address inputs are used to identify MPC registers for message and interconnect space operations. Note that A0 and A1 are omitted to provide a consistent register address for all data-bus width options. These signals are qualified by commands (e.g., –RD or –WR) in the MPC and therefore may "glitch" outside the specified set-up and hold window.
–BE0, –BE1, –BE2, –BE3	6, 8, 9, 7	The byte enable input signals are used to identify the valid bytes and for data path control during memory and I/O reference operations. Only combinations supported by the iPSB bus specification are valid. These are summarized in the table below. Values not shown are illegal and may result in unpredictable results. These signals are qualified by commands (e.g., –RD or –WR) in the MPC and therefore may glitch outside the specified set-up and hold window.

Operation with 32-bit local buses requires all byte enable and data signals to be used. For 16-bit local buses, the –BE3 and –BE2 signals are held inactive and only D15-D0 are used. For all cases a read operation enables all 32 data signals, even if all byte enables are inactive. For 8-bit local bus operations –BE3 is held active, –BE2 is held inactive, –BE1 is connected to –A0, and –BE0 is connected to A0. This mode uses only D7-D0.

–BE3	–BE2	–BE1	–BE0	LOCAL BUS				IPSB BUS			
				D31 - D24	D23 - D16	D15 - D8	D7 - D0	AD31-AD24	AD23-AD16	AD15-AD8	AD7-AD0
L	L	L	L	V3	V2	V1	V0	V3	V2	V1	V0
L	L	L	H	V3	V2	V1	X	V3	V2	V1	X
H	L	L	L	X	V2	V1	V0	X	V2	V1	V0
L	L	H	H	V3	V2	X	X	X	X	V3	V2
H	L	L	H	X	V2	V1	X	X	V2	V1	X
H	H	L	L	X	X	V1	V0	X	X	V1	V0
L	H	H	H	V3	X	X	X	X	X	V3	X
H	L	H	H	X	V2	X	X	X	X	X	V2
H	H	L	H	X	X	V1	X	X	X	V1	X
H	H	H	L	X	X	X	V0	X	X	X	V0
L	H	L	H	X	X	X	V0	X	X	V0	X
L	H	L	H	X	X	X	V0	X	X	X	V0

L - Electrical low state (active)

H - Electrical high state (inactive)

Vx - Valid data bus

For reference only

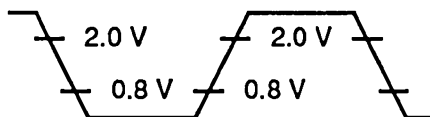
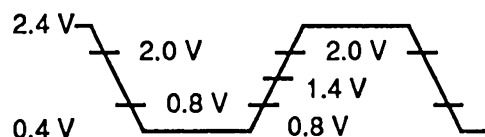
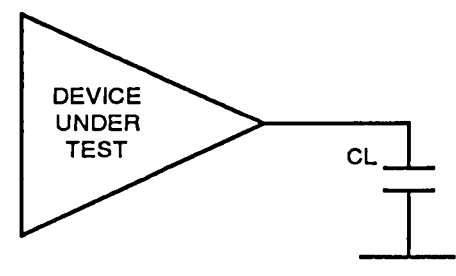
–MEMSEL	11	The memory select input signal is used to identify a memory reference operation to the iPSB bus. It is qualified by commands (e.g., –RD or –WR) in the MPC and therefore may glitch outside the specified set-up and hold window.
–IOSEL	10	The I/O select input signal is used to identify an I/O reference operation to iPSB bus. It is qualified by commands (e.g., –RD or –WR) in the MPC and therefore may "glitch" outside the specified set-up and hold window.
–REGSEL	12	The register select input signal is used to identify operations to internal MPC registers used to perform message and interconnect space operations. This signal is qualified by commands (e.g., –RD or –WR) in the MPC and therefore may glitch outside the specified set-up and hold window.
–LOCK	23	The –LOCK signal is an input to the MPC that allows back-to-back operations to be performed on the iPSB bus or to local interconnect space. When –LOCK is asserted, any resource accessed by the operation (iPSB bus or local interconnect space) is locked until the –LOCK signal is deasserted.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Description																
–RD	18	The read input signal is activated to initiate a read operation. This signal must provide clean transitions.																
–WR	17	The write input signal is activated to initiate a write operation. This signal must provide clean transitions.																
–WAIT	19	The –WAIT signal is driven by the MPC to hold up a transfer operation. This signal is used by the MPC for all accesses that require synchronization to another resource. When used, it is activated by a command going active and deactivated when the accessed resource is ready to complete the requested operation.																
MINT	21	The message interrupt output signal is used for all message-related signalling to the host CPU. This includes arrival of an unsolicited message, completion of a solicited transfer, and an error on message transfer.																
EINT	22	The error interrupt output signal is used to signal all errors related to memory, I/O or interconnect space operations. Internal registers in the MPC provide exact details of the error via interconnect space. (Even though this is a local bus signal, it will be discussed with the interconnect bus signals for simplicity in future sections.)																
ODREQ	16	The output channel DMA request signal is generated by the MPC to enable DMA transfer of data to the MPC (e.g., output to the iPSB bus).																
IDREQ	15	The input channel DMA request signal is generated by the MPC to enable DMA transfer of data from the MPC (e.g., input from the iPSB bus).																
–ODACK	14	The output channel DMA acknowledge input signal is activated to perform a DMA data transfer to the MPC. It is qualified by commands (e.g., –RD or –WR) in the MPC and therefore may glitch outside the specified set up and hold window.																
–IDACK	13	The input channel DMA acknowledge input signal is activated to perform a DMA data transfer from the MPC. It is qualified by commands (e.g., –RD or –WR) in the MPC and therefore may glitch outside the specified set-up and hold window.																
IAD0-IAD7	104-111	The interconnect address/data bus is a multiplexed bus designed to directly interface to a microcontroller. In addition to the MPC, other interconnect registers can be connected to this bus.																
<table><tr><td>IAD7</td><td>IAD6</td><td>IAD5</td><td>IAD4</td><td>IAD3</td><td>IAD2</td><td>IAD1</td><td>IAD0</td></tr><tr><td>111</td><td>107</td><td>110</td><td>106</td><td>109</td><td>104</td><td>108</td><td>105</td></tr></table>			IAD7	IAD6	IAD5	IAD4	IAD3	IAD2	IAD1	IAD0	111	107	110	106	109	104	108	105
IAD7	IAD6	IAD5	IAD4	IAD3	IAD2	IAD1	IAD0											
111	107	110	106	109	104	108	105											
–IREQ	100	The interconnect request signal is generated by the MPC when an interconnect operation has been requested either from the local bus or from the iPSB bus. This signal remains active until the microcontroller performs arbitration.																
IAST	101	The interconnect address strobe signal is an input to the MPC used to indicate that a valid address is on the interconnect bus. This signal may be directly connected to the ALE output of most microcontrollers. This signal must provide clean transitions.																
–IRD	102	The interconnect bus read signal is an input to the MPC. This signal is used to perform a read operation to one of the MPC interconnect interface registers. This signal must provide clean transitions. When this signal is activated in conjunction with the –IWR signal, all MPC outputs are disabled.																
–IWR	103	The interconnect bus write signal is an input to the MPC. This signal is used to perform a write operation to one of the MPC interconnect interface registers. This signal must provide clean transitions. When this signal is activated in conjunction with the –IRD signal, all MPC outputs are disabled.																

TIMING CHARACTERISTICS $T_A = 0^{\circ}\text{C to } +70^{\circ}\text{C}$, $V_{CC} = 5\text{ V} \pm 5\%$
LOCAL BUS

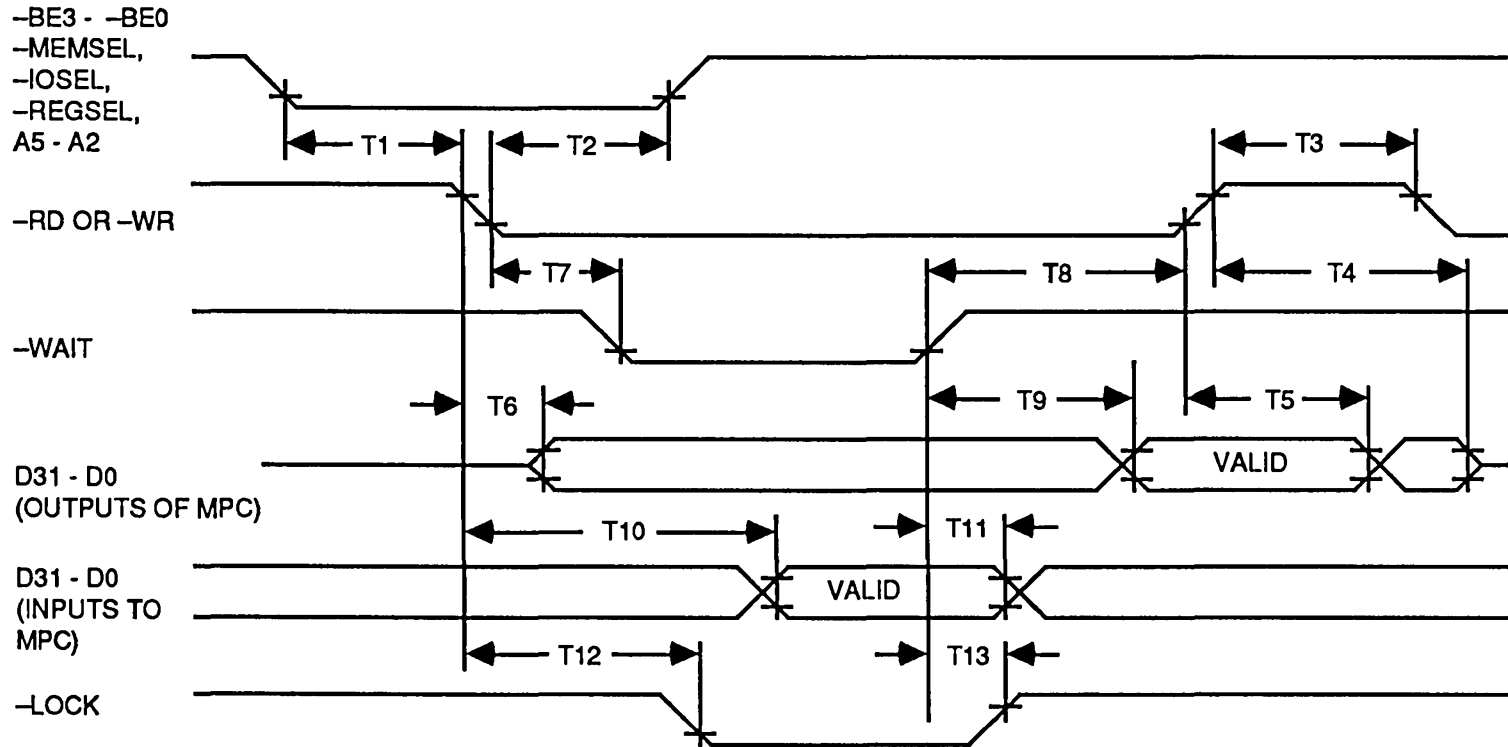
Symbol	Parameter	Min	Max	Units	Test Conditions
T1	Address and --BE Set-Up To Command Active	30		ns	
	Select and DACK Set-Up To Command Active	24		ns	
T2	Address, --BEn , --Select , and --DACK Hold From Command Active	10		ns	
T3	Command Inactive	35		ns	
T4	Command Inactive To Read Data Disable (Note 1)		24	ns	
T5	Read Data Hold From Command Inactive	3		ns	
T6	Read Data Enable From Command Active	0		ns	
T7	--WAIT Active From Command Active		35	ns	$CL = 50\text{ pF}$
T8	Command Inactive From --WAIT Inactive	0		ns	
T9	--WAIT Inactive To Read Data Valid		50	ns	$CL = 150\text{ pF}$
T10	Command Active To Write Data Valid		200	ns	
T11	Write Data Hold From --WAIT Inactive	0		ns	
T12	Command Active To --LOCK Active (Note 2)		100	ns	
T13	LOCK^* Hold From --WAIT Inactive (Note 3)	0		ns	
T14	Command Active	70		ns	
T15	Read Data Valid From Command Active		60	ns	$CL = 150\text{ pF}$
T16	Write Data Set-Up To Command Inactive	Registers	35	ns	
		DMA	25	ns	
T17	Write Data Hold From Command Inactive	5		ns	
T18	Command Active To MINT Or --DREQ Inactive (Notes 4, 5)		70	ns	$CL = 50\text{ pF}$
T19	Command Active To --DREQ Inactive (Note 5)		45	ns	$CL = 50\text{ pF}$

FIGURE 1. OUTPUT WAVEFORM TEST POINTS

FIGURE 2. INPUT WAVEFORM TEST POINTS (Note 6)

FIGURE 3. AC TEST LOAD CIRCUIT

Notes:

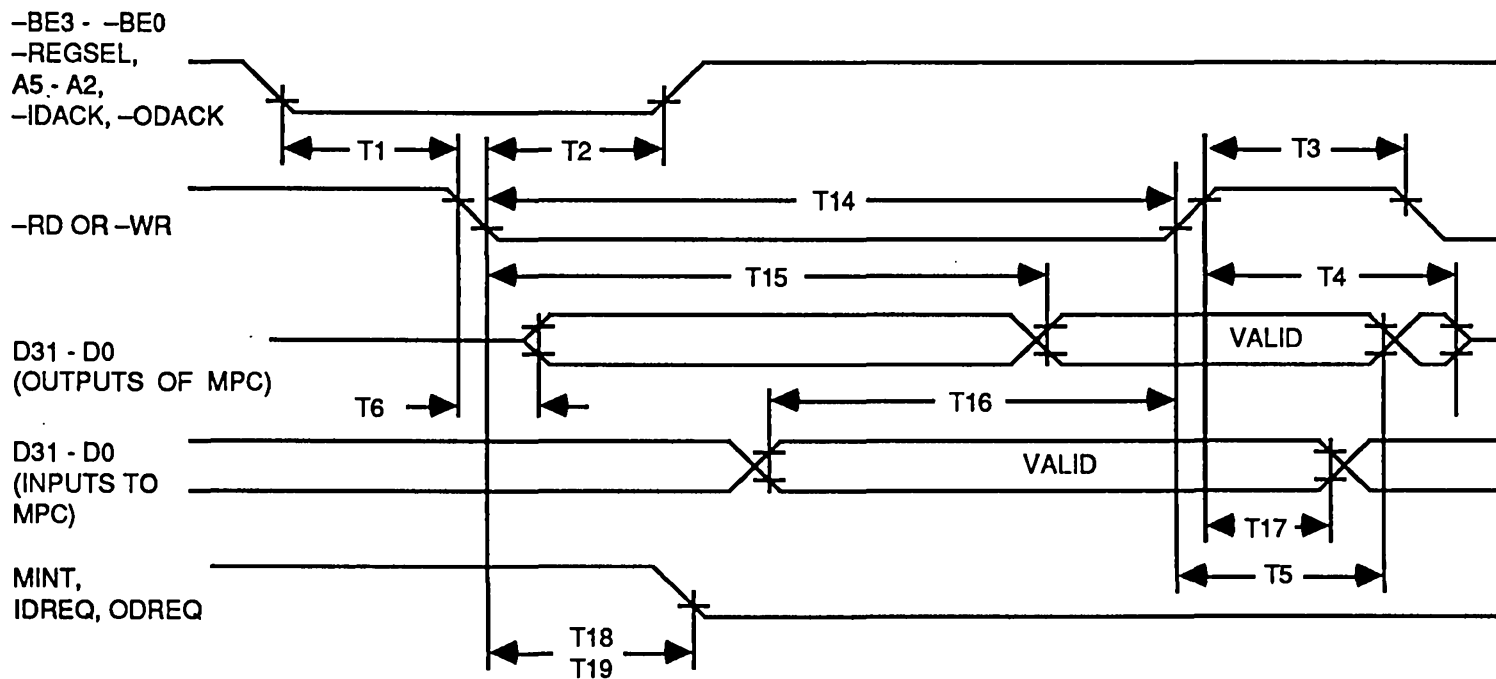
1. Disable condition occurs when the output current becomes less than the input leakage specification.
2. Required to guarantee locking of resource.
3. Required to guarantee resource remains locked.
4. MINT deassertion only if no other sources are pending.
5. For --DREQ inactive timing, T19 applies to a normal last transfer de-assert condition and T18 to an error de-assert condition.
6. 1.4 V level for BBCLK only.

TIMING DIAGRAMS

LOCAL BUS REFERENCE

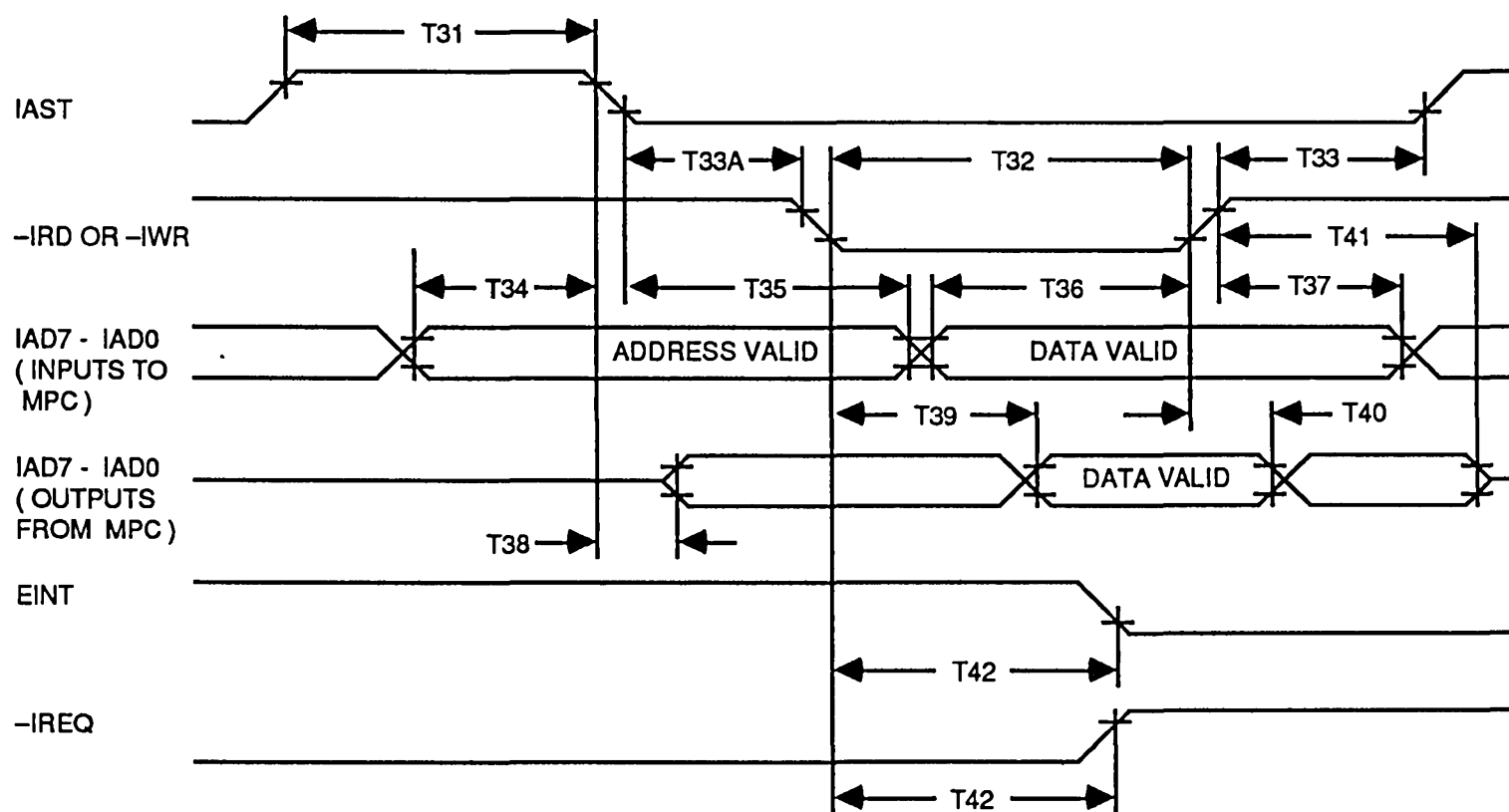


LOCAL BUS REGISTER AND DMA OPERATIONS



AC CHARACTERISTICS $T_A = 0^\circ\text{C to } +70^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 5\%$
INTERCONNECT BUS

Symbol	Parameter	Min	Max	Units	Test Conditions
T31	IAST Active	85		ns	
T32	Command Active	250		ns	
T33	Command Inactive To IAST Active	25		ns	
T33A	IAST Inactive To Command Active	120		ns	
T34	Address Set-Up To IAST Inactive	40		ns	
T35	Address Hold From IAST Inactive	20		ns	
T36	Write Data Set-Up To Command Inactive	120		ns	
T37	Write Data Hold From Command Inactive	5		ns	
T38	Read Data Enable From Command Active	0		ns	
T39	Read Data Valid From Command Active		120	ns	$CL = 150\text{ pF}$
T40	Read Data Hold From Command Inactive	0		ns	
T41	Read Data Disable From Command Inactive (Note 1)		30	ns	
T42	EINT, -IREQ Inactive From Command Active (Note 2)		100	ns	$CL = 50\text{ pF}$

TIMING DIAGRAM

Notes:

1. Disable condition occurs when the output current becomes less than the input leakage specification.
2. EINT inactive only on write to error register. -IREQ inactive only on write to arbitration register.

TIMING CHARACTERISTICS $T_A = 0^\circ\text{C to } +70^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 5\%$
IPSB BUS

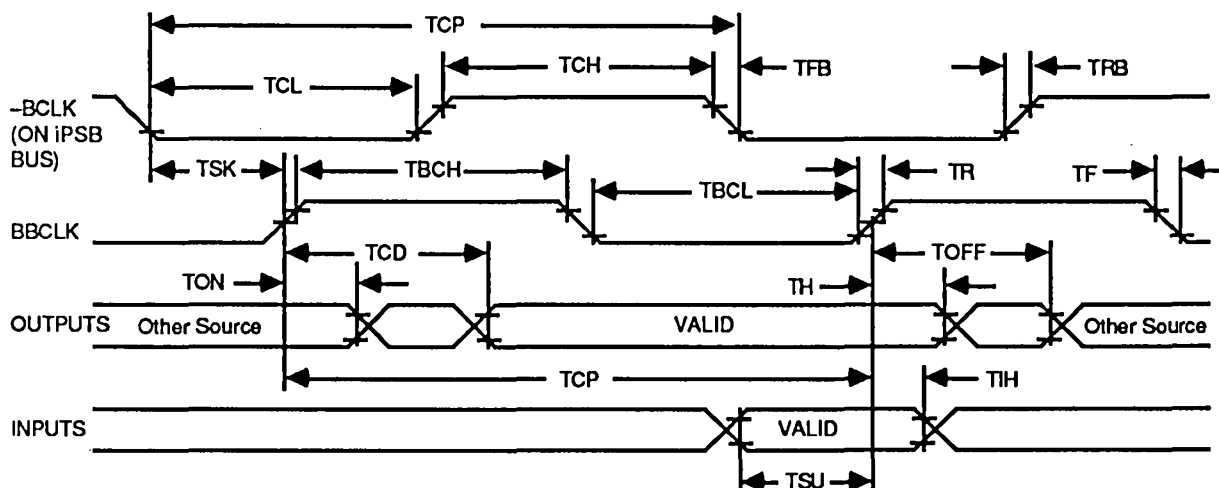
Symbol	Parameter		Min	Max	Units	Test Conditions
TCP	Clock Period		99.9		ns	
TCL	-BCLK Low Time		40		ns	
TCH	-BCLK High Time		40		ns	
TBCL	BBCLK Low Time		38		ns	
TBCH	BBCLK High Time		38		ns	
TRB	-BCLK Rise Time		1.0	5.0	ns	
TFB	-BCLK Fall Time		1.0	2.0	ns	
TR	BBCLK Rise Time		0.5	1.0	ns	
TF	BBCLK Fall Time		0.5	1.0	ns	
TSK	-BCLK To BBCLK Skew (Note 1)		-0.5	4.0	ns	
TCD	Clock To Output Delay	-BREQ, -BUSERR, -RSTNC (Note 2)		36	ns	CL = 500 pF
		-ARB5 - -ARB0 (Note 2,3)		36	ns	CL = 500 pF
		-BSC7 - -BSC0, -BAD31 - -BAD0		29	ns	CL = 75 pF
		-BPAR3 - -BPAR0, -BSC9, -BSC8		29	ns	CL = 50 pF
		SCDIR0, SCDIR1	High To Low	19	ns	CL = 25 pF
			Low To High	21	ns	CL = 25 pF
		ADDR	High To Low	27	ns	CL = 50 pF
			Low To High	21	ns	CL = 50 pF
		-REFADR		29	ns	CL = 75 pF
TH	Hold Time From Clock	-SEL		29	ns	CL = 50 pF
		-BREQ, -BUSERR, -RSTNC	6.5		ns	
		-ARB5 - -ARB0 (Note 3)	6.5		ns	
		-BAD31 - -BAD0, -BPAR3 - -BPAR0	5.0		ns	
		-BSC9 - -BSC0	4.0		ns	
		SCDIR0, SCDIR1	4.0		ns	
		ADDR	5.0		ns	
		-REFADR	4.0		ns	
		-SEL	4.0		ns	

Notes:

1. These clock timings refer the MPC specification to the iPSB bus specifications. They assume a 74AS1804 type buffer is used.
2. The 500 pF load is a distributed value as defined in the iPSB bus specification. The open-drain signals are designed such that the output delay and bus loss meets the iPSB specification requirement. An appropriate test condition that correlates to the distributed load will be determined during characterization.
3. The -ARB5 - -ARB0 signal timings are with respect to the first and last clock of the arbitration period. Details are in the iPSB bus specification. Also, the arbitration logic has been designed to meet the loop delay specification accounting for the full path of input to output plus bus loss. An appropriate test condition will be determined during device characterization.

TIMING CHARACTERISTICS $T_A = 0^\circ\text{C to } +70^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 5\%$
IPSB BUS (Cont.)

Symbol	Parameter	Min	Max	Units	Test Conditions
TON	Turn On Delay From Clock (Note 4)	-BREQ, -BUSERR, -RSTNC	6.5	ns	
		-ARB5 - -ARB0 (Note1)	6.5	ns	
		-BAD31 - -BAD0, -BPAR3 - -BPAR0	5.0	ns	
		-BSC9 - -BSC0	4.0	ns	
TOFF	Turn Off Delay From Clock (Note 5)	-BREQ, -BUSERR, -RSTNC		36	ns
		-ARB5 - -ARB0 (Note 3)		36	ns
		-BAD31 - -BAD0, -BPAR3 - -BPAR0		29	ns
		-BSC9 - -BSC0		29	ns
TSU	Input Set-Up To Clock	-BREQ, -BUSERR, -RSTNC	22	ns	
		-ARB5 - -ARB0 (Note 3)	40	ns	
		-BAD31 - -BAD0, -BPAR3 - -BPAR0	24	ns	
		-BSC9 - -BSC0	24	ns	
		TIMOUT, LACHN, RESET	24	ns	
		-COM, -ERR	40	ns	
TIH	Input Hold From Clock	-BREQ, -BUSERR, -RSTNC	0	ns	
		-ARB5 - -ARB0 (Note 3)	0	ns	
		-BAD31 - -BAD0, -BPAR3 - -BPAR0	3	ns	
		-BSC9 - -BSC0	2	ns	
		TIMOUT, LACHN, RESET	2	ns	
		-COM, -ERR	3	ns	

TIMING DIAGRAM
IPSB BUS

Notes:

- Minimum turn-on times are measured the same way as hold times. Specifically, the logic level driven by another device on the previous clock cycle must not be disturbed.
- Maximum turn-off times are measured to the condition where the output leakage current becomes less than the input leakage specification.

ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	−10°C to +80°C
Storage Temperature	−65°C to +150°C
Supply Voltage to Ground Potential	−0.5 V to +7.0 V
Applied Output Voltage	−0.3 V to VCC +0.5 V
Applied Input Voltage	−0.5 V to VCC +0.5 V

Stresses above those listed may cause permanent damage to the device. These are stress ratings only, and operation of this device at these or other conditions above those indicated in this data

sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS TA = 0 C to + 70 C, VCC = 5 V 5%

Symbol	Parameter		Min	Max	Units	Test Conditions
VIL	Input Low Voltage		− 0.5	0.8	V	
VIH	Input High Voltage		2.0	VCC + 0.5	V	
VOL	Output Low Voltage	Open Drain		0.55	V	IOL Max
		All Others		0.45	V	IOL Max
VOH	Output High Voltage		2.4		V	IOH Max
ILI	Input Leakage Current	Open Drain		± 400	μA	0 ≤ VIN ≤ VCC
		BBCLK		± 100	μA	0 ≤ VIN ≤ VCC
		All Others		± 10	μA	0 ≤ VIN ≤ VCC
IOL	Output Low Current	Open Drain	60.0		mA	VOL = 0.55 V
		ADDR and −REFADR	8.0		mA	VOL = 0.45 V
		All Others	4.0		mA	VOL = 0.45 V
IOH	Output High Current		−1.0			VOH = 2.4 V
ICC	Operating Supply Current			400	mA	

CAPACITANCE TA = 25 C, fC = 1 MHz (Note 1)

Symbol	Parameter		Min.	Max.	Units	Test Conditions
CI	Input Capacitance	BBCLK		15	pF	
		All Others		10	pF	
CIO	I/O Capacitance			20	pF	
COC	Output Capacitance			20	pF	

Note:

- Periodically sampled rather than 100% tested.

PROGRAMMABLE INTERRUPT CONTROLLER

FEATURES

- Compatible with 8086, 8088, and similar microprocessors
- Low power consuming CMOS
- Interrupt modes are programmable
- Minimizes software overhead
- Eight prioritized control levels
- 64 levels of expandability
- Single 5 V power supply
- 28-pin DIP Package

DESCRIPTION

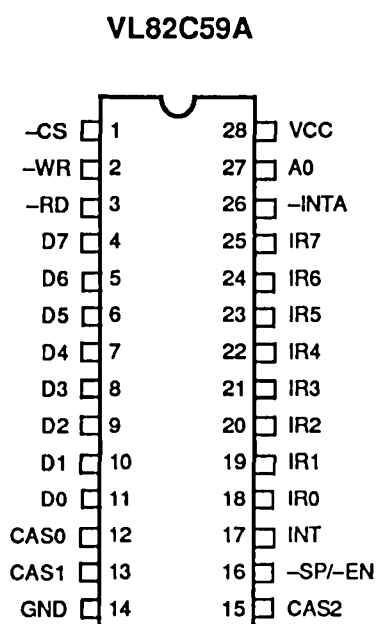
The VL82C59A Programmable Interrupt Controller can manage up to eight vectored priority interrupts for the system's CPU. It can be cascaded to handle up to 64 interrupts. No additional circuitry is required.

The VL82C59A has been designed to relieve the software of the burden of handling multi-level priority interrupts. It controls several modes, permitting optimization for a large number of system needs.

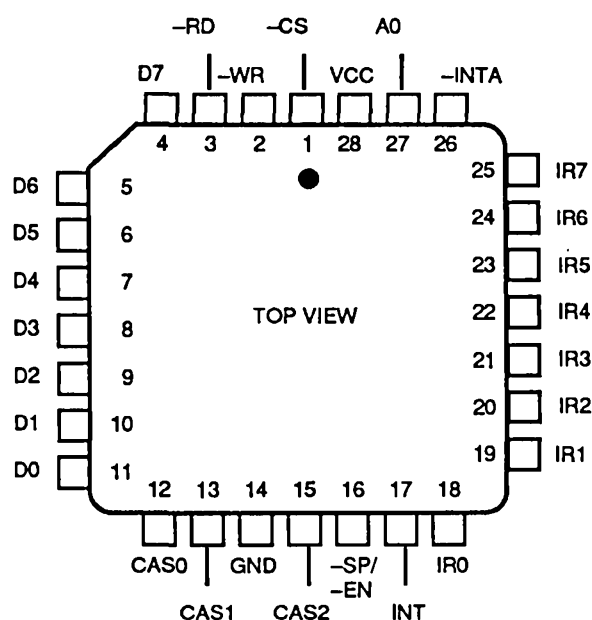
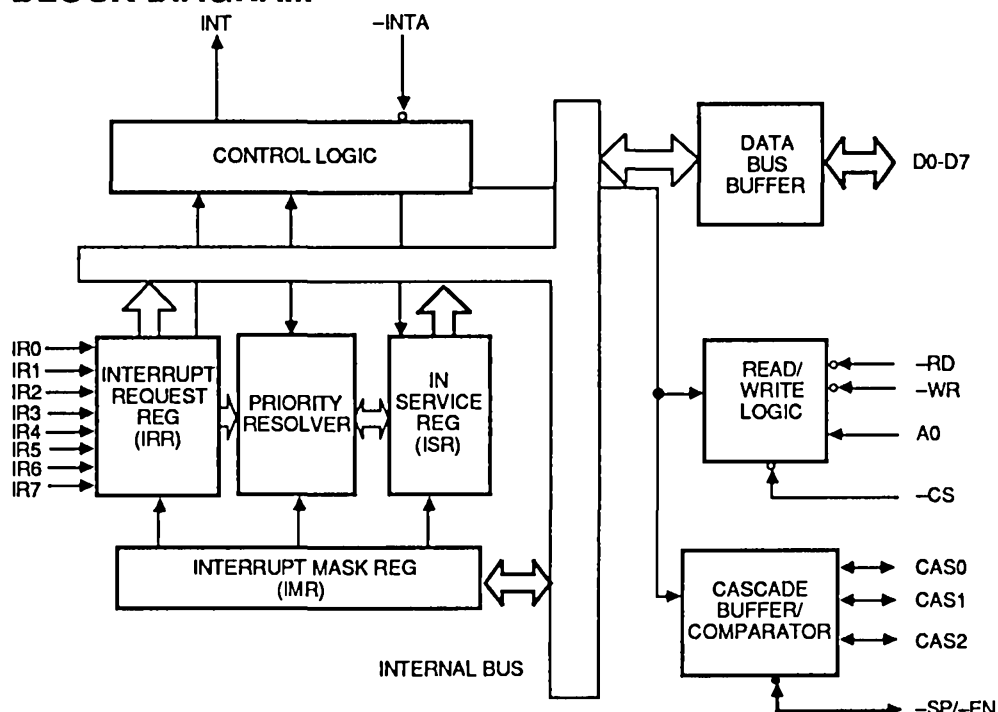
The VL82C59A is fully upward compatible with the HMOS 8259 or 8259A. Software originally written for the HMOS 8259 or 8259A will operate the VL82C59A in all 8259 or 8259A equivalent modes.

The VL82C59A is housed in a 28-pin DIP, uses CMOS technology and requires a single 5 V supply. The circuit is totally static, requiring no clock input.

PIN DIAGRAM



BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Bus Speed	Package
VL82C59A-08PC	8 MHz	Plastic DIP
VL82C59A-08QC		Plastic Leaded Chip Carrier (PLCC)
VL82C59A-08CC		Ceramic DIP
VL82C59A-10PC	10 MHz	Plastic DIP
VL82C59A-10QC		Plastic Leaded Chip Carrier (PLCC)
VL82C59A-10CC		Ceramic DIP

Note: Operating temperature range is 0°C to +70°C.

SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Type	Signal Description
-CS	1	I	Chip Select - A low on -CS enables -RD and -WR communication between the CPU and the VL82C59A. INTA functions are independent of -CS.
-WR	2	O	Write - A low on -WR when -CS is low enables the VL82C59A to accept command words from the CPU.
-RD	3	I	Read - A low on -RD when -CS is low enables the VL82C59A to release status onto the data bus for the CPU.
D0-D7	11-4	I/O	Bidirectional Data Bus - Control, status, and interrupt-vector information is transferred by this bus.
CAS0-CAS2	12, 13, 15	I/O	Cascade Lines - The CAS lines form a unique VL82C59A bus to control a multiple VL82C59A configuration. These pins are outputs for a master VL82C59A and inputs for a slave VL82C59A.
-SP/-EN	16	I/O	Slave Program/Enable Buffer - The -SP/-EN pin provides a dual function. When in the Buffered Mode, it can be used as an output to control the buffer transceivers (EN). When not in the buffered mode, it is used as an input to designate a master (SP = 1) or a slave (SP = 0).
INT	17	O	Interrupt - The INT pin goes high whenever a valid interrupt request is present. It is used to interrupt the CPU and is connected to the CPU's interrupt pin.
IR0-IR7	18-25	I	Interrupt Requests - Asynchronous inputs. An interrupt request is executed by raising an IR input (low to high) and holding it high until it is acknowledged (Edge Triggered Mode), by a high level on an IR input (Level Triggered Mode).
-INTA	26	I	Interrupt Acknowledge - The -INTA pin is used to enable the VL82C59A's interrupt-vector data onto the data bus by a sequence of interrupt acknowledge pulses issued from the CPU.
A0	27	I	A0 Address Line - The A0 pin acts together with the -CS, -WR, and -RD pins. It is used by the VL82C59A to decode various Command words the CPU writes and status the CPU needs to read. It is typically connected to the CPU A0 address line (A1 on the iAPX86, 88).
VCC	28	I	+5 V Supply
GND	14	I	Ground

FUNCTIONAL DESCRIPTION

The VL82C59A has been designed to be used in real-time, interrupt-driven microcomputer systems. It controls eight levels or requests, and has a built-in feature for expandability to other VL82C59A's (up to 64 levels). It is programmed by the system's software as an I/O peripheral. A selection of priority modes are usable by the programmer so that the way in which the requests are handled by the VL82C59A can be configured to match the system requirements. The priority modes can be changed at any time during the main program. The entire interrupt structure can be defined as needed, based on the total system requirements.

Interrupt Request Register (IRR) and In-Service Register (ISR) - The interrupts at the IR input lines are handled by two registers in cascade, the Interrupt Request Register (IRR) and the In-Service Register (ISR). The IRR stores all the interrupt levels which are requesting service, and the ISR stores all of the interrupt levels which are being handled.

Priority Resolver - This logic block sets the priorities of the bits set in the IRR. The highest priority is selected and strobed into the corresponding bit of the ISR during the --INTA pulse.

Interrupt Mask Register (IMR) - The IMR holds the bits which mask the interrupt lines. The IMR changes the IRR. Masking of a higher priority input will not affect the interrupt request lines of a lower priority.

Interrupt (INT) - This output interfaces to the CPU interrupt input. The VOH level on this line has been designed to be fully compatible with the 8080A, 8085A and 8086 input levels.

Interrupt Acknowledge (--INTA) - The --INTA pulses will cause the VL82C59A to release vectoring information onto the data bus. The format of this data depends on the system mode of the VL82C59A.

Data Bus Buffer - This three-state, bidirectional 8-bit buffer is used to interface the VL82C59A to the system Data Bus. Control words and status information are transferred through the Data Bus Buffer.

Read/Write Control Logic - The purpose of this block is to accept output commands from the CPU. It contains the Initialization Command Word (ICW) registers and Operation Command Word (OCW) registers. They store the various control formats for device operation. This function block also permits the status of the VL82C59A to be transferred onto the Data Bus.

Chip Select (--CS) - A low on this input enables the VL82C59A. Reading or writing of the chip will not occur unless the device is selected.

Write (--WR) - A low on this input permits the CPU to write control words (ICWs and OCWs) to the VL82C59A.

Read (--RD) - A low on this input enables the VL82C59A to transmit the status of the Interrupt Request Register (IRR), In-Service Register (ISR), the Interrupt Mask Register (IMR), or the interrupt level to the Data bus.

Cascade Buffer/Comparator - This function block stores and compares the identities of all VL82C59A's used in the system. The three I/O pins (CAS0-CAS2) are outputs when the VL82C59A functions as a master and are inputs when the VL82C59A functions as a slave. As a master, the VL82C59A sends the identity of the interrupting slave device onto the CAS0-CAS2 lines. The slave selected can now send its preprogrammed address to the Data Bus during the next consecutive --INTA pulses.

Interrupt Sequence - Interrupt routine addressing is a very important aspect of VL82C59A operation, as is device programmability. Interrupt routine addressing permits direct or indirect jumping to the specific interrupt routine requested with no polling of the interrupting devices. The activities occurring during an interrupt depends on the type of CPU being used.

The events occur as shown below in an MCS 80/85 system:

1. Interrupt Request lines (IR0-IR7) are raised high, setting the corresponding IRR bit(s).
2. The VL82C59A evaluates these

requests, then sends an INT to the CPU, if necessary.

3. The CPU acknowledges the INT and responds with the --INTA pulse.
4. When receiving an --INTA from the CPU group, the highest priority ISR bit is asserted, and the proper IRR bit is reset. The VL82C59A will also send a CALL instruction code (11001101) to the 8-bit Data Bus through its D0-D7 pins.
5. The CALL instruction will initiate two additional --INTA pulses which will be sent to the VL82C59A from the CPU group.
6. The two --INTA pulses permit the VL82C59A to send its preprogrammed subroutine address to the Data Bus. The lower 8-bit address is sent at the first --INTA pulse and the higher 8-bit address is sent at the next --INTA pulse.
7. The 3-byte CALL instruction sent by the VL82C59A is then completed. In the AEOI mode, the ISR bit is reset at the end of the third --INTA pulse. If not, the ISR bit remains set until an appropriate EOI command is issued at the end of the interrupt sequence.

The sequence of events occurring in an iAPX86-type system are the same until step 4. The sequence then continues:

4. When receiving an --INTA from the CPU group, the highest priority ISR bit is set and the corresponding IRR bit is reset. The VL82C59A does not use the Data Bus during this cycle.
5. The iAPX 86/10 will send a second --INTA pulse. During this second pulse, the VL82C59A releases an 8-bit pointer to the Data Bus and it is read by the CPU.
6. The interrupt cycle is then complete. In the AEOI mode the ISR bit is reset at the end of the second --INTA pulse. If not, the ISR bit remains set until a valid EOI command is sent at the end of the interrupt subroutine.

If there is no interrupt request present at step 4 of either sequence (i.e., the



request duration was too short) the VL82C59A will send an interrupt level 7. Both the vectoring bytes and the CAS lines will appear as though an interrupt level 7 was requested.

INTERRUPT SEQUENCE OUTPUTS FOR MCS-80® & MCS-85®

This sequence is timed by three -INTA pulses. During the first -INTA pulse the CALL opcode is enabled onto the Data Bus.

CONTENTS OF FIRST INTERRUPT VECTOR BYTE

CALL OPCODE	D7	D6	D5	D4	D3	D2	D1	D0
	1	1	0	0	1	1	0	1

During the second -INTA pulse the lower address of the selected service routine is enabled to the data bus. When the interval = 4 address bits A5-A7 are programmed, while addresses A0-A4 are automatically inserted by the VL82C59A. When interval = 8 only A6 and A7 are programmed, while A0-A5 are automatically inserted.

CONTENT OF SECOND INTERRUPT VECTOR BYTE

IR	Interval = 4							
	D7	D6	D5	D4	D3	D2	D1	D0
7	A7	A6	A5	1	1	1	0	0
6	A7	A6	A5	1	1	0	0	0
5	A7	A6	A5	1	0	1	0	0
4	A7	A6	A5	1	0	0	0	0
3	A7	A6	A5	0	1	1	0	0
2	A7	A6	A5	0	1	0	0	0
1	A7	A6	A5	0	0	1	0	0
0	A7	A6	A5	0	0	0	0	0

IR	Interval = 8							
	D7	D6	D5	D4	D3	D2	D1	D0
7	A7	A6	1	1	1	0	0	0
6	A7	A6	1	1	0	0	0	0
5	A7	A6	1	0	1	0	0	0
4	A7	A6	1	0	0	0	0	0
3	A7	A6	0	1	1	0	0	0
2	A7	A6	0	1	0	0	0	0
1	A7	A6	0	0	1	0	0	0
0	A7	A6	0	0	0	0	0	0

During the third INTA pulse, the higher address of the correct service routine-programmed as byte 2 of the initialization sequence (address lines A8-A15)-is enabled to the bus.

CONTENT OF THIRD INTERRUPT VECTOR BYTE

D7	D6	D5	D4	D3	D2	D1	D0
A15	A14	A13	A12	A11	A10	A9	A8

INTERRUPT SEQUENCE OUTPUTS FOR IAPX86® & IAPX88®

iAPX 86 mode is the same as the MCS-80 mode, with the exception that only two interrupt acknowledge cycles are issued by the processor and no CALL opcode is sent to the processor. The first interrupt acknowledge cycle is like that of MCS-80, 85 systems in that the VL82C59A uses it to internally hold the state of the interrupts for priority resolution. As a master, it issues the interrupt code on the cascade lines at the termination of the INTA pulse. On this first cycle, it does not send any data to the processor. It leaves its Data Bus buffers disabled. On the second interrupt acknowledge cycle (in iAPX86 and iAPX88 modes) the master (or slave) will send a byte of data to the processor with the acknowledged interrupt code as follows (The state of the ADI mode control is ignored and address lines A5-A11 are unused in iAPX86 and iAPX88 mode.):

CONTENT OF INTERRUPT VECTOR BYTE FOR iAPX86, iAPX88 SYSTEM MODE

	D7	D6	D5	D4	D3	D2	D1	D0
IR7	T7	T6	T5	T4	T3	1	1	1
IR6	T7	T6	T5	T4	T3	1	1	0
IR5	T7	T6	T5	T4	T3	1	0	1
IR4	T7	T6	T5	T4	T3	1	0	0
IR3	T7	T6	T5	T4	T3	0	1	1
IR2	T7	T6	T5	T4	T3	0	1	0
IR1	T7	T6	T5	T4	T3	0	0	1
IR0	T7	T6	T5	T4	T3	0	0	0

PROGRAMMING

The VL82C59A uses two types of command words generated by the CPU:

1. Initialization Command Words (ICWs): Before normal operation begins, each VL82C59A in the system should be brought to a starting point. This is done by a sequence of 2 to 4 bytes timed by -WR pulses.
2. Operation Command Words (OCWs): OCWs are the command words which command the VL82C59A to operate in various interrupt modes. These modes are:
 - A. Fully nested mode
 - B. Rotating priority mode
 - C. Special mask mode
 - D. Polled mode

The OCWs may be written into the VL82C59A anytime following initialization.

Initialization Command Words (ICWs) - When a command is issued with address line A0 = 0 and D4 = 1, this is decoded as Initialization Command Word 1 (ICW1). ICW1 commences the initialization sequence during which the following occurs:

- A. The edge sense circuit is reset. Following initialization, an interrupt request (IR) input should make a low-to-high transition to generate an interrupt.
- B. The Interrupt Mask Register is cleared.
- C. IR7 input is assigned priority 7.
- D. The slave mode address is set to 7.
- E. Special Mask Mode is cleared and Status Read is set to IRR.
- F. If IC4 = 0, all functions that were selected in ICW4 are set to zero. (Non-Buffered mode, no Auto-EOI, MCS-80 and MCS-85 system. Master/Slave in ICW4 is only used in the buffered mode.)

Initialization Command Words 1 and 2 (ICW1, ICW2) - A5-A15: Page starting address of service routines. In an MCS80/MCS85 system, all eight request levels will generate CALLs to eight locations equally separated in memory. These can be programmed to be separated at intervals of four or eight memory locations. The eight routines

will then occupy a page of 32 or 64 bytes, respectively.

The address format is 2 bytes in length (A0-A15). When the routine interval is 4, A0-A4 are inserted by the VL82C59A, while A5-A15 are externally programmed. When the routine interval is 8, A0-A5 are inserted by the VL82C59A, while A6-A15 are externally programmed.

The 8-byte interval will maintain compatibility with software presently being used, while 4-byte interval should be used for a small jump table.

In an iAPX86 and iAPX88 system address lines A15-A11 are inserted in the five most significant bits of the vectoring byte and the VL82C59A sets the three least significant bits in accordance with the interrupt level. A10-A5 are ignored and ADI (Address Interval) is not used.

LTIM: If LTIM = 1, the VL82C59A will operate in the level interrupt mode. Edge detection logic on the interrupt inputs will be disabled.

ADI: CALL address interval. ADI = 1 then interval = 4; ADI = 0 then interval = 8.

SNGL: Single. This indicates that only one VL82C59A is in the system. If SNGL = 1 no ICW3 will be issued.

IC4: If this bit is set, ICW4 must be read. If ICW4 is not used, set IC4 = 0.

Initialization Command Word 3 (ICW3) - This word indicates that there is more than one VL82C59A in the system and cascading is used (SNGL = 0). It will load the 8-bit slave register. The functions of this register are below:

A. In the master mode (either when SP = 1, or in buffered mode when M/S = 1 in ICW4) a "1" is set for every slave in the system. The master will release byte 1 of the CALL sequence (for MCS80/MCS85 system) and will then enable the corresponding slave to release bytes 2 and 3 (for iAPX86, iAPX88 only byte 2) through the cascade lines.

B. In the slave mode (either when -SP = 0, or if BUF = 1 and M/S = 0 in ICW4) bits 2-0 identify the slave.

The slave compares its cascade input with these bits. If they are equal, bytes 2 and 3 of the CALL sequence (or just byte 2 of iAPX86, iAPX88) are released by it on the Data Bus.

Initialization Command Word (ICW4) - SFNM: If SFNM = 1, the special fully nested mode is programmed.

BUF: If BUF = 1, then the buffered mode is programmed. In buffered mode -SP/-EN becomes an enable output and the master/slave selection is made by M/S.

M/S: M/S = 1 indicates the VL82C59A is a master, M/S = 0 indicates the VL82C59A is a slave. If BUF = 0, M/S has no meaning.

AEOI: If AEOI = 1, then the automatic end of interrupt mode is programmed.

Microprocessor mode: μ PM = 0 sets the VL82C59A for MCS80, MCS85 system operation. μ PM = 1 sets the VL82C59A for iAPX86 system operation.

Operation Command Words (OCWs) - After the initialization Command Words (ICWs) are programmed into the VL82C59A, the chip is prepared to accept interrupt requests on its inputs. During VL82C59A operation, a selection of algorithms can command the VL82C59A to operate in different modes through the Operation Command Words (OCWs).

OPERATING CONTROL WORDS (OCWs)

OCW1								
A0	D7	D6	D5	D4	D3	D2	D1	D0
1	M7	M6	M5	M4	M3	M2	M1	M0

OCW2								
A0	D7	D6	D5	D4	D3	D2	D1	D0
0	R	SL	EOI	0	0	L2	L1	L0

OCW3								
A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	ESSM	SMM	0	1	P	RR	RIS

Operation Control Word (OCW1) - OCW1 sets and clears the mask bits in the interrupt Mask Register (IMR). M7-M0 control the eight mask bits. M = 1 indicates the channel is masked, M = 0 indicates the channel is enabled.

Operation Control Word 2 (OCW2) - R, SL, EOI - These three bits control the Rotate and End of Interrupt modes and their combinations. A drawing of these combinations can be found on the Operation Command Word Format, Figure 3.

L2, L1, L0 - These bits determine the interrupt level responded to when the SL bit is active.

Operation Control Word 3 (OCW3) ESM - Enable Special Mask Mode. When this bit is set to 1 it enables the SMM bit to set or reset the Special Mask Mode. When ESM = 0 the SMM bit is a "don't care".

SMM - Special Mask Mode. If ESM = 1 and SMM = 1 the VL82C59A will enter Special Mask Mode. If ESM = 1 and SMM = 0 the VL82C59A will revert to normal mask mode. When ESM = 0, SMM is not used.

FIGURE 1. INITIALIZATION SEQUENCE

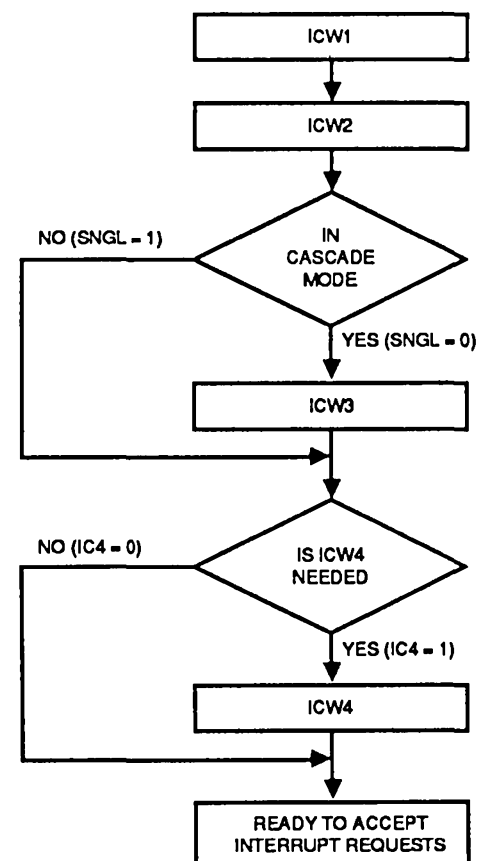
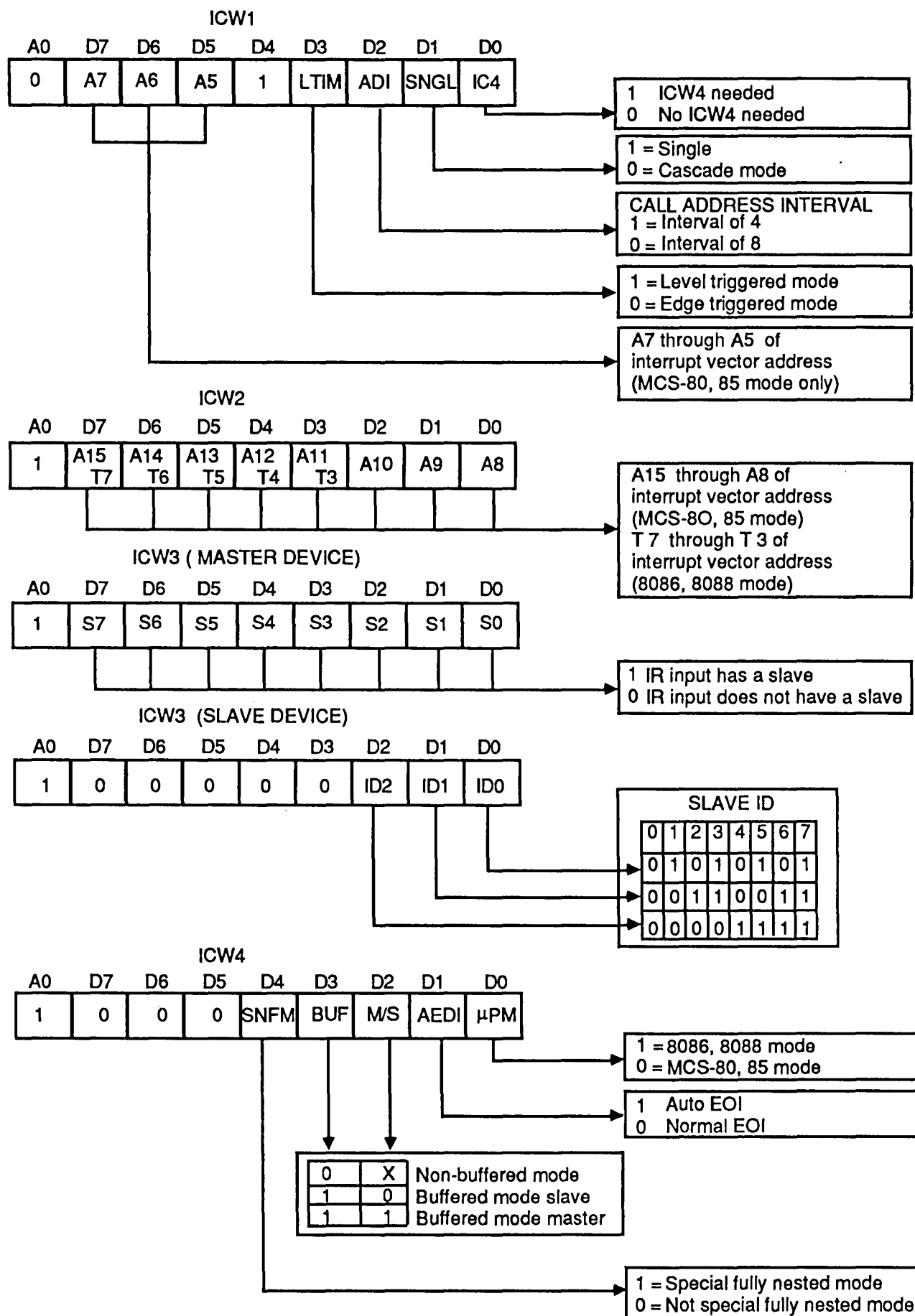
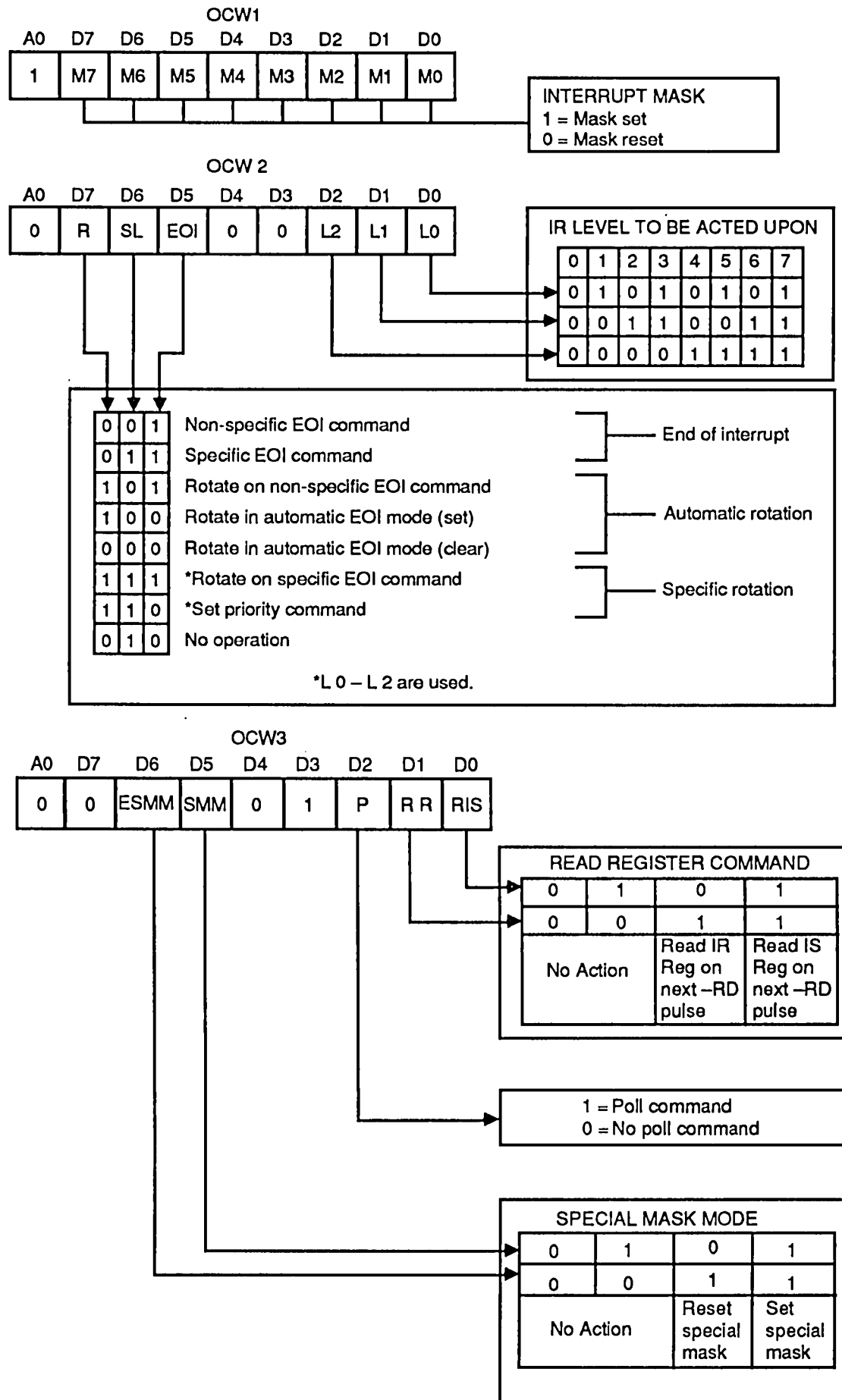


FIGURE 2. INITIALIZATION COMMAND WORD FORMAT



Note: Slave ID is equal to the corresponding master IR input.

FIGURE 3. OPERATION COMMAND WORD FORMAT



MODES

Fully Nested Mode - This is the default mode after initialization unless another mode is programmed. The interrupt requests are ordered in priority from 0 through 7 (0 highest). When an interrupt is acknowledged, the highest priority request is decoded and its vector placed onto the bus. A bit of the Interrupt Service register (IS0-IS7) is also set. This bit stays set until the microprocessor issues an End of Interrupt (EOI) command before returning from the service routine. It also stays set if the AEOL (Automatic End of Interrupt) bit is set, until the trailing edge of the last INTA. While the In-Service (IS) bit is set, all further interrupts of the same or lower priority are disabled. Higher levels will generate an interrupt.

After the initialization sequence, IR0 has the highest priority and IR7 the lowest. Priorities may be changed in the rotating priority mode.

End of Interrupt (EOI)- The In-Service (IS) bit may be reset either automatically following the trailing edge of the last in sequence -INTA pulse (when AEOL bit in ICW1 is set), or by a command word that should be issued to the VL82C59A before returning from a service routine (EOI command). An EOI command is issued twice if in the Cascade mode, once for the master and once for the corresponding slave.

Two forms of an EOI command are used; Specific and Non-Specific. When the VL82C59A is operated in modes which maintain the fully nested structure, it can determine which IS bit to reset on EOI. When a Non-Specific EOI command is sent the VL82C59A will reset the highest IS bit of those that are set. In the fully nested mode the highest IS level was necessarily the last level operated upon. A Non-Specific EOI can be sent with OCW2 (EOI = 1, SL = 0, R = 0).

When a mode may change the fully nested structure, the VL82C59A may not be able to determine the last level responded to. A Specific End of Interrupt must then be issued, which includes IS level to be reset as part of the command. A Specific EOI can be sent with OCW2 (EOI = 1, SL = 1, R =

0, and L0-L2 is the binary level of the IS bit to be reset).

When the IS is masked by an IMR bit, it will not be cleared by a Non-Specific EOI, if the VL82C59A is in the Special Mask Mode.

Automatic End of Interrupt (AEOL) Mode - If AEOL = 1 in ICW4, then the VL82C59A will operate in AEOL mode until changed by ICW4. In this mode, the VL82C59A will perform a Non-Specific EOI operation at the trailing edge of the last interrupt acknowledge pulse. This mode should be used only when a nested multilevel interrupt structure is not required in a single VL82C59A.

The AEOL mode can only be used in a master VL82C59A.

Automatic Rotation (Equal Priority Devices) - In many applications there are several interrupting devices of equal priority. In this mode the device receives the lowest priority. A device requesting an interrupt will wait, in the worst case, until each of seven other devices with higher priority are serviced. If the priority and "in service" status is:

Before Rotate (IR4 the highest priority-requiring service)

	IS7	IS6	IS5	IS4	IS3	IS2	IS1	IS0
"IS" Status	0	1	0	1	0	0	0	0
	Lowest Priority				Highest Priority			
Priority Status	7	6	5	4	3	2	1	0

After Rotate (IR4 was serviced):

	IS7	IS6	IS5	IS4	IS3	IS2	IS1	IS0
"IS" Status	0	1	0	0	0	0	0	0
	Highest Priority				Lowest Priority			
Priority Status	2	1	0	7	6	5	4	3

There are two ways to accomplish Automatic Rotation using OCW2, the Rotation on Non-Specific EOI Command (R = 1, SL = 0, EOI = 1) and the Rotate in Automatic EOI Mode which is set by (R = 1, SL = 0, EOI = 0) and cleared by (R = 0, SL = 0, EOI = 0).

Specific Rotation (Specific Priority) - The programmer may change priorities by programming the bottom priority and thereby fixing all of the other priorities (e.g., if IR5 is programmed as the

bottom priority device, then IR6 will be the highest one).

The Set Priority command is issued in OCW2 where: R = 1, SL = 1; L0-L2 is the binary priority level code of the bottom priority device.

In this mode internal status is updated by software control during OCW2. It is independent of the End of Interrupt (EOI) command. Priority changes may be performed during an EOI command by using the Rotate on Specific EOI command in OCW2 (R = 1, SL = 1, EOI = 1, and L0-L2 = IR level to receive bottom priority).

Interrupt Masks - Each Interrupt Request input may be masked individually by the Interrupt Mask Register (IMR) by programming OCW1. Each bit in the IMR masks one interrupt channel when it is set (1). Bit 0 masks IR0, bit 1 masks IR1, etc. Masking an IR channel has no affect on the other channels operation.

Special Mask Mode - Some applications will require an interrupt service routine to change the system priorities during its execution under program control. The routine may need to inhibit lower priority requests for a portion of its execution, but enable some, for another portion.

If an Interrupt Request is acknowledged and an End of Interrupt command did not reset the IS bit during a service routine, the VL82C59A will inhibit all lower priority requests without a simple routine to enable them.

In the Special Mask Mode, a mask bit set in OCW1 inhibits further interrupts at that level and enables interrupts from all other levels that are not masked.

Any interrupts may be enabled selectively by loading the mask register.

The Special Mask Mode is set by OCW3 when: SSMM = 1, SMM = 1, and cleared where SSMM = 1, SMM = 0.

Poll Command - In this mode the INT output is disabled or the microprocessor internal Interrupt Enable flip-flop is reset, disabling its interrupt input. Service to devices is programmed by software using a Poll command.

The Poll command is issued by setting $P = "1"$ in OCW3. The VL82C59A treats the next $-\text{RD}$ pulse to the VL82C59A (i.e., $-\text{RD} = 0$, $-\text{CS} = 0$) as an interrupt acknowledge, sets the appropriate IS bit if requested and reads the priority level. Interrupt is frozen from $-\text{WR}$ to $-\text{RD}$.

The word enabled to the data bus during $-\text{RD}$ is:

D7	D6	D5	D4	D3	D2	D1	D0
1	—	—	—	—	W2	W1	W0

W0-W2: Binary code of the highest priority level requesting service.

1: Equal to a "1" if there is an interrupt.

This mode is most useful when there is a routine command common to several levels. Then the $-\text{INTA}$ sequence is not needed. It is frequently useful to expand the number of priority levels to more than 64.

VL82C59A STATUS

The input status of several internal registers can be read to update user information from the system. The following registers can be read by using OCW3 (IRR and ISR or OCW1 (IMR)).

Interrupt Request Register (IRR): 8-bit register which contains the levels requesting an interrupt to be acknowledged. The highest request level is reset from the IRR when an interrupt is serviced. (Not affected by IMR.)

In-Service Register (ISR): 8-bit register which contains the priority levels that are being updated. The ISR is changed when an End of Interrupt Command is sent.

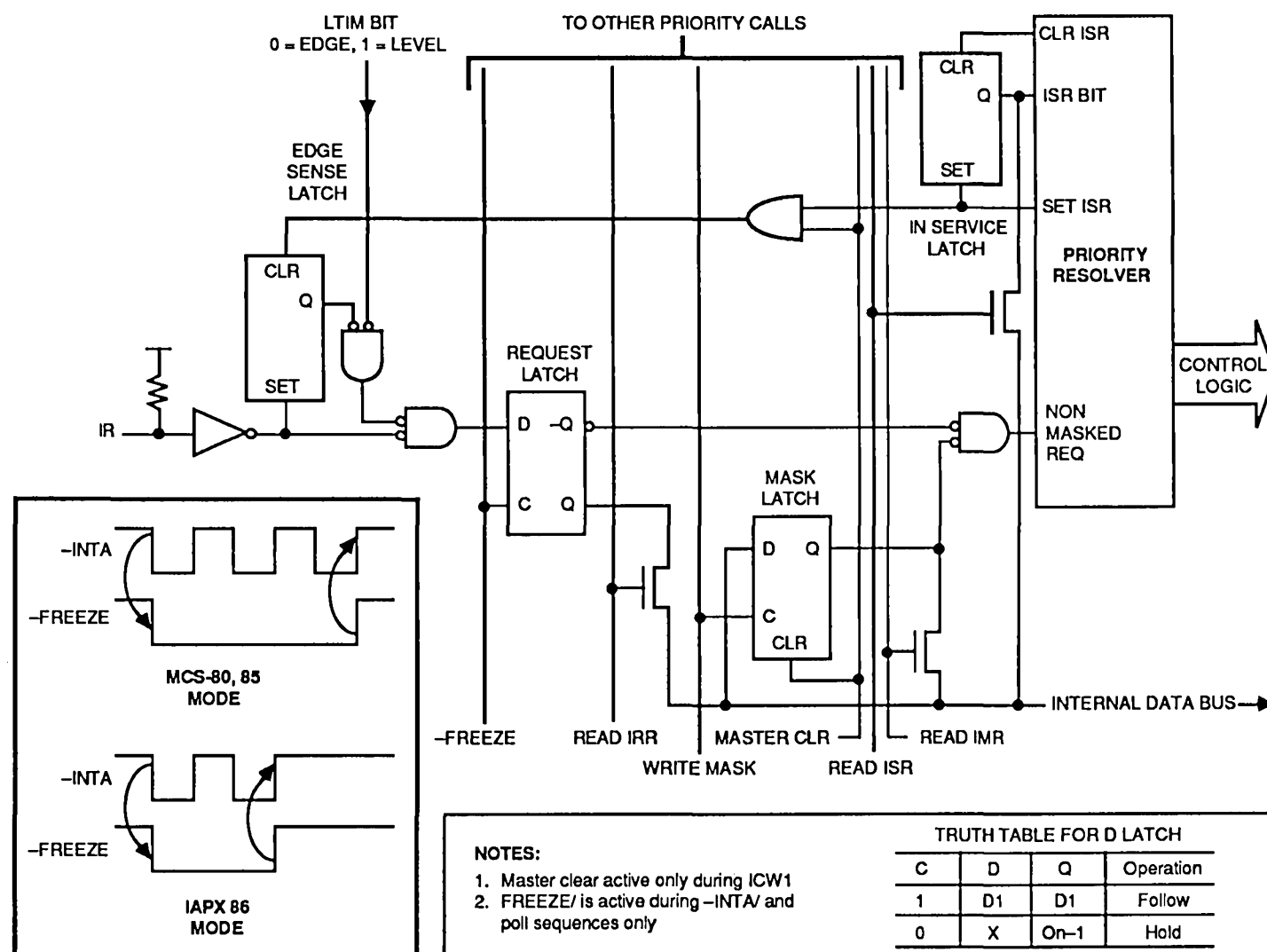
Interrupt Mask Register: 8 bit register which contains the interrupt request lines which are masked.

The IRR may be read when, prior to the $-\text{RD}$ pulse, a Read Register Command is sent with OCW3 ($\text{RR} = 1$, $\text{RIS} = 0$).

The ISR may be read when, prior to the $-\text{RD}$ pulse, a Read Register Command is sent with OCW3 ($\text{RR} = 1$, $\text{RIS} = 1$).

OCW3 is not written before every status read operation, as long as the status read corresponds with the previous one.

FIGURE 4. PRIORITY CELL—SIMPLIFIED LOGIC DIAGRAM



The VL82C59A retains whether the IRR or ISR has been previously selected by the OCW3. This is untrue when the poll is used.

After initialization, the VL82C59A is set to IRR.

For reading the IMR, no OCW3 is needed. The output data bus will contain the IMR when $\overline{\text{RD}}$ is active and $\text{A0} = 1$ (OCW1).

Polling overrides a status read when $\text{P} = 1$, $\text{RR} = 1$ in OCW3.

Edge and Level Triggered Modes - This mode is selected using bit 3 in ICW1.

If $\text{LTIM} = 0$, an interrupt request will be recognized by a positive-going transition on an IR input. The IR input may stay high without generating another interrupt.

If $\text{LTIM} = 1$, an interrupt request can be recognized by a high level on IR input and there is no requirement for edge detection. The interrupt request should be disabled before the EOI command is issued or the CPU interrupt is enabled to preclude a second interrupt from occurring.

Figure 4, shows a basic circuit of the level sensitive and edge sensitive input circuitry of the VL82C59A. The request latch is a "D" type latch, which is transparent.

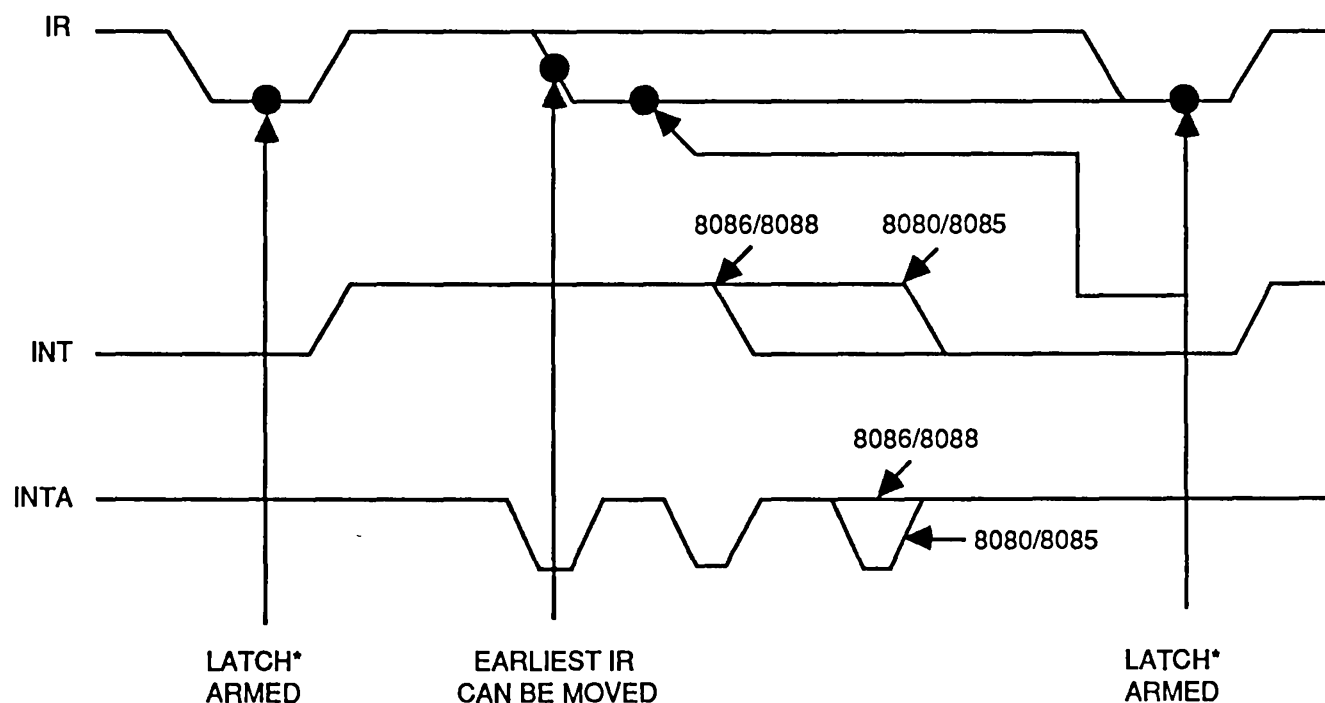
In the edge and level triggered modes, the IR inputs should stay high until after the falling edge of the first INTA. If the IR input goes low before this time, a default IR7 occurs when the CPU responds to the interrupt. This may detect interrupts generated by noise on the IR inputs. The IR7 routine is used for smoothing by simply executing a return instruction thus ignoring the interrupt. If IR7 is needed for other purposes a default IR7 can still be detected by reading the ISR. A normal IR7 interrupt will set the corresponding ISR bit, a default IR7 will not. If a default IR7 routine occurs during a normal IR7 routine, the ISR will remain set. It is necessary to record whether or not the IR7 routine was previously entered. If another IR7 occurs, it is a default.

The Special Fully Nested Mode - This mode can be used for a big system, where cascading occurs, and the

priority has to be saved by each slave. Using ICW4, the fully nested mode will be programmed to the master. This mode is the same as the normal nested mode, except as follows:

- A. When an interrupt request from a given slave is in service, the slave is not locked out from the master's priority logic. Further interrupt requests from higher priority IR's within the slave will be recognized by the master and will initiate interrupts to the processor. In the normal nested mode a slave is masked out when its request is in service and no higher requests from the same slave can be handled.
- B. When exiting the Interrupt Service routine, the software has to insure that the interrupt serviced was the only one from the slave. This is accomplished by sending a Non-Specific End of Interrupt (EOI) command to the slave, then reading its In-Service register and checking for zero. If empty, a Non-Specific EOI may be sent. If not, no EOI may be sent.

FIGURE 5. IR TRIGGERING TIMING REQUIREMENT



*Edge Triggered Mode Only

Buffered Mode - When the VL82C59A is used in a large system and bus driving buffers are needed, on the data bus (when the cascading mode is used) enabling buffers may cause difficulty.

The buffered mode will structure the VL82C59A to send an enable signal on -SP/-EN to enable the buffers in this mode, when the VL82C59A data bus outputs are enabled, the -SP/-EN output is active.

This change mandates the use of software programming to ascertain whether the VL82C59A is a master. Bit 3 in ICW4 programs the buffered mode, and bit 2 in ICW4 decides whether it is a master or a slave.

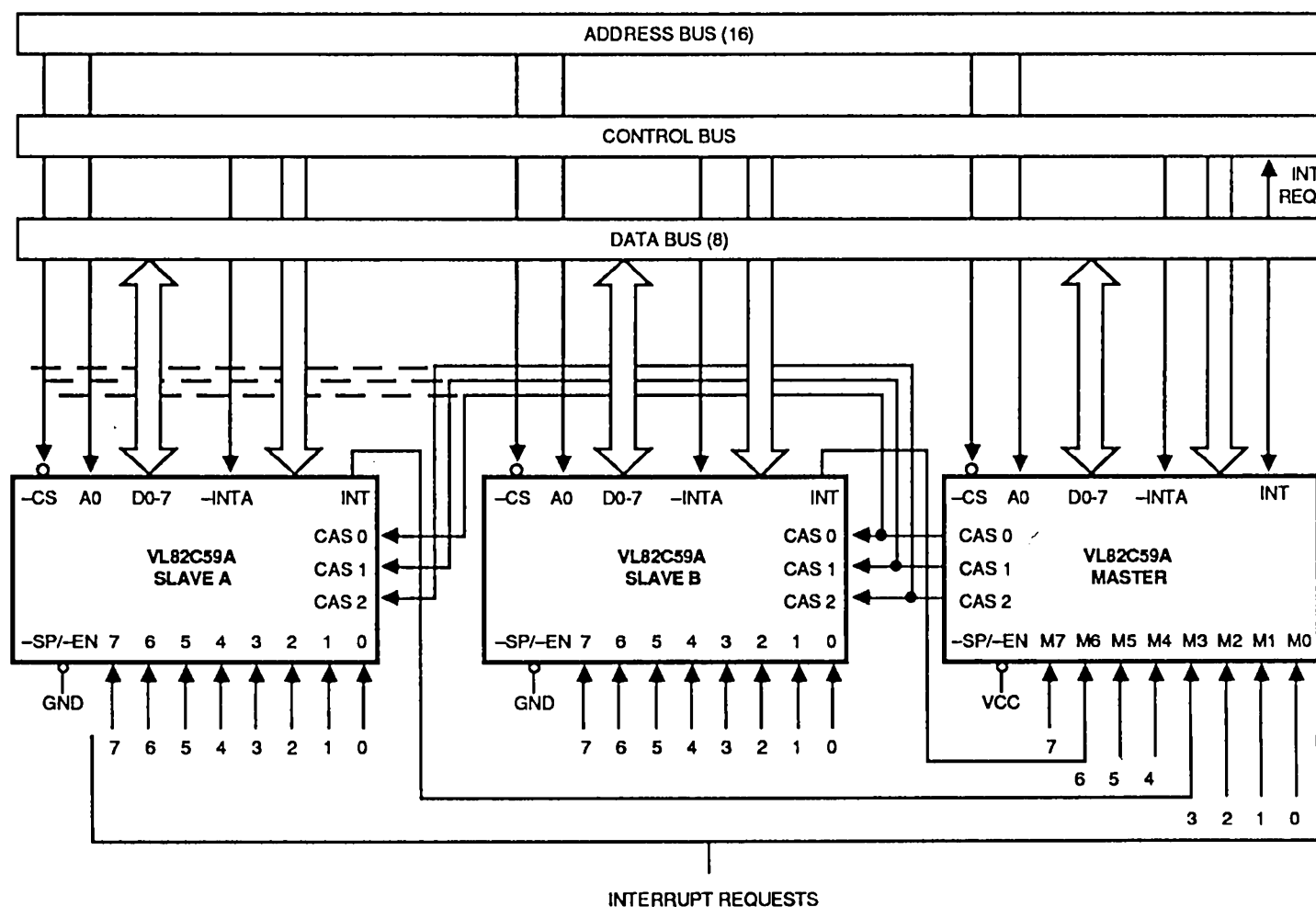
Cascade Mode - The VL82C59A may be interconnected in a system of a master with as many as eight slaves and handle up to 64 priority levels.

The master controls the slaves by the three-line cascade bus. The cascade bus is like chip selects to the slaves during the -INTA . In a cascade configuration, the slave interrupt outputs are connected to the master interrupt request inputs. When a slave request line is asserted and then acknowledged, the master will enable the slave to release the device routine address during bytes 2 and 3 of INTA . Byte 2 is only for 8086/8088-based systems.

The cascade bus lines are normally low and contain the slave address code from the falling edge of the first INTA pulse to the falling edge of the third pulse. All VL82C59As in the system must follow a separate initialization sequence. Each may be programmed to work in a different mode. An EOI command should be issued; once for the master, and once for the slave. An address decoder is needed to assert the Chip Select (CS) input of each VL82C59A.

The cascade lines of the Master VL82C59A are asserted for slave inputs. Non-slave inputs let the cascade line remain inactive (low).

FIGURE 6. CASCADING THE VL82C59A



AC CHARACTERISTICS: TA = 0°C to +70°C, VCC = 5 V ±10%
TIMING REQUIREMENTS

Symbol	Parameter	VL82C59A -08		VL82C59A -10		Units	Conditions
		Min	Max	Min	Max		
tAHL	A0/-CS Setup to -RD/-INTA Low	10				ns	
tRHAX	A0/-CS Hold after -RD/-INTA High	5				ns	
tRLRH	-RD/-INTA Pulse Width	160				ns	
tAHL	A0/-CS Setup to -WR Low	0				ns	
tWHAX	A0/-CS Hold after -WR High	0				ns	
tWLWH	-WR Pulse Width	190				ns	
tDVWH	Data Setup to -WR High	160				ns	
tWHD	Data Hold after -WR High	0				ns	
tLJH	Interrupt Request Width (Low)	100				ns	Note
tCVIAL	Cascade Setup to Second or Third -INTA Low (Slave Only)	40				ns	
tRHRL	End of -RD to next -RD End of -INTA to next -INTA within an -INTA sequence only	160				ns	
tWHWL	End of -WR to next -WR	190				ns	
tCHCL*	End of Command to Next Command (Not Same Command Type) End of -INTA Sequence to Next -INTA Sequence	400				ns	

*Worst case timing for tCHCL in an actual microprocessor system is typically much greater than 400 ns
(i.e. 8085A = 1.6 µs, 8085-A2 = 1 µs, 80C86 = 1 µs, 8086-2 = 625 ns).

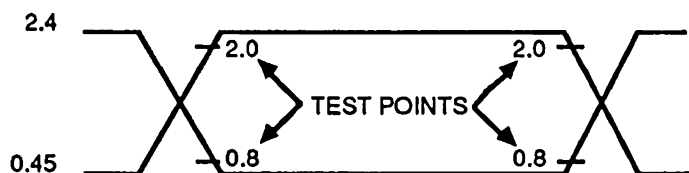
Note: This is the low time required to clear the input latch in the edge triggered mode.

TIMING RESPONSES

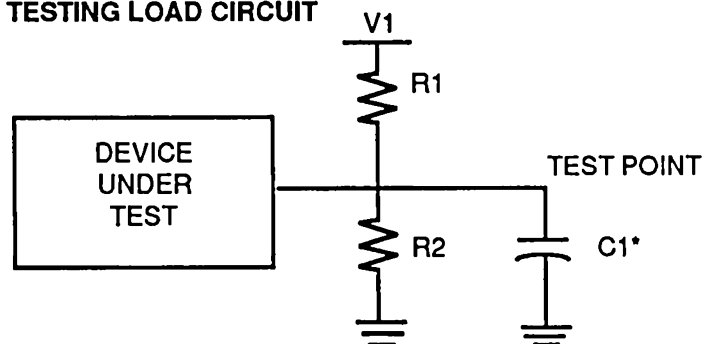
Symbol	Parameter	VL82C59A -08		VL82C59A -10		Units	Conditions
		Min	Max	Min	Max		
tRLDV	Data Valid from --RD/--INTA Low		120			ns	1
tRHDZ	Data Float after --RD/--INTA High	10	85			ns	2
tJHIH	Interrupt Output Delay		300			ns	1
tIALCV	Cascade Valid from First --INTA Low (Master Only)		360			ns	1
tRLEL	Enable Active from --RD Low or --INTA low		110			ns	1
tRHEH	Enable Inactive from --RD High or --INTA High		150			ns	1
tAHDV	Data Valid from Stable Address		200			ns	1
tCVDV	Cascade Valid to Valid Data		200			ns	1

TEST CONDITION DEFINITION TABLE

Test Condition	V1	R1	R2	C1
1	1.7 V	523 Ω	Open	100 pF
2	4.5 V	1.8 k Ω	1.8 k Ω	30 pF

TESTING INPUT, OUTPUT WAVEFORM


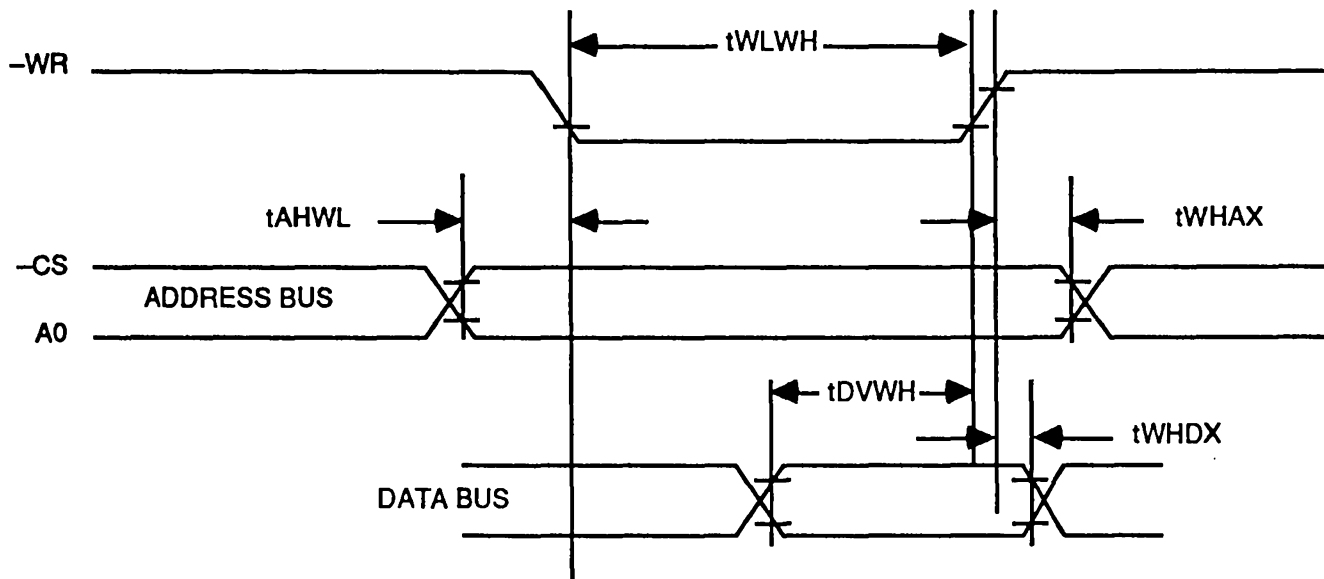
AC testing inputs are driven at 2.4 V for a Logic 1 and 0.45 V for a Logic 0. Timing measurements are made at 2.0 V for a Logic 1 and 0.8 V for a Logic 0.

TESTING LOAD CIRCUIT


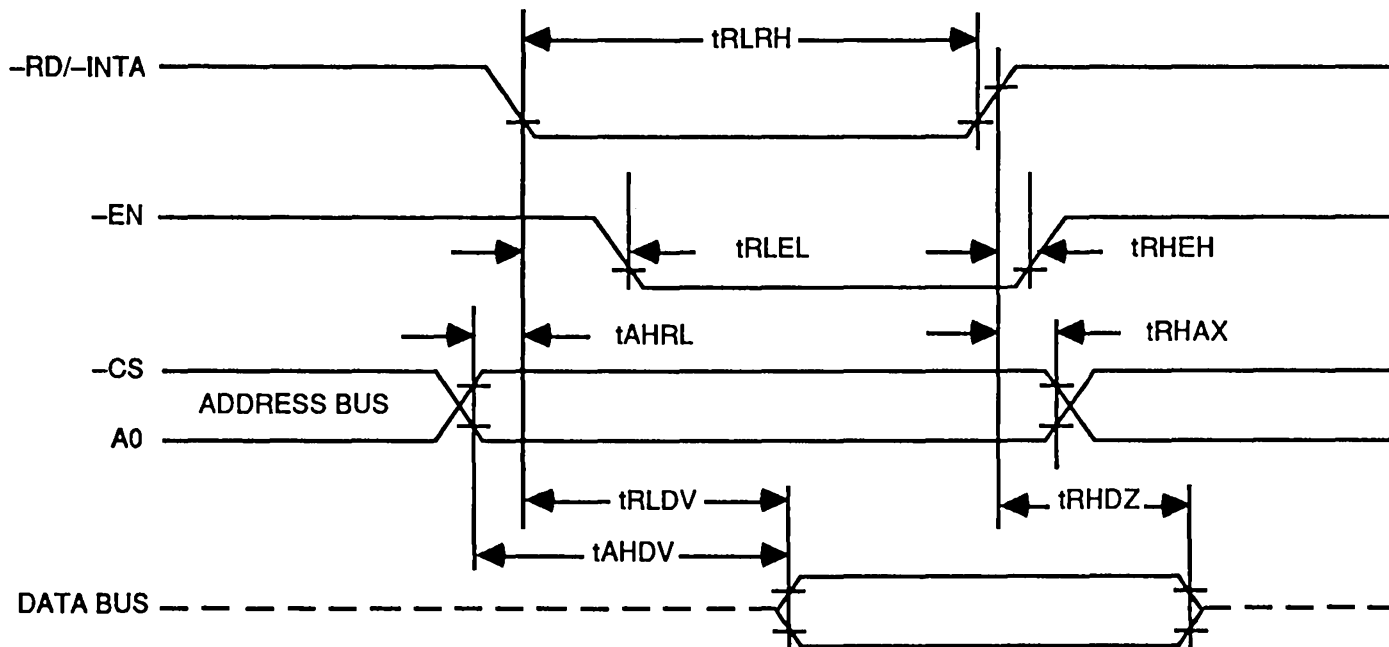
*Includes stray and jig capacitance.



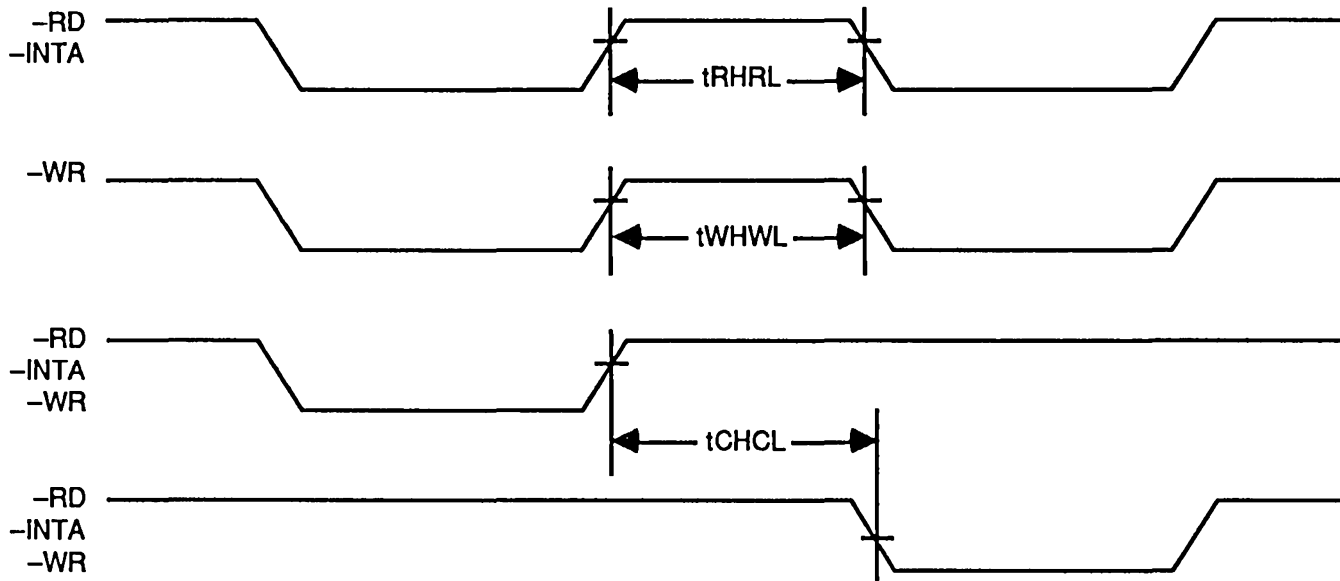
WRITE WAVEFORM



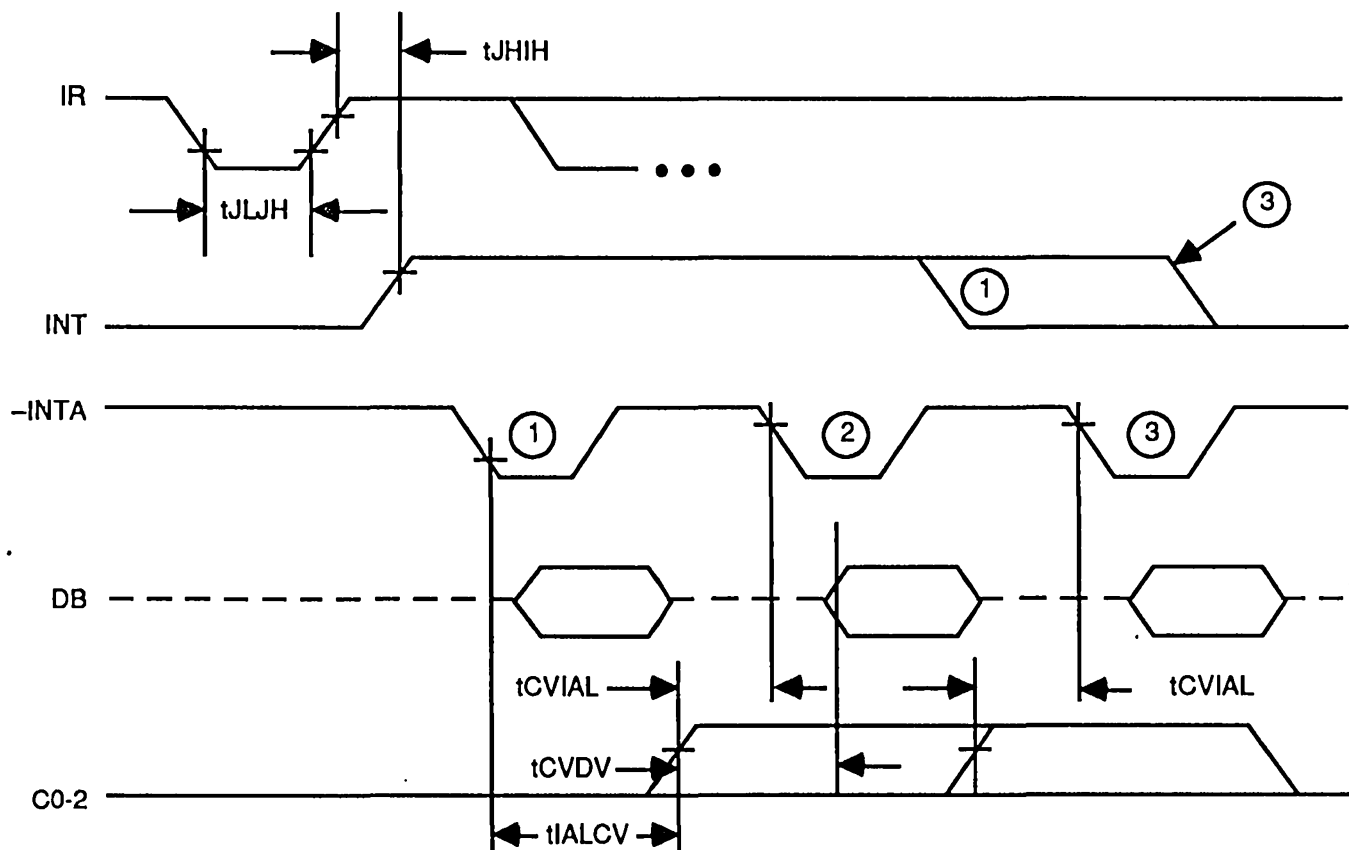
READ/INTA WAVEFORM



OTHER TIMING WAVEFORMS



-INTA SEQUENCE WAVEFORM



Notes: Interrupt output must remain HIGH at least until leading edge of first INTA.

1. Cycle 1 in iAPX 86, iAPX 88 systems, the Data Bus is not active.

ABSOLUTE MAXIMUM RATING

Ambient Temperature
 Under Bias 0°C to 70° C
 Storage Temperature -65°C to +150°C
 Voltage on Any Pin
 with Respect to Ground -0.5 V to 7 V
 Power Dissipation 1 Watt

Stresses above those listed may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those

indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS: TA = 0°C to 70°C, VCC = 5 V ±10%

Symbol	Parameter	VL82C59A -08		VL82C59A -10		Units	Conditions
		Min	Max	Min	Max		
VIL	Input Low Voltage	-0.5	0.8			V	
VIH	Input High Voltage	2.2	VCC + 0.5			V	
VOL	Output Low Voltage		0.4			V	IOL = 2.5 mA
VOH	Output High Voltage	3.0				V	IOH = -2.5 mA
		VCC - 0.4				V	IOH = -100 µA
ILI	Input Leakage Current		±1.0			µA	0 V ≤ VIN ≤ VCC
ILO	Output Leakage Current		±10.0			µA	0 V ≤ VOUT ≤ VCC
ILIR	IR Input Leakage Current		-300			µA	VIN = 0
			+10			µA	VIN = VCC
ICC	Operating Supply Current		5			mA	Note
ICCS	Standby Supply Current		10			µA	VIN = VCC or GND All IR = VCC Outputs Unloaded VCC = 5.5 V

Note: For extended temperature EXPRESS VIH = 2.3 V.

CAPACITANCE: TA = 25° C, VCC = GND = 0 V

Symbol	Parameter	Min	Max	Units	Test Conditions
CIN	Input Capacitance		7	pF	fc = 1 MHz
CI/O	I/O Capacitance		20	pF	Unmeasured pins returned to VSS
COU	Output Capacitance		15	pF	

Note: Capacitance values guaranteed and sampled, but not 100% tested.

PC-AT MEMORY MAPPER (74LS612)

FEATURES

- Expands address lines from four to 12
- Paged memory mapping design
- Three-state or open-collector map outputs
- Compatible with IBM PC/AT as well as most popular microprocessor-based systems
- Single 5 V power supply
- Low power-consuming CMOS technology
- Fully compatible with 74LS612

DESCRIPTION

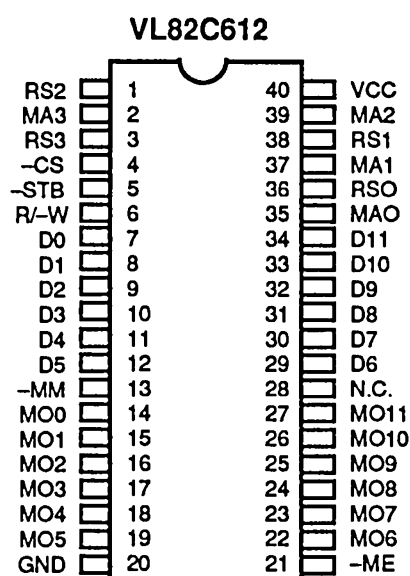
The VL82C612 CMOS memory-mapper integrated circuit contains a 4-line to 16-line decoder, a 16-word by 12-bit RAM, 16 channels of 2-line to 1-line multiplexers, and the necessary control logic to operate efficiently in an IBM PC/AT or most other microprocessor environments. The device is fabricated in CMOS technology to insure low power consumption and maximum system performance while remaining fully compatible with the 74LS612.

The memory-mapper expands the microprocessor's system memory

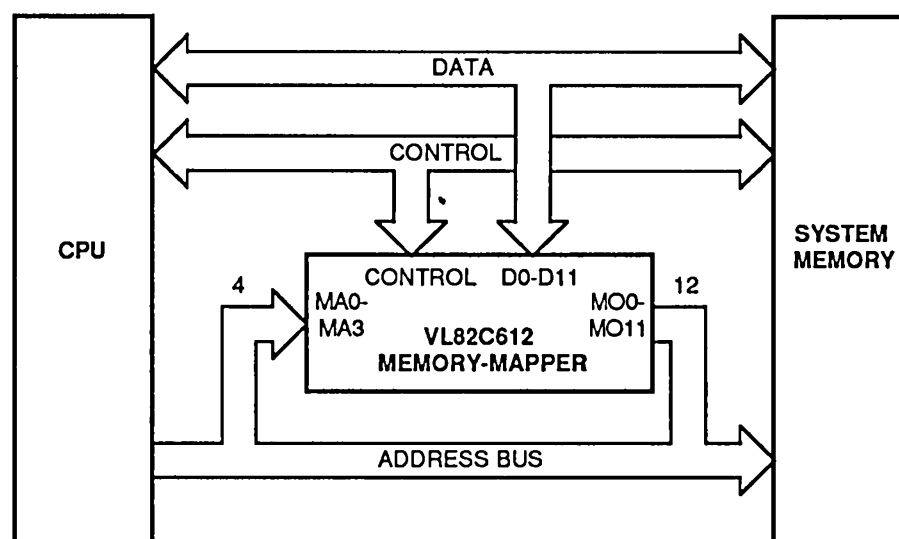
address capability by eight bits. Four bits of the memory address bus (see System Block Diagram below) can be used to select one of 16 map registers that contain 12 bits each. These 12 bits are presented to the system memory address bus through the map output buffers along with the remaining memory address bits from the CPU.

The device is available in a 40-pin DIP as well as a 44-pin plastic leaded chip carrier (PLCC).

PIN DIAGRAM



SYSTEM BLOCK DIAGRAM



PLEASE CONSULT DATA SHEET FOR DETAILED INFORMATION

ORDER INFORMATION

Part Number	Package
VL82C612-PC	Plastic DIP
VL82C612-QC	Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range is 0°C to +70°C.

GENERAL PURPOSE (SCSI) BUS TRANSCEIVER

FEATURES

- Meets full Small Computer Systems Interface (SCSI) specifications for system cables up to six meters long
- Fully buffered, bidirectional data and control buses
- Interfaces directly to VL53C86 and NCR 5386 family
- Can be used with other interfaces requiring a 48 mA drive
- Low cost
- Two-micron CMOS technology
- Housed in a standard 52-pin PLCC

DESCRIPTION

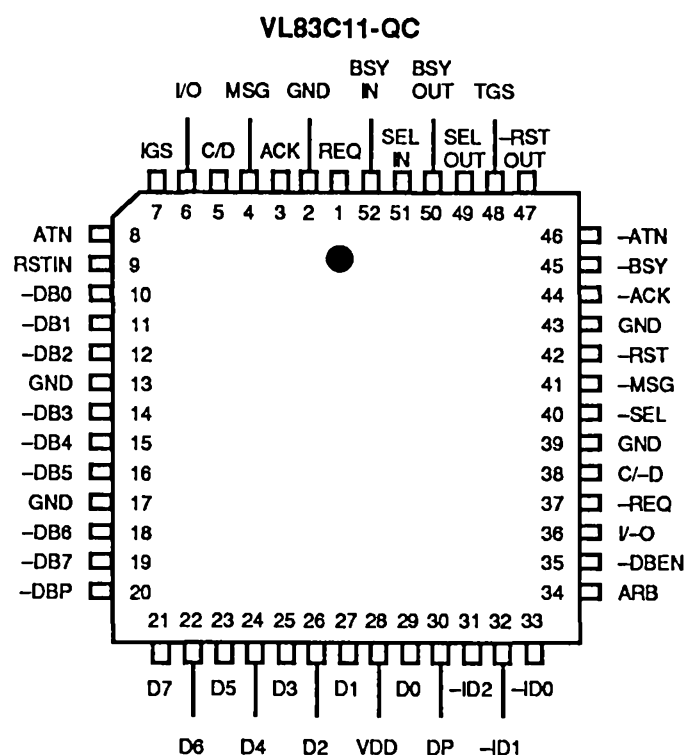
The VL83C11 General Purpose Bus Transceiver Chip, is a two-micron CMOS device designed as a 48 mA bus transceiver chip for all of the Small Computer System Interface (SCSI) bus signals. It incorporates high current single-ended drivers for the SCSI bus. The VL83C11 is specifically intended to be used with the VL53C86 or NCR 53C86 SCSI Protocol Controller families. It interfaces directly to those devices, with no additional circuits required. It can be used with other interfaces where a general purpose 48 mA bus transceiver is required. Logical and electrical flexibility also allow its use

as a general purpose interface driver/receiver chip.

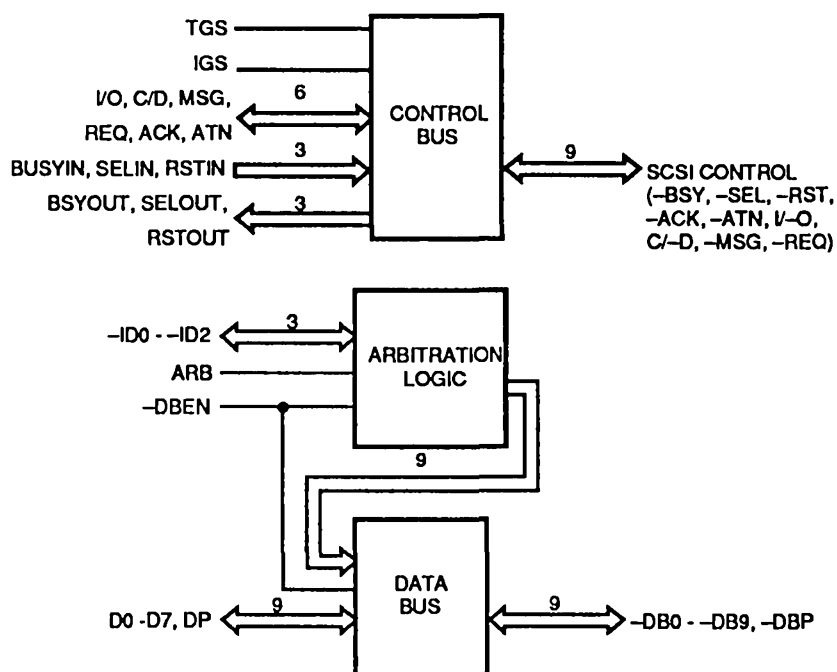
The VL83C11 is functionally equivalent to the NMOS NCR 8310, but has been designed in CMOS technology. It meets the full electrical specifications of Small Computer Systems Interface (SCSI) for system cable lengths up to six meters long. Further, it has been optimized for connection to the standard SCSI connector.

The VL83C11 General Purpose Transceiver Chip is packaged in a 52-pin plastic leaded chip carrier (PLCC).

PIN DIAGRAM



BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Package
VL83C11-QC	Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range is 0°C to +70°C

SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Description
-DB0 - -DB7, -DBP	10-12, 14-16, 18-20	These nine bits (-DB0 through -DB7, -DBP) are bidirectional, active low, open-drain signals that form the data bus. -DB7 is the most significant bit and has the highest priority during Arbitration phase. Data parity is odd. Parity is not valid during arbitration.
-RST	42	Reset - Indicates a SCSI bus reset condition. An "or-tied" signal. This signal is bidirectional, active low and open-drain.
-ATN	46	Attention - Driven by an initiator, -ATN indicates an attention condition. This bidirectional, active low and open-drain signal is received in the target role.
-ACK	44	Acknowledge - Driven by an initiator, -ACK indicates an acknowledgment for a REQ/ACK data transfer handshake. In the target role, -ACK is received as a response to the -REQ signal. It is a bidirectional, active low, open-drain signal.
-REQ	37	Request - Driven by a target, -REQ indicates a request for a REQ/ACK data transfer handshake. This signal is received by the initiator. It is a bidirectional, active low, open-drain signal.
-MSG	41	Message - Driven by the target during the Message phase. This bidirectional, active low, open-drain signal is received by the initiator.
I/-O	36	Input/Output - This bidirectional, open-drain signal is driven by a target which controls the direction of data movement on the SCSI bus. High indicates input to the initiator. This signal is also used to distinguish between Selection and Reselection phases.
C/-D	38	Control or Data - This bidirectional, open-drain signal is driven by the target. It indicates whether Control or Data is on the data bus. High indicates Control. This signal is received by the initiator.
-SEL	40	Select - Used by an initiator to select a target or by a target to reselect an initiator. It is a bidirectional, active low, open-drain signal.
-BSY	45	Busy - Indicates the SCSI bus is being used and can be driven by both the initiator and the target device. An "or-tied" signal. This is a bidirectional, active low, open-drain signal.
D0, D1-D7, DP	29, 27- 21, 30	These nine bits (D0 through D7, DP) form the data bus. D7 is the most significant bit and has the highest priority during Arbitration phase. DP is the parity bit.
-DBEN	35	Data Bus Enable - This signal enables the SCSI bus drivers for -DB7 through -DBP.
TGS	48	Target Group Select - Enables the SCSI bus drivers for I/-O, C/-D, -MSG, and -REQ.
IGS	7	Initiator Group Select - Enables the SCSI bus drivers for -ACK and -ATN.
ARB	34	Arbitration - Enables decode of ID0 - ID2 and asserts priority decode as SCSI data bus ID.
-ID0-2	33-31	Identification - The ID signals are used during arbitration to select the correct DBx line.
I/O	6	Input/Output - This line is used to drive or receive the SCSI signal I/-O.
C/D	5	Control/Data - This line is used to drive or receive the SCSI signal C/-D.
MSG	4	Message - This line is used to drive or receive the SCSI signal -MSG.
REQ	1	Request - This line is used to drive or receive the SCSI signal -REQ.
ACK	3	Acknowledge - This line controls the SCSI signal -ACK.
ATN	8	Attention - This line controls the SCSI signal -ATN.
BSYIN	52	Busy - This line indicates the received state of the SCSI signal -BSY.
BSYOUT	50	Busy - This line drives the SCSI signal -BSY.
SELIN	51	Select - This line indicates the received state of the SCSI signal -SEL.

SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Description
SEOUT	49	Select - This line drives the SCSI signal –SEL.
RSTIN	9	Reset - This line indicates the received state of the SCSI signal –RST.
–RSTOUT	47	Reset - This line drives the SCSI signal –RST.
VDD	28	+5 V
GND	2, 13, 17, 39, 43	Ground

FUNCTIONAL DESCRIPTION

The VL83C11 General Purpose Transceiver has been designed primarily a buffer whose purpose is to translate signals from a microprocessor data bus to the low impedance, terminated, 48 mA, single ended, environment of the SCSI bus.

There is also an arbitration scheme, consistent with SCSI requirements, implemented in this device's logic.

LOGICAL OPERATION

Bus Operation - Data bus direction is usually controlled with a single line –DBEN (pin 35). With –DBEN active (low voltage level), data flow is from Dx to DBx or onto the SCSI data bus.

Arbitration - Arbitration allows one SCSI device to gain control of the SCSI bus so that it can assume a role as Initiator or Target. Arbitration is a system option, but if not implemented, there can be only one Initiator.

The SCSI ID bit is a single bit on the data bus which corresponds to the SCSI device's unique SCSI Address. All other seven data bus bits are released by the SCSI device. During arbitration, parity is not guaranteed, but may not be driven to the false state.

During arbitration with the VL83C11, –DBEN is normally inactive and ARB is driven active (high voltage level).

Under those circumstances, –DBP will be high as will all other –DBx lines except for the one showing a decode of the –ID2 - –ID0 lines.

Target Group Select (TGS) - When the TGS line is driven active (high voltage level), the driving device is controlling in the Target role. The purpose is to enable the VL83C11 SCSI drivers for signals I/O, C/D, –MSG, and –REQ.

Initiator Group Select (IGS) - When at a high voltage level, the IGS line enables the SCSI bus drives for –ATN and –ACK that the driver is in the Initiator role. In the low voltage state, –ATN and –ACK will be received by the Initiator.

APPLICATIONS

Driving Circuitry

The VL83C11 can be driven with either 7400 TTL, LS or Schottky or a MOS microprocessor.

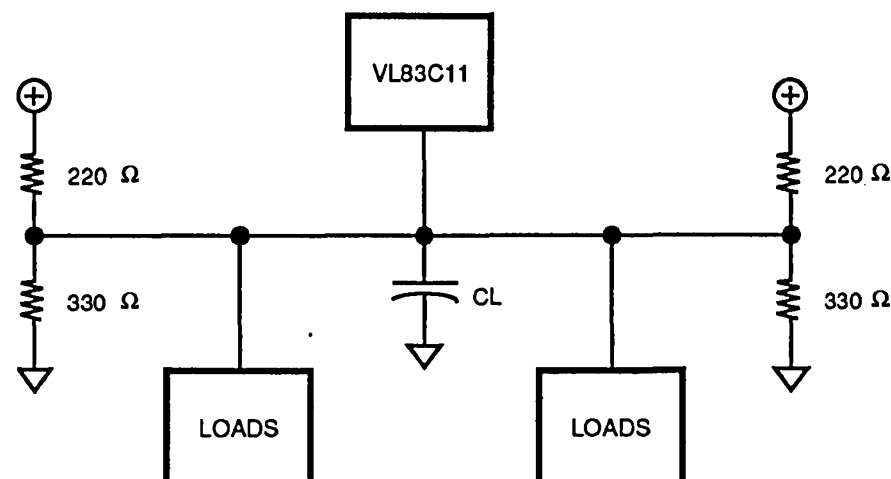
A typical driver/load implementation is represented in Figure 2, TTL Drive of the VL83C11.

Output Loading

Output loading of the VL83C11 is prescribed in ANSI document X3T9.2, SCSI, Small Computer Systems Interface, Section 4, Physical level. An example of a typical bus loading is shown in Figure 1, Illustration of SCSI Bus Loading. Note that the resistive

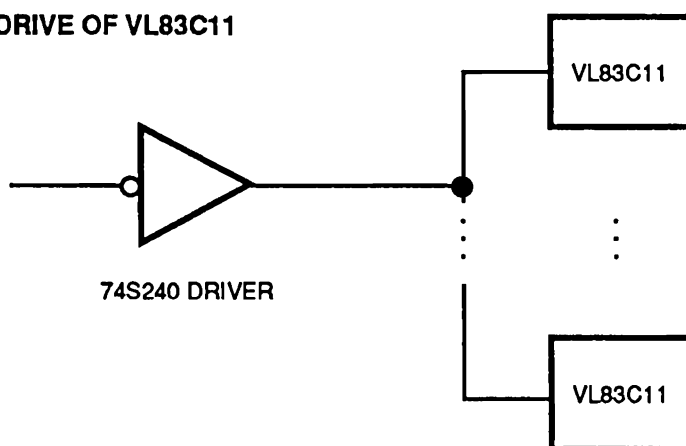
loading element is clearly specified regarding terminating resistors. In contrast, the capacitive/inductive loads imposed as a result of cabling, connectors, or printed circuitry traces can only be estimated when the application has been defined. External loading must be considered when evaluating the AC characteristics.

FIGURE 1: ILLUSTRATION OF SCSI BUS LOADING



Note: SCSI bus may be loaded per ANSI X3T9.2, Section 4.

FIGURE 2. TTL DRIVE OF VL83C11



Note: 74S240 easily drives eight VL83C11 driver chips.

AC CHARACTERISTICS: $T_A = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$, $V_{CC} = 5\text{ V} \pm 5\%$

PROPAGATION DELAY

Propagation Delay Reference defines measurement points used in determination of delay times. Since there is no internal clock in the VL83C11 Driver/

Receiver chip, measurements are to be made relative to other signals defined as references.

CHIP TIMING

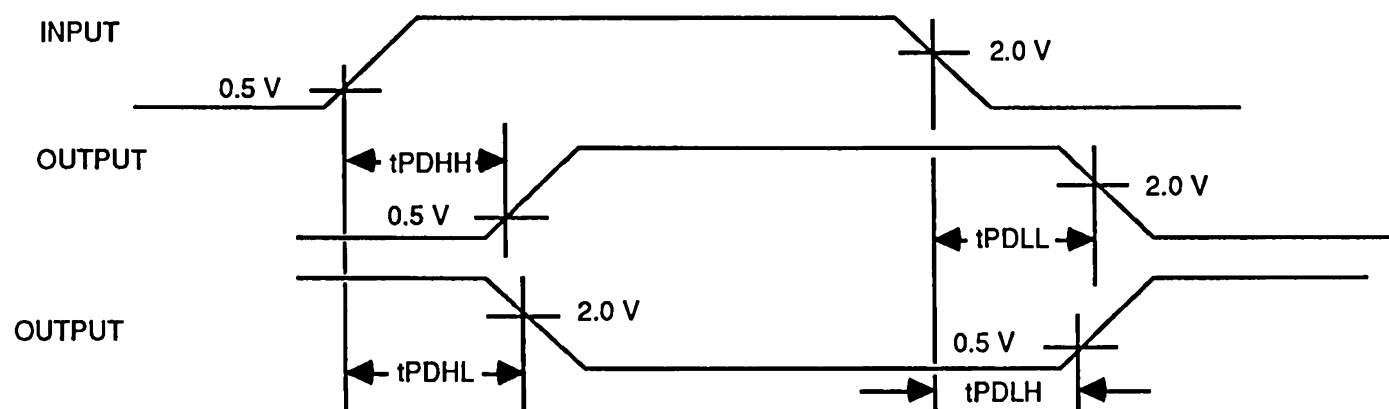
The VL83C11 Driver/Receiver chip

conforms to propagation delays illustrated in Data Bus and Control Signal Turnaround, as well as Control Signal and Arbitration Delay Times.

PROPAGATION DELAY REFERENCE

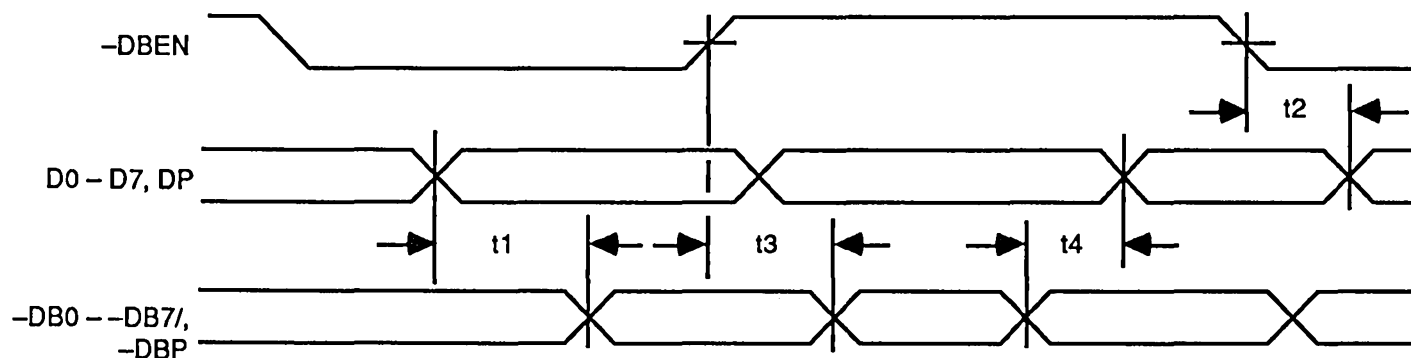
Symbol	Parameter	Min	Max	Unit	Condition
tPDHH				ns	No Internal Clock
tPDLL				ns	No Internal Clock
tPDHL				ns	No Internal Clock

PROPAGATION DELAY REFERENCE TIMING

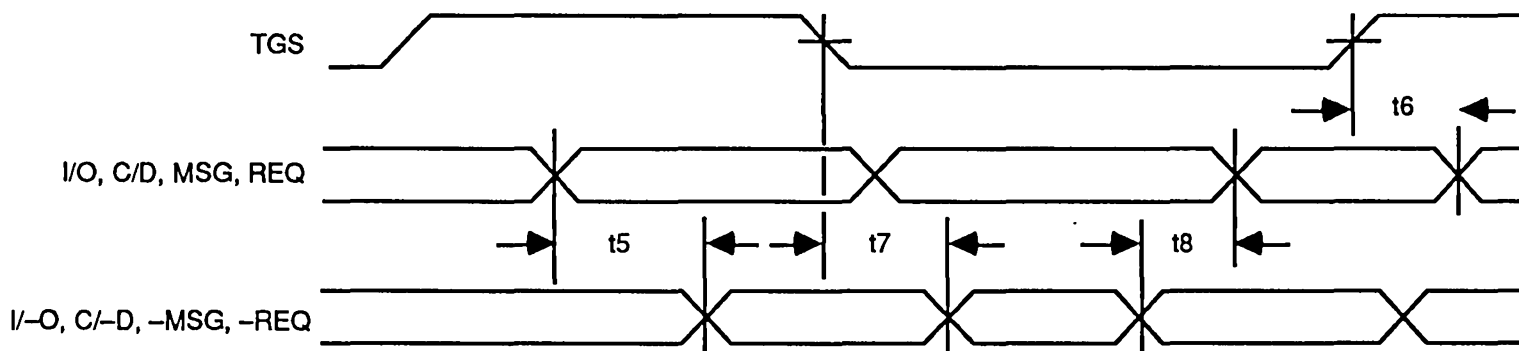


DATA BUS PROPAGATION

Symbol	Parameter	Min	Max	Unit	Condition
t1	Data Bus to SCSI Bus Delay		90	ns	
t2	SBEN True to Data Bus Three-State		90	ns	
t3	SBEN False to SCSI Bus Release		100	ns	
t4	SCSI Bus to Data Bus Delay		60	ns	

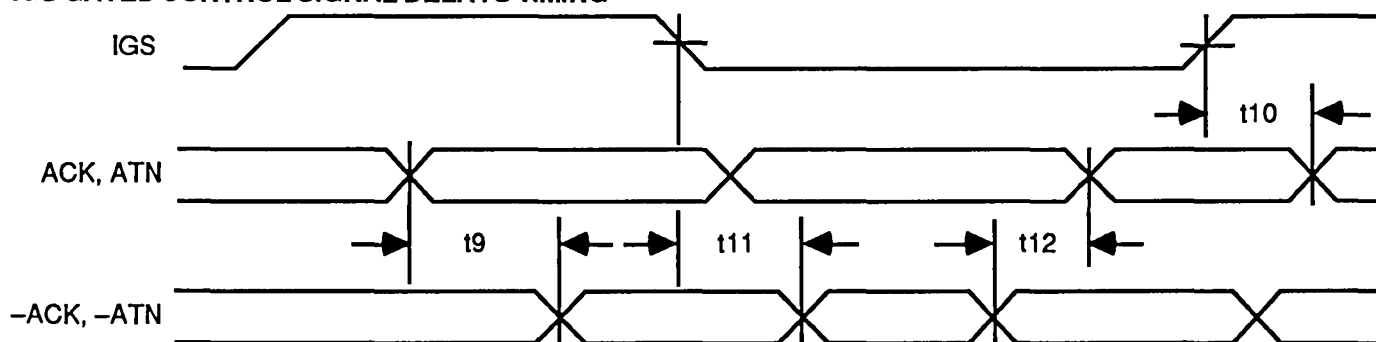
DATA BUS PROPAGATION TIMING

TGS GATED CONTROL SIGNAL DELAYS

Symbol	Parameter	Min	Max	Unit	Condition
t5	Control Signal Delay to SCSI Bus		70	ns	
t6	TGS True to Input Release		50	ns	
t7	TGS False to SCSI Bus Release		70	ns	
t8	SCSI Bus Receiver Delay		50	ns	

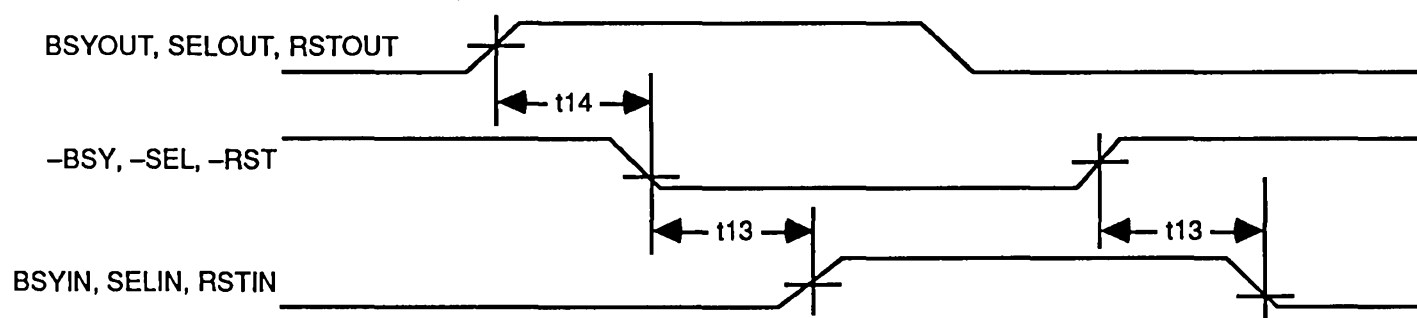
TGS GATED CONTROL SIGNAL DELAYS TIMING


IGS GATED CONTROL SIGNAL DELAYS

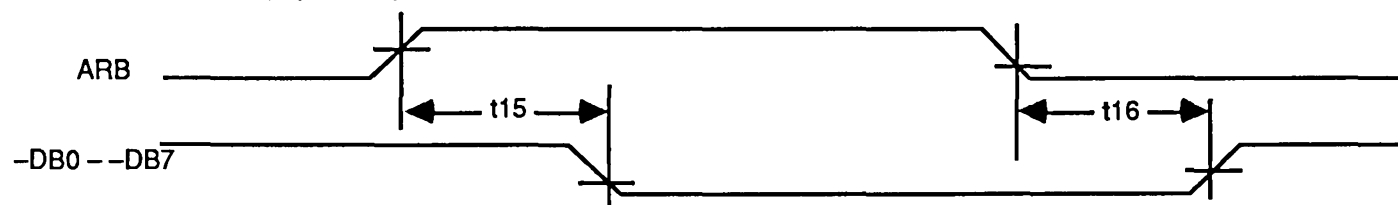
Symbol	Parameter	Min	Max	Unit	Condition
t9	Control Signal Delay to SCSI Bus		70	ns	
t10	IGS True to Input Release		50	ns	
t11	IGS False to SCSI Bus Release		70	ns	
t12	SCSI Bus Receiver Delay		50	ns	

IGS GATED CONTROL SIGNAL DELAYS TIMING

CONTROL SIGNAL TURNAROUND

Symbol	Parameter	Min	Max	Unit	Condition
t13	Receiver Delay BSY RST SEL		50	ns	
t14	Driver Delay BSY RST SEL		70	ns	

CONTROL SIGNAL TURNAROUND TIMING

ARBITRATION DELAY

Symbol	Parameter	Min	Max	Unit	Condition
t15	ARB True to -DB0-7 True		70	ns	
t16	ARB False to -DB0-7 False		70	ns	

ARBRITRATION DELAY TIMING


ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature 0°C to +70°C
 Storage Temperature -65°C to +150°C
 Supply Voltage to Ground Potential -0.5 V to +6.0 V
 Applied Input Voltage -0.5 V to VCC + 0.5 V
 Power Dissipation 800 mW

Stresses above those listed may cause permanent damage to the device. These are stress ratings only, functional operation of this device at these or any other conditions above those indicated

in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS: TA = 0°C to +70°C, VCC = 5 V ± 5%

Symbol	Parameter	Min	Max	Units	Conditions
VCC	Positive Supply Voltage	4.75	5.25	V	
ICC	Operating Current		2.0	mA	All Inputs = VIL = 0.8
VIH	High Level Input Voltage	2.0	5.25	V	
VIL	Low Level Input Voltage	-0.3	0.8	V	
IiH	High Level Input Current (SCSI)		50	μA	VIH = 5.25
IiL	Low Level Input Current (SCSI)		-50	μA	VIL = 0
IIL	Low Level Input Current (DP)		-2	mA	VIL = 0
IiH	High Level Input Current (All Other Pins)		10	μA	VIH = 5.25
IiL	Low Level Input Current (All Other Pins)		-10	μA	VIL = 0
VOH	High Level Output Voltage	2.5	5.25	V	VCC = 4.75 V, IOH = 7.0 mA
VOL	Low Level Output Voltage	0	0.4	V	VCC = 4.75 V, IOL = 7.0 mA
VOL	Low Level Output Voltage (SCSI)	0	0.5	V	VCC = 4.75 V, IOL = 48.0 mA

SERIAL COMMUNICATIONS CONTROLLER (SCC)

FEATURES

- Two independent full-duplex channels
- 0 to 1.5M bit/second
- Multi-protocol operation for NRZ, NRZI, or FM
- Asynchronous mode includes 1, 1.5, or 2 stop bits per character
- Programmable clock factor
- Break generation and error detection
- Intelligent SDLC/HDLC
- Local loopback and auto echo modes
- Synchronous support includes internal or external character synchronization

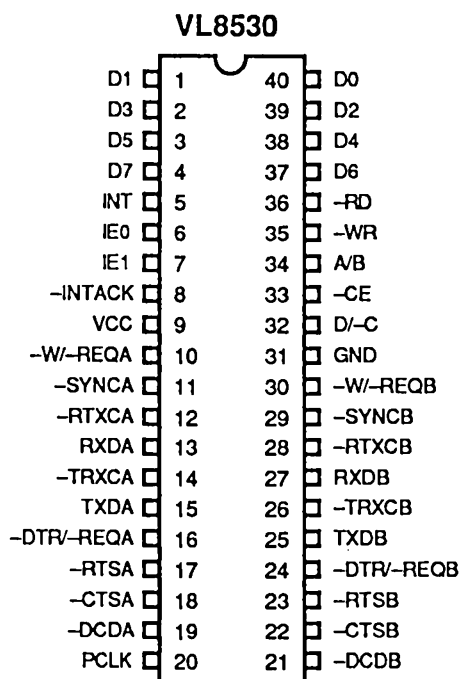
DESCRIPTION

The VL8530 Serial Communications Controller (SCC) is a dual-channel, multi-protocol data communications peripheral designed for use with conventional non-multiplexed buses. The SCC can be software configured to satisfy a wide variety of serial communications applications. The device contains a variety of new, sophisticated internal functions, including on-chip baud rate generators, digital phase-locked loops, and crystal oscillators that dramatically reduce the need for external logic.

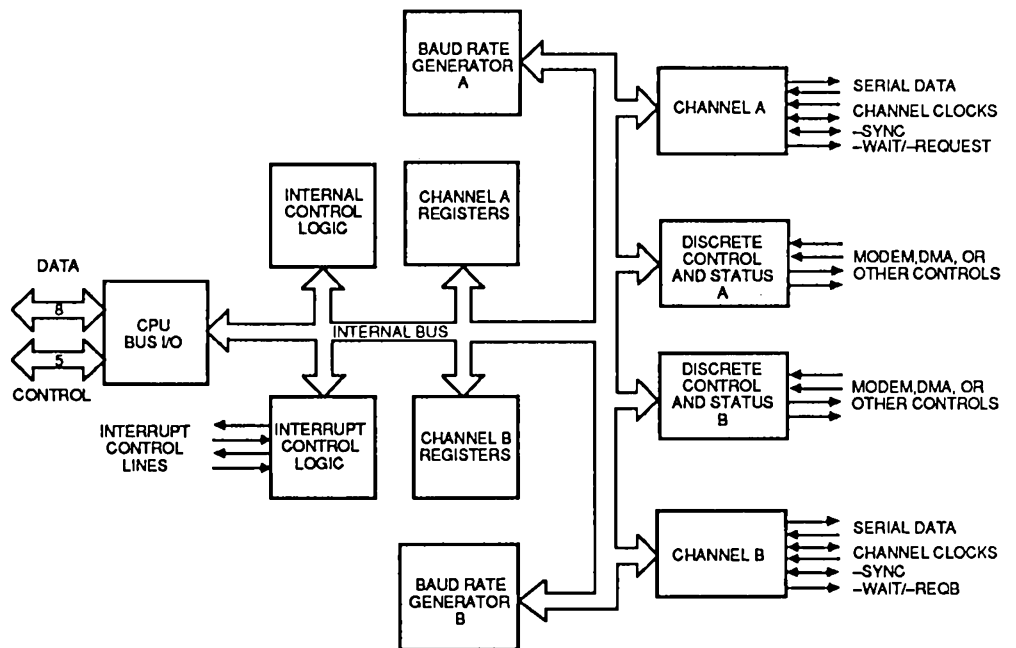
The SCC handles asynchronous formats, synchronous byte-oriented protocols, such as IBM Bisync, and synchronous bit-oriented protocols, such as HDLC and IBM SDLC. This versatile device supports virtually any serial data transfer application (cassette, diskette, tape drives, etc.).

The device can generate and check CRC codes in any synchronous mode and can be programmed to check data integrity in various modes. The SCC also has facilities for modem controls in both channels.

PIN DIAGRAM



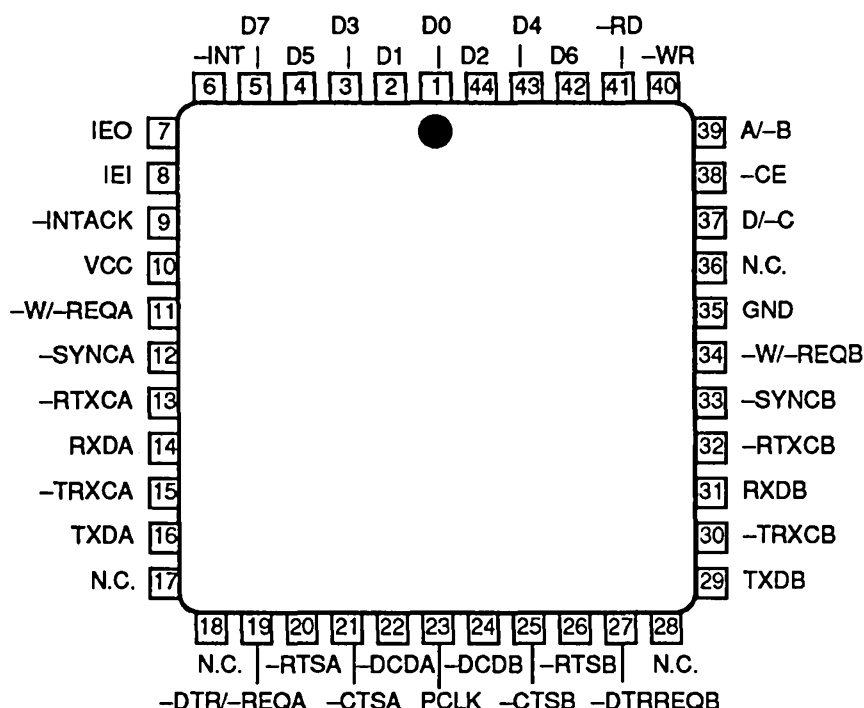
BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Clock Frequency	Package
VL8530-04PC	4 MHz	Plastic DIP
VL8530-04CC		Ceramic DIP
VL8530-04QC		Plastic Leaded Chip Carrier (PLCC)
VL8530-06PC	6 MHz	Plastic DIP
VL8530-06CC		Ceramic DIP
VL8530-06QC		Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range is 0° to +70°C.

PIN DIAGRAM

SIGNAL DESCRIPTIONS

Signal Name	DIP Pin Number	Signal Description
A/-B	34	Channel A/Channel B Select - This input signal selects the channel on which the read or write operation occurs.
-CE	33	Chip Enable - This active low input signal selects the SCC for a read or write operation.
-CTSA, -CTSB	18, 22	Clear To Send - Active low inputs - If these pins are programmed as auto enables, a low on the inputs enables the respective transmitters. If not programmed as auto enables, they may be used as general-purpose inputs. Both inputs are Schmitt trigger buffered to accommodate slow rise time inputs. The SCC detects pulses on these inputs and can interrupt the CPU on both logic level transitions.
D/-C	32	Data/Control Select - This input signal defines the type of information transferred to or from the SCC. A high means data is transferred; a low indicates a command.
-DCDA, -DCDB	19 21	Data Carrier Detect - Active low inputs - These pins function as receiver enables if they are programmed for auto enables; otherwise, they may be used as general-purpose input pins. Both pins are Schmitt trigger buffered to accommodate slow rise time signals. The SCC detects pulses on these pins and can interrupt the CPU on both logic level transitions.
D0-D7	40,1,39,2,38, 3,37,4	Data Bus - These bidirectional, three-state lines carry data and commands to and from the SCC.
-DTR/-REQA -DTR/-REQB	16, 24	Data Terminal Ready/Request - These active low outputs follow the state programmed into the -DTR bit. They can also be used as general-purpose outputs or as request lines for a direct memory access (DMA) controller.
IEI	7	Interrupt Enable In - Active high output - IEI is used with IEO to form an interrupt daisy chain when there is more than one interrupt-driven device. A high IEI indicates that no other higher priority device has an interrupt underservice or is requesting an interrupt.
IEO	6	Interrupt Enable Out - Active high output - IEO is high only if IEI is high and the CPU is not servicing an SCC interrupt or the SCC is not requesting an interrupt (Interrupt Acknowledge cycle only). IEO is connected to the next lower priority device's IEI input and thus inhibits interrupts from lower priority devices.
-INT	5	Interrupt Request - Active low open-drain output - This signal is activated when the SCC requests an interrupt.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	DIP Pin Number	Signal Description
-INTACK	8	Interrupt Acknowledge - Active low input - This signal indicates an active Interrupt Acknowledge cycle. During this cycle, the SCC interrupt daisy chain settles. When -RD becomes active, the SCC places an interrupt vector on the data bus (if IEI is high). The -INTACK signal is latched by the rising edge of PCLK.
PCLK	20	Clock - This input is the master SCC clock used to synchronize internal signals. PCLK is a TTL level signal.
-RD	36	Read - Active low input - This signal indicates a read operation and, when the SCC is selected, enables the SCC's bus drivers. During the Interrupt Acknowledge cycle, this signal gates the interrupt vector onto the bus if the SCC is the highest priority device requesting an interrupt.
RXDA, RXDB	13, 27	Receive Data - Active high inputs - These input signals receive serial data at standard TTL levels.
-RTXCA, -RTXCB	12, 28	Receive/Transmit Clocks - Active low inputs - These pins can be programmed in several different modes of operation. In each channel, -RTXC may supply the receive clock, the transmit clock, the clock for the baud rate generator, or the clock for the digital phase locked loop. These pins can also be programmed for use with the respective -SYNC pins as a crystal oscillator. The receive clock may be 1, 16, 32, or 64 times the data rate in asynchronous modes.
-RTSA, -RTSB	17, 23	Request To Send - Active low outputs - When the -RTS bit in write register 5 (figure 7) is set, the -RTS signal goes low. When the -RTS bit is reset in the asynchronous mode and auto enable is on, the signal goes high after the transmitter is empty. In synchronous mode or in asynchronous mode with auto enable off, the -RTS pin strictly follows the state of the -RTS bit. Both pins can be used as general purpose outputs.
-SYNCA, -SYNCB	11, 29	Synchronization - Active low inputs or outputs - These pins can act either as inputs or outputs, or part of the crystal oscillator circuit. In the asynchronous receive mode (crystal oscillator option not selected), these pins are inputs similar to -CTS and -DCD. In this mode, transitions on these lines affect the state of the synchronous/hunt status bits in read register 0 (Figure 6) but have no other function. In external synchronization mode with the crystal oscillator not selected, these lines also act as inputs. In this mode, -SYNC must be driven low to receive clock cycles after the last bit in the synchronous character is received. Character assembly begins on the rising edge of the receive clock immediately preceding the activation of -SYNC. In the internal synchronization mode (Monosync and Bisync) with the crystal oscillator not selected, these pins act as outputs and are active only during the part of the receive clock cycle in which synchronous characters are recognized. The synchronous condition is not latched, so these outputs are active each time a synchronization pattern is recognized (regardless of character boundaries). In SDLC mode, these pins act as outputs and are valid on receipt of a flag.
TXDA, TXDB	15, 25	Transmit Data - Active high outputs - These output signals transmit serial data at standard TTL levels.
-TRXCA, -TRXCB	14, 26	Transmit/Receive Clocks - Active low inputs or outputs - These pins can be programmed in several different modes of operation. -TRXC may supply the receive clock or the transmit clock in the input mode or supply the output of the digital phase-locked loop, the crystal oscillator, the baud rate generator, or the transmit clock in the output mode.
-WR	35	Write - Active low input - When the SCC is selected, this signal indicates a write operation. The coincidence of -RD and -WR is interpreted as a reset.
-W/-REQA, -W/-REQB	10, 30	Wait/Request - Open-drain outputs when programmed for a wait function, driven high or low when programmed for a Request function - These dual-purpose outputs may be programmed as Request lines for a DMA controller or as Wait lines to synchronize the CPU to the SCC data rate. The reset state is Wait.

FUNCTIONAL DESCRIPTION

The functional capabilities of the SCC can be described from two different points of view. As a data communications device, it transmits and receives data in a wide variety of data communications protocols. As a microprocessor peripheral, the SCC offers valuable features as vectored interrupts, polling, and simple handshake capability.

DATA COMMUNICATIONS CAPABILITY

The SCC provides two independent full-duplex channels programmable for use in any common asynchronous or synchronous data communication protocol. Figure 1 and the following description briefly detail these protocols.

Asynchronous modes - Transmission and reception can be accomplished independently on each channel with 5 to 8 bits per character, plus optional even or odd parity. The transmitters can supply 1, 1 1/2, or 2 stop bits per character and a break output at any time. The receiver break-detection logic interrupts the CPU both at the start and at the end of a received break.

Reception is protected from spikes by a transient spike-rejection mechanism that checks the signal one-half a bit time after a low level is detected on the receive data input (RXDA or RXDB). If the low does not persist (as in the case of a transient), the character assembly process does not start.

Framing errors and overrun errors are detected and buffered together with the partial character on which they occur. Vectored interrupts allow fast servicing or error conditions using dedicated routines. Furthermore, a built-in checking process avoids the interpretation of a framing error as a new start bit: a framing error results in the addition of one-half a bit time to the point at which the search for the next start bit begins.

The SCC does not require symmetric transmit and receive clock signals a feature allowing use of the wide variety of clock sources. The transmitter and receiver can handle data at a rate of 1, 1/16, 1/32, or 1/64 of the clock rate supplied to the receive and transmit clock inputs. In asynchronous modes,

the -SYNC pin may be programmed as an input used for such functions as monitoring a ring indicator.

Synchronous modes. The SCC supports both byte-oriented and bit-oriented synchronous communication. Synchronous byte-oriented protocols can be handled in several modes, allowing character synchronization with a 6-bit or 8-bit synchronous character (Monosync) any 12-bit synchronization pattern (Bisync), or with an external synchronous signal. Leading sync characters can be removed without interrupting the CPU.

5- or 7-bit synchronous characters are detected with 8- or 16-bit patterns in the SCC by overlapping the larger pattern across multiple incoming synchronous characters.

The CRC checking for synchronous byte-oriented modes is delayed by one character time so that the CPU may disable CRC checking on specific characters. This allows the implementation of IBM Bisync. protocols.

Both CRC-16 ($X^{16} + X^{15} + X^2 + 1$) and CCITT ($X^{16} + X^{12} + X^5 + 1$) error checking polynomials are supported. Either polynomial may be selected in all Synchronous modes. Users may preset the CRC generator and checker to all ones or all zeros. The SCC also provides a feature that automatically transmits CRC data when no other data is available for transmission. This allows for high-speed transmissions under DMA control, with no need for CPU intervention at the end of a message. When there is no data or CRC to send in synchronous modes, the transmitter inserts 6-, 8-, or 16-bit synchronous characters, regardless of the programmed character length.

The SCC supports synchronous bit-oriented protocols, such as SDLC and HDLC, by performing automatic flag sending, zero insertion, and CRC generation. A special command can be used to abort a frame in transmission. At the end of a message, the SCC automatically transmits the CRC and trailing flag when the transmitter underruns. The transmitter may also be

programmed to send an idle line consisting of continuous flag characters or a steady marking condition.

If a transmit underrun occurs in the middle of a message, an external/status interrupt warns the CPU of this status change so that an abort may be issued. The SCC may also be programmed to send an abort itself in case of an underrun, relieving the CPU of this task. One to eight bits per character can be sent, allowing reception of a message with no prior information about the character structure in the information field of a frame.

The receiver automatically acquires synchronization on the leading flag of a frame in SDLC or HDLC and provides a synchronization signal on the -SYNC pin (an interrupt can also be programmed). The receiver can be programmed to search for frames addressed by a single byte (or four bits within a byte) of a user-selected address or to a global broadcast address. In this mode, frames not matching either the user-selected or broadcast address are ignored. The number of address bytes can be extended under software control. For receiving data, an interrupt on the first received character, or an interrupt on every character, or on special condition only (end-of-frame) can be selected. The receiver automatically deletes all zeros inserted by the transmitter during character assembly. The CRC is also calculated and is automatically checked to validate frame transmission. At the end of transmission, the status of a received frame is available in the status registers. In SDLC mode, the SCC must be programmed to use the SDLC CRC polynomial, but the generator and checker may be preset to all ones or all zeros.

The CRC is inverted before transmission and the receiver checks against the bit pattern 0001110100001111.

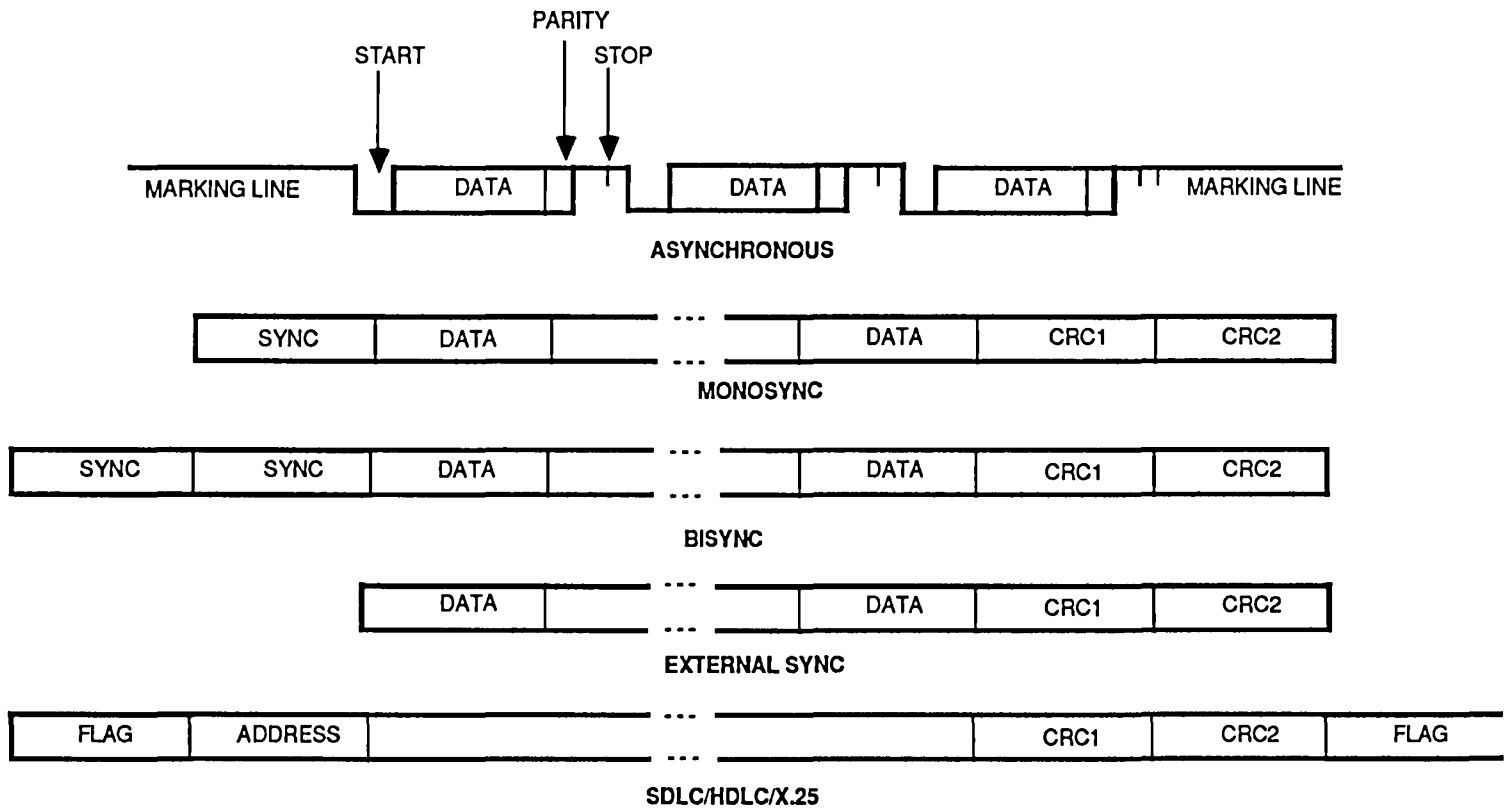
The NRZ, NRZI, or FM coding may be used in any 1x mode. The parity options available in asynchronous modes are available in synchronous modes.

The SCC can be conveniently used under DMA control to provide high-speed reception or transmission. In reception, for example, the SCC can

interrupt the CPU when the first character of a message is received. The CPU then enables the DMA to

transfer the message to memory. The SCC then issues an end-of-frame interrupt and the CPU can check the status of the received message.

FIGURE 1. SCC PROTOCOLS



The CPU is thereby freed for other service while the message is being received. The CPU may also enable the DMA first and have the SCC interrupt only on end-of-frame. This procedure allows all data to be transferred via the DMA.

SDLC LOOP MODE

The SCC supports SDLC loop mode in addition to normal SDLC. In an SDLC loop, there is a primary controller station that manages the message traffic flow on the loop and any number of secondary stations. In SDLC loop mode, the SCC performs the functions of a secondary station while an SCC operating in regular SDLC mode can act as a controller (Figure 3).

A secondary station in an SDLC Loop is always listening to the messages being sent around the loop, and in fact must pass these messages to the rest of the loop by retransmitting them with a one-bit time delay. The secondary station can place its own message on the loop only at specific times. The controller signals that secondary stations may transmit messages by sending a special character, called an End Of Poll (EOP), around the loop. The EOP character is the bit pattern 11111110. Because of zero insertion during messages, this bit pattern is unique and easily recognized.

When a secondary station has a message to transmit and recognizes an EOP on the line, it changes the last binary 1 of the EOP to a 0 before transmission. This has the effect of turning the EOP into a flag sequence. The secondary station now places its message on the loop and terminates the message with an EOP. Any secondary stations, further down the loop with messages to transmit, can then append their messages to the message of the first secondary station without messages to send. The following stations merely echo the incoming messages and are prohibited from placing messages on the loop (except upon recognizing an EOP). The SDLC loop mode is a programmable option in the SCC; NRZ, NRZI, and FM coding may all be used in SDLC Loop mode.

BAUD RATE GENERATOR

Each channel in the ESCC contains a programmable baud rate generator. Each generator consists of two 8-bit time constant registers that form a 16-bit time-constant, a 16-bit down counter, and a flip-flop on the output producing a square wave. On startup, the flip-flop on the output is set in a HIGH state, the value in the time-constant register is loaded into the counter, and the counter starts counting down. The output of the baud rate generator toggles upon reaching 0, the value in the time-constant register

process is repeated. The time constant may be changed at any time, but the new value does not take effect until the next load of the counter.

The output of the baud rate generator may be used as either the transmit clock, the receive clock, or both. It can also drive the digital phase-locked loop (see next section).

If the receive clock or transmit clock is not programmed to come from the -TRxC pin, the output of the baud rate generator may be echoed out via the -TRxC pin.

The following formula relates the time constant to the baud rate (the baud rate is in bits/second and BR clock period is in seconds):

$$\text{baud rate} = \frac{1}{2 (\text{time constant} + 2) \times (\text{BR clock period})}$$

DIGITAL PHASE-LOCKED LOOP

The ESCC contains a digital phase-locked-loop (DPLL) to recover clock information from a data stream with NRZI or FM encoding. The DPLL is driven by a clock that is nominally 32 (NRZI) or 16 (FM) times the data rate. The DPLL uses this clock, along with the data stream, to construct a clock for the data. This clock may then be used as the SCC receive clock, the transmit clock, or both.

FIGURE 2. DETECTING 5- OR 7-BIT SYNCHRONOUS CHARACTERS

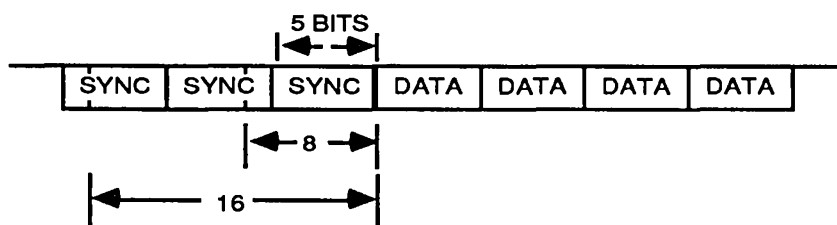
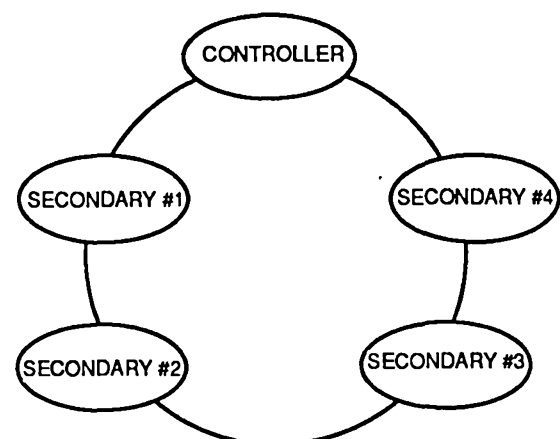


FIGURE 3. AN SDLC LOOP



For NRZI encoding, the DPLL counts the 32x clock to create nominal bit times. As the 32x clock is counted, the DPLL is searching the incoming data stream for edges (either 1 to 0 or 0 to 1). Whenever an edge is de-tected, the DPLL makes a count adjustment (during the next counting cycle), producing a terminal count closer to the center of the bit cell.

For FM encoding, the DPLL still counts from 0 to 31, but with a cycle corresponding to two bit times. When the DPLL is locked, the clock edges in the data stream should occur between counts 15 and 16, and between counts 31 and 0. The DPLL looks for edges only during a time centered on the 15 to 16 counting transition.

The 32x clock for the DPLL can be programmed to come from either the -RTxC input or the output of the baud rate generator. The DPLL output may be programmed to be echoed out of the ESCC via the -TRxC pin (if this pin is not being used as an input).

DATA ENCODING

The ESCC may be programmed to encode and decode the serial data in four different ways (Figure 4). In NRZ encoding, a 1 is represented by a HIGH level and a 0 is represented by a LOW level. In NRZI encoding, a 1 is represented by no change in level and a 0 is represented by a change in level.

In FM1 (more properly, bi-phase mark), a transition occurs at the beginning of every bit cell. A 1 is represented by

an additional transition at the center of the bit cell and a 0 is represented by no additional transition at the center of the bit cell. In FM0 (bi-phase space), a transition occurs at the beginning of every bit cell. A 0 is represented by an additional transition at the center of the bit cell, and a 1 is represented by no additional transition at the center of the bit cell.

In addition to these four methods, the ESCC can be used to decode Manchester (bi-phase level) data by using the DPLL in the FM mode and programming the receiver for NRZ data. Manchester encoding always produces a transition at the center of the bit cell. If the transition is 0 to 1, the bit is a 0. If the transition is 1 to 0, the bit is a 1.

AUTO ECHO AND LOCAL LOOPBACK

The ESCC is capable of automatically echoing everything it receives. This feature is useful mainly in Asynchronous modes, but works in Synchronous and SDLC modes as well. In Auto Echo mode, TxD is RxD. Auto Echo mode can be used with NRZI or FM encoding with no additional delay, because the data stream is not decoded before retransmission. In Auto Echo mode, the -CTS input is ignored as a transmitter enable (although transitions on this input can still cause interrupts if programmed to do so). In this mode, the transmitter is actually bypassed and the programmer is responsible for disabling transmitter interrupts and Wait/Request on transmit.

The ESCC is also capable of local loopback. In this mode TxD is RxD, just as in auto echo mode. However, in local loopback mode, the internal transmit data is tied to the internal receive data and RxD is ignored (except to be echoed out via TxD). The -CTS and -DCD inputs are also ignored as transmit and receive enables. However, transitions on these inputs can still cause interrupts. Local loopback works in asynchronous, synchronous, and SDLC modes with NRZ, NRZI, or FM coding of the data stream.

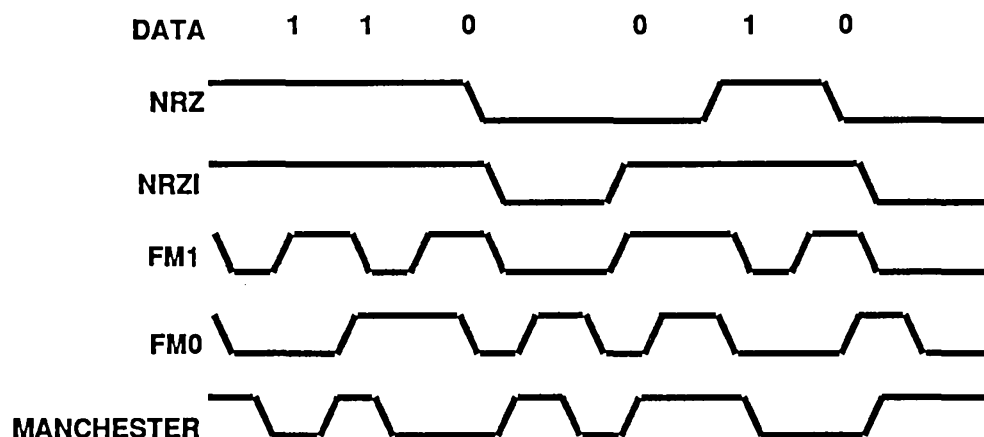
I/O INTERFACE CAPABILITIES

The ESCC offers the choice of polling, interrupt (vectored or nonvectored), and block transfer modes to transfer data, status, and control information to and from the CPU. The block transfer mode can be implemented under CPU or DMA control.

POLLING

All interrupts are disabled. Three status registers in the ESCC are automatically updated whenever any function is performed. For example, end-of-frame in SDLC mode sets a bit in one of these status registers. The idea behind polling is for the CPU to periodically read a status register until the register contents indicate the need for data to be transferred. Only one register needs to be read; depending on its contents, the CPU either writes data, reads data, or continues. Two bits in the register indicate the need for data transfer.

FIGURE 4. DATA ENCODING METHODS





An alternative is a poll of the Interrupt Pending register to determine the source of an interrupt. The status for both channels resides in one register.

INTERRUPTS

When an SCC responds to an Interrupt Acknowledge signal (-INTACK) from the CPU, an interrupt vector may be placed on the data bus. This vector is written in Write Register 2 (WR2) and may be read in Read Register 2A (RR2A) or Read Register 2B (RR2B) (Figures 8).

To speed interrupt response time, the SCC can modify three bits in this vector to indicate status. If the vector is read in Channel A, status is never included; if it is read in Channel B, status is always included.

Each of the six sources of interrupts in the SCC (Transmit, Receive, and External/Status interrupts in both channels) has three bits associated with the interrupt source: Interrupt Pending (IP), Interrupt Under Service (IUS), and Interrupt Enable (IE). Operation of the IE bit is straightforward. If the IE bit is set for a given interrupt source, that source can request interrupts. The exception is when the MIE (Master Interrupt Enable) bit in WR9 is reset and no interrupts may be requested. The IE bits are write only.

The other two bits are related to the interrupt priority chain (Figure 5). As a microprocessor peripheral, the SCC may request an interrupt only when no higher priority device is requesting one; e.g., when IEI is high. If the device in question requests an interrupt, it pulls

down -INT . The CPU then responds with -INTACK , and the interrupting device places the vector on the data bus.

In the SCC, the IP bit signals a need for interrupt servicing. When an IP bit is 1 and the IEI input is high, the INT output is pulled low, requesting an interrupt. In the SCC, if the IE bit is not set by enabling interrupts, then the IP for that source can never be set. The IP bits are readable in RR3A.

The IUS bits signal that an interrupt request is being serviced. If an IUS is set, all interrupt sources of lower priority in the SCC and external to the SCC are prevented from requesting interrupts. The internal interrupt sources are inhibited by the state of the internal daisy chain, while lower priority devices are inhibited by the IEO output of the SCC being pulled LOW and propagated to subsequent peripherals.

An IUS bit is set during an interrupt acknowledge cycle if there are no higher priority devices requesting interrupts. There are three types of interrupts: transmit, receive, and external/status. Each interrupt type is enabled under program control with Channel A having higher priority than Channel B, and with receive, transmit, and external/status interrupts prioritized in that order within each channel. When the transmit interrupt is enabled, the CPU is interrupted when the transmit buffer becomes empty. (This implies that the transmitter must have had a data character written into it so that it can become empty.) When enabled, the

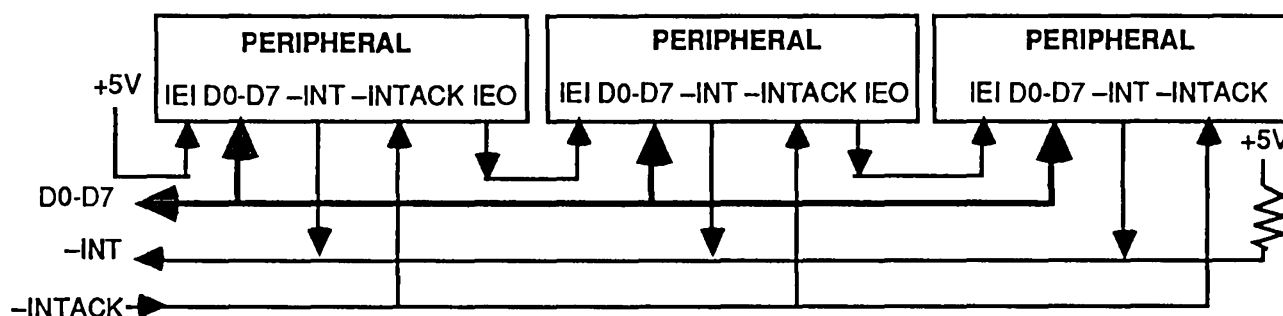
receiver can interrupt the CPU in one of three ways:

- On first receive character or special receive condition
- On all receive characters or special receive condition
- On special receive condition only.

Interrupt on first character or special condition and interrupt on special condition only are typically used with the Block Transfer mode. A special receive condition is one of the following: receiver overrun, framing error in Asynchronous mode, end-of-frame in SDLC mode, and optionally, a parity error. The special receive condition interrupt is different from an ordinary receive character interrupt only in that the status is placed in the vector during the Interrupt Acknowledge cycle. In interrupt on first receive character, an interrupt can occur from special receive conditions any time after the first receive character interrupt.

The main function of the external/status interrupt is to monitor the signal transitions of the -CTS , -CCD , and -SYNC pins; however, an external/status interrupt is also caused by a transmit underrun condition, or a zero count in the baud rate generator, or by the detection of a break (asynchronous mode), abort (SDLC mode) or EOP (SDLC loop mode) sequence in the data stream.

FIGURE 5. INTERRUPT SCHEDULE



The interrupt caused by the abort or EOP has a special feature allowing the SCC to interrupt when the abort or EOP sequence is detected or terminated. This feature facilitates the proper termination of the current message, correct initialization of the next message, and the accurate timing of the Abort condition in external logic in SDLC mode. In SDLC Loop mode, this feature allows secondary stations to recognize the need of the primary station to regain

control of the loop during a poll sequence.

CPU/DMA BLOCK TRANSFER

The SCC provides a Block Transfer mode to accommodate CPU block transfer functions and DMA controllers. The Block Transfer mode uses the Wait/Request output in conjunction with the Wait/Request bits in WR1. The Wait/Request output can be defined under software control as a Wait line in the

CPU Block Transfer mode or as a Request line in the DMA Block Transfer mode.

To a DMA controller, the SCC Request output indicates that the SCC is ready to transfer data to or from memory. To the CPU, the Wait line indicates that the SCC is not ready to transfer data, thereby requesting that the CPU extend the I/O cycle. The DTR/Request line allows full-duplex operation under DMA control.

PROGRAMMING

The SCC contains 13 write registers in each channel that are programmed by the system separately to configure the functional personality of the channels.

In the SCC, register addressing is direct for the data registers only, which are selected by a high on the D/-C pin. In all other cases (with the exception of WR0 and RR0), programming the write registers requires two write operations and reading the read registers requires both a write and a read operation. The first write is to WR0 and contains three bits that point to the selected register. The second write is the actual control word for the selected register, and if the second operation is read, the selected read register is accessed. All of the registers in the SCC, including the data registers, may be accessed in this fashion. The pointer bits are automatically cleared after the read or write operation so that WR0 (or RR0) is addressed again.

The system program first issues a series of commands to initialize the basic mode of operation. This is followed by other commands to qualify conditions within the selected mode. For example, the asynchronous mode, character length, clock rate, number of stop bits, and even or odd parity might be set first. Then the interrupt mode would be set, and, finally, receiver or transmitter enable.

READ REGISTERS

The SCC contains ten read registers (eleven counting receive buffer RR8) in each channel. Four of these may be read to obtain status information (RR0, RR1, RR10, and RR15). Two registers (RR12 and RR13) may be read to learn the baud rate generator time constant. The RR2 contains either the unmodified interrupt vector (Channel A) or the vector modified by status information (Channel B). Both RR7 and RR6 read the DMA FIFO. The RR3 contains the Interrupt Pending (IP) bits (Channel A).

Figures 6 through 13 and Figure 31 show the formats for each read register.

The status bits of RR0 and RR1 are carefully grouped to simplify status monitoring; e.g., when the interrupt vector indicates a special receive condition interrupt, all the appropriate error bits can be read from a single register (RR1).

WRITE REGISTERS

The SCC contains 13 write registers (14 counting WR8, the transmit buffer) in each channel. These write registers are programmed separately to configure the functional personality of the channels. In addition, there are two registers (WR2 and WR9) shared by the two channels that may be accessed through either of them; WR2 contains the interrupt vector for both channels, while WR9 contains the interrupt control bits. Figures 14 through 28 and Figure 31 show the format of each write register.

TIMING

The SCC generates internal control signals from -WR and -RD that are related to PCLK. Since PCLK has no phase relationship with -WR and -RD, the circuitry generating these internal control signals must provide time for metastable conditions to disappear. This gives rise to a recovery time related to PCLK. The recovery time applies only between bus transactions involving the SCC. The recovery time required for proper operation is specified from the rising edge of -WR or -RD in the first transaction involving the SCC, to the falling edge of WR or RD in the second transaction involving the SCC. This time

must be at least four PCLK cycles plus 200 ns.

READ CYCLE TIMING

Figure 32 illustrates Read cycle timing. Addresses on A/-B and D/-C and the status on -INTACK must remain stable through the cycle. If -CE falls after -RD falls or if it rises before -RD rises, the effective -RD is shortened.

WRITE CYCLE TIMING

Figure 33 illustrates Write cycle timing. Addresses on A/-B and D/-C and the status on -INTACK must remain stable throughout the cycle. If -CE falls after -WR falls, or if it rises before -WR rises, the effective -WR is shortened.

INTERRUPT ACKNOWLEDGE CYCLE TIMING

Figure 34 illustrates Interrupt Acknowledge cycle timing. Between the time -INTACK goes low and the falling edge of -RD, the internal and external IEI/IEO daisy chains settle. If there is an interrupt pending in the SCC and IEI is high when -RD falls, the Acknowledge cycle is intended for the SCC. In this case, the SCC may be programmed to respond to -RD low by placing its interrupt vector on D0-D7 and it then internally sets the appropriate Interrupt-Under-Service latch.

FIGURE 6. READ REGISTER 0

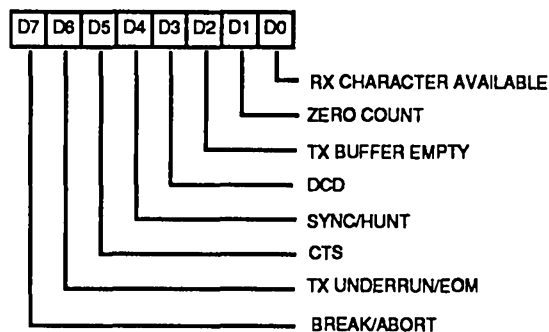


FIGURE 10. READ REGISTER 10

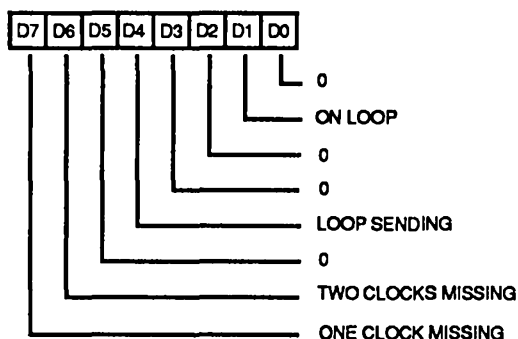


FIGURE 7. READ REGISTER 1

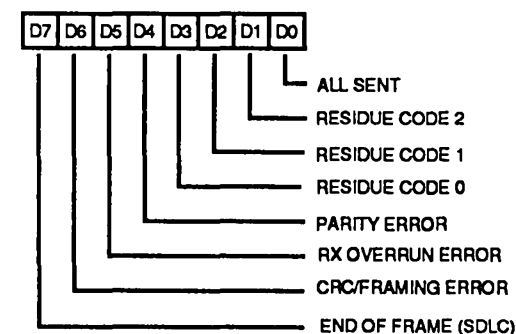


FIGURE 11. READ REGISTER 12

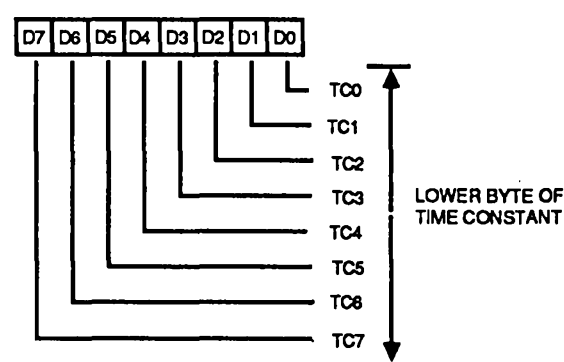


FIGURE 8. READ REGISTER 2

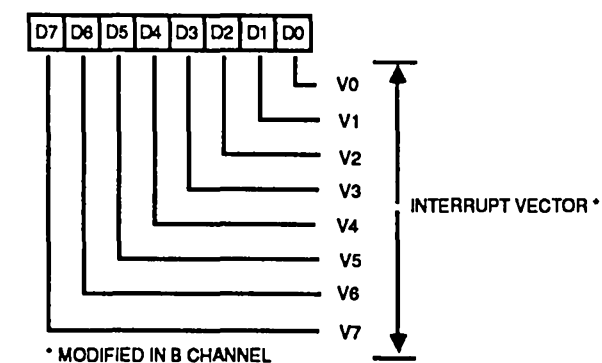


FIGURE 12. READ REGISTER 13

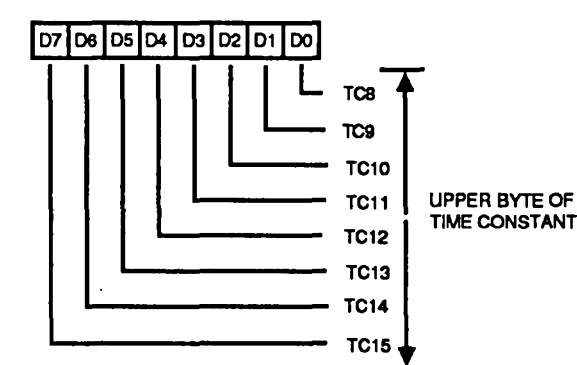


FIGURE 9. READ REGISTER 3

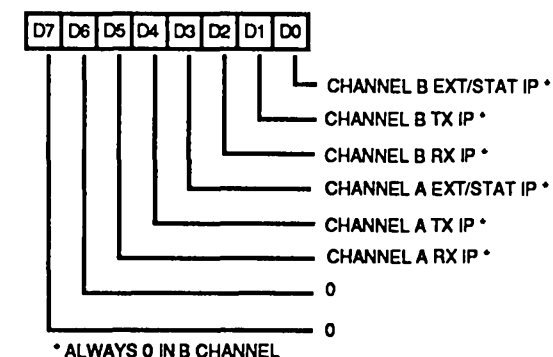


FIGURE 13. READ REGISTER 15

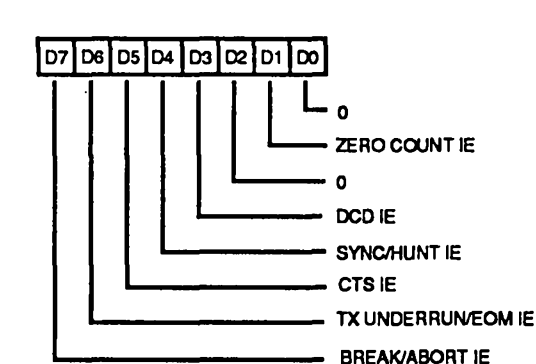
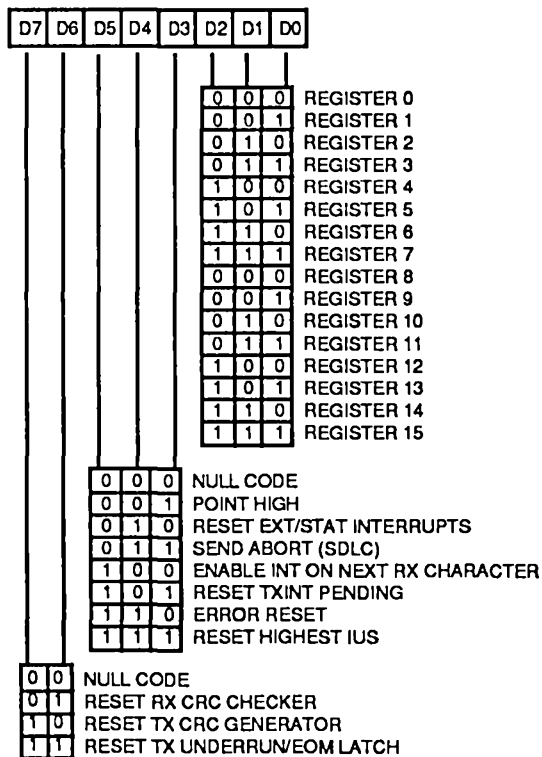


FIGURE 14. WRITE REGISTER 0



* WITH POINT HIGH COMMAND

FIGURE 15. WRITE REGISTER 1

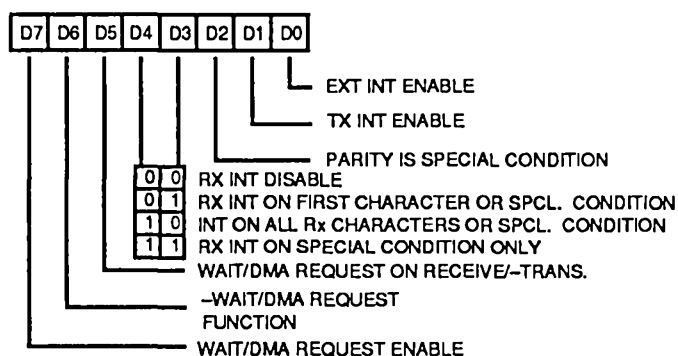


FIGURE 16. WRITE REGISTER 2

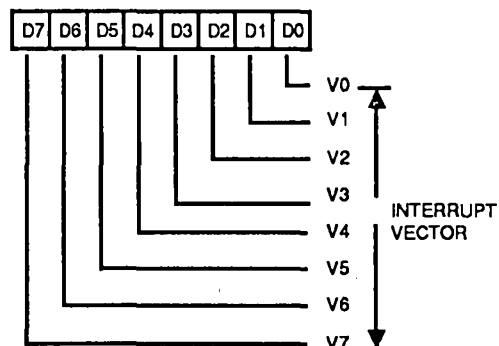


FIGURE 17. WRITE REGISTER 3

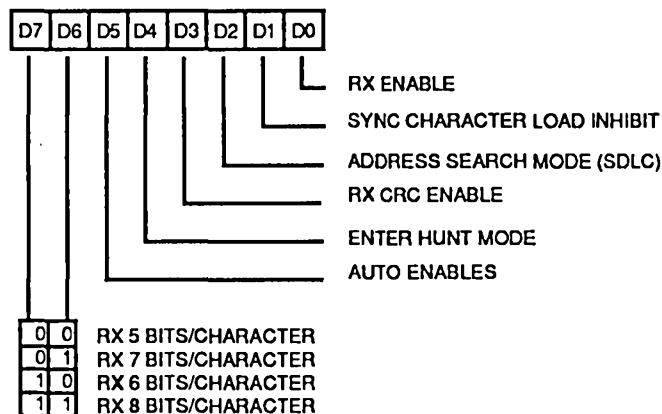


FIGURE 18. WRITE REGISTER 4

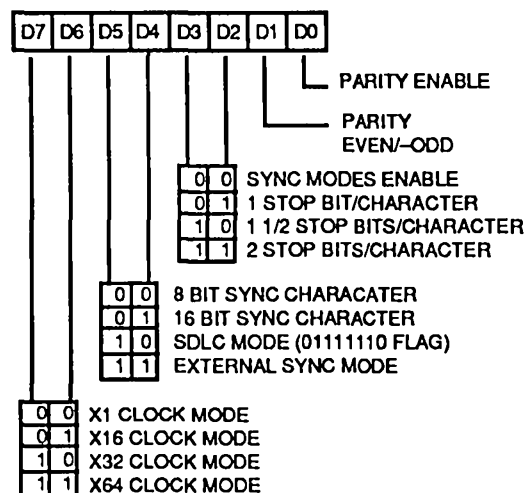


FIGURE 19. WRITE REGISTER 5

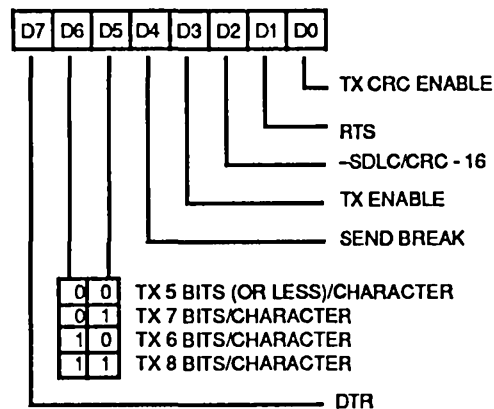


FIGURE 20. WRITE REGISTER 6

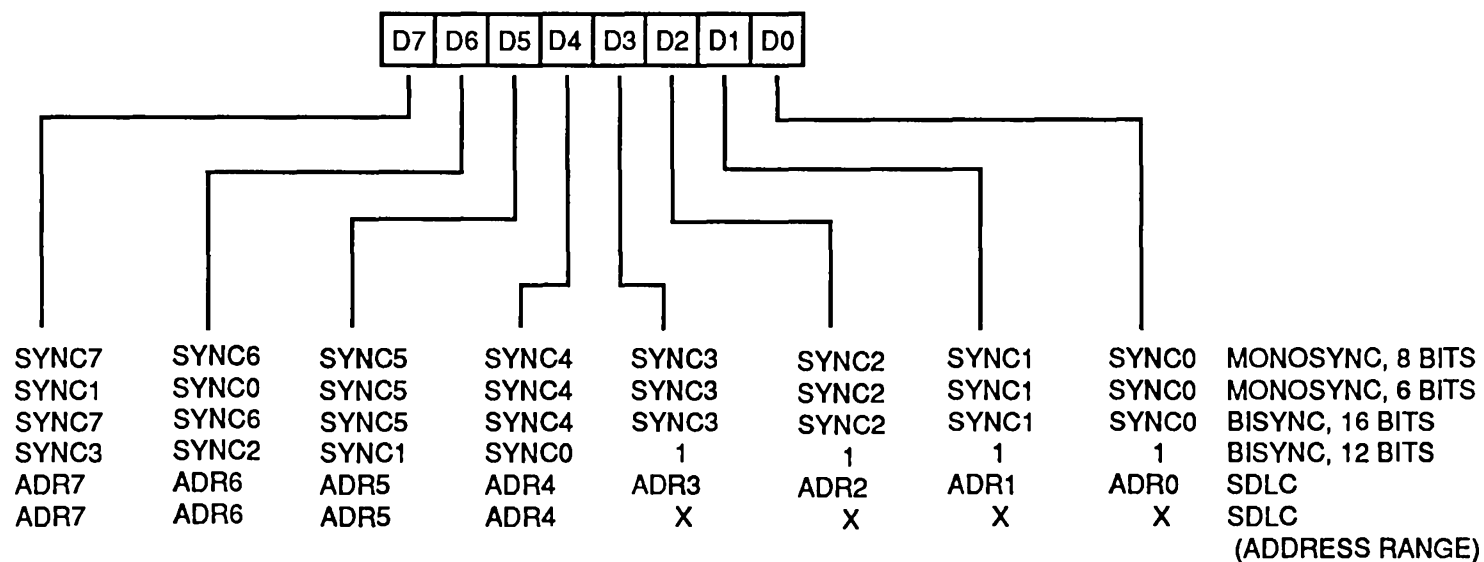


FIGURE 21. WRITE REGISTER 7

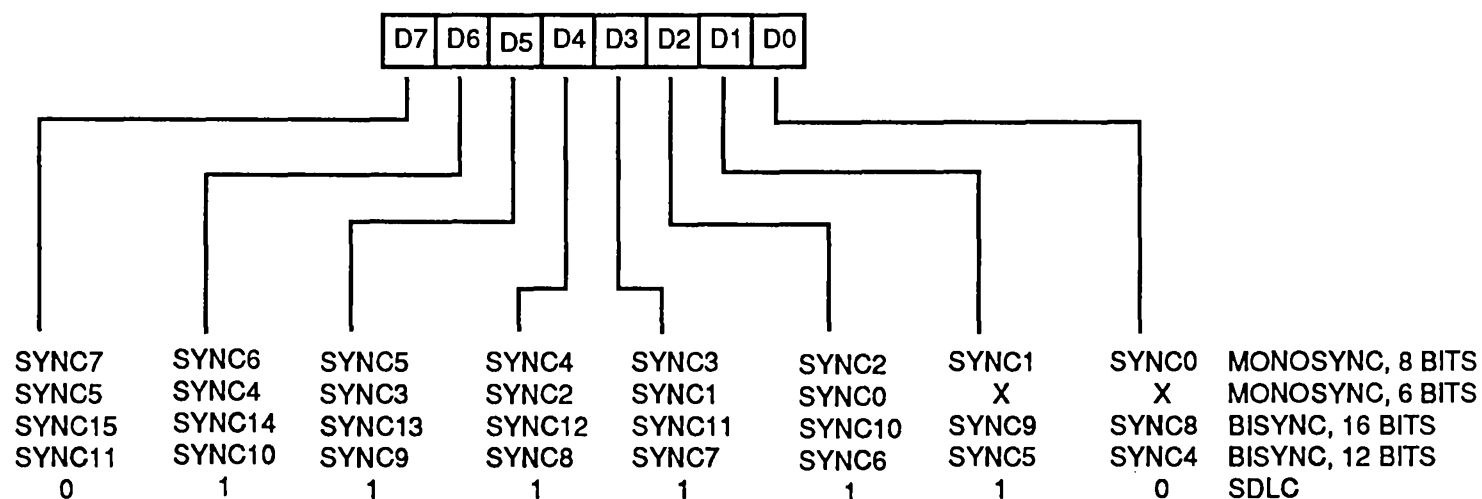


FIGURE 22. WRITE REGISTER 9

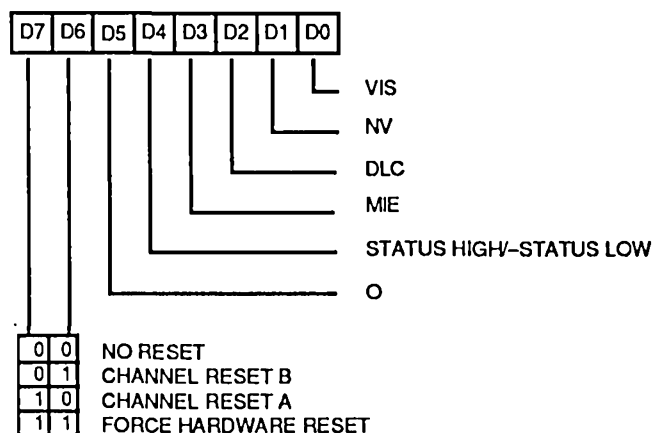


FIGURE 23. WRITE REGISTER 10

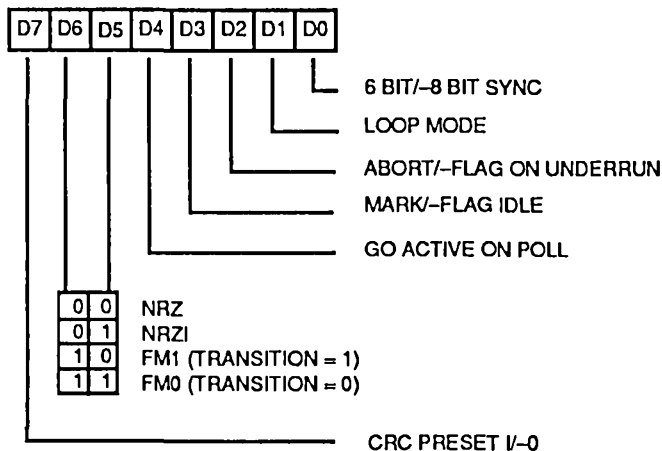


FIGURE 24. WRITE REGISTER 11

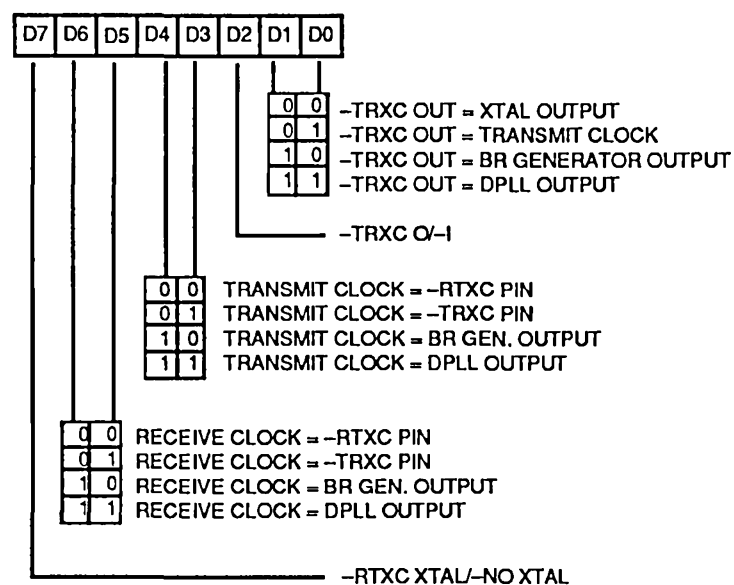


FIGURE 25. WRITE REGISTER 12

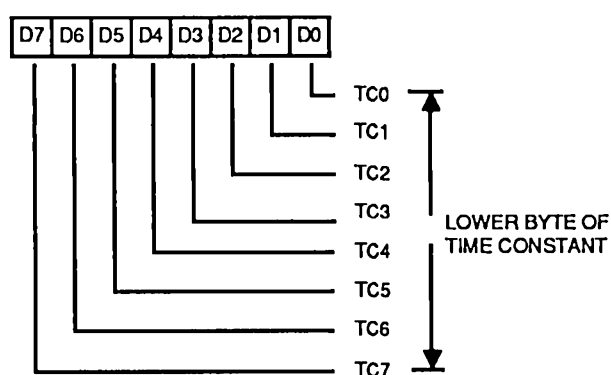


FIGURE 26. WRITE REGISTER 13

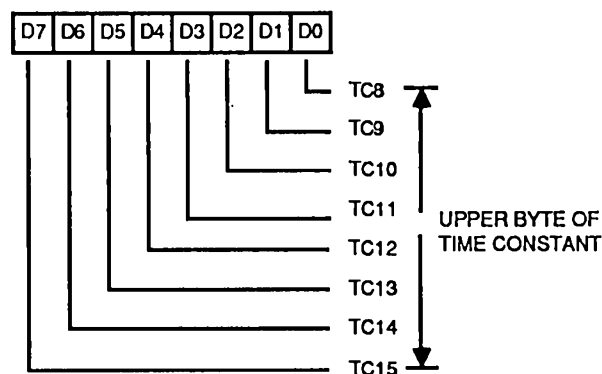


FIGURE 27. WRITE REGISTER 14

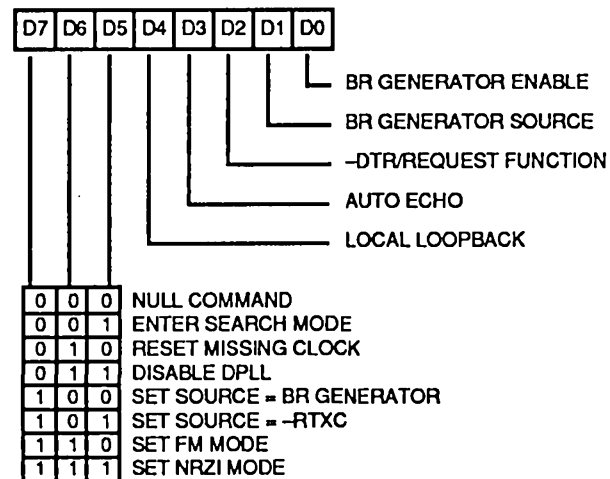


FIGURE 28. WRITE REGISTER 15

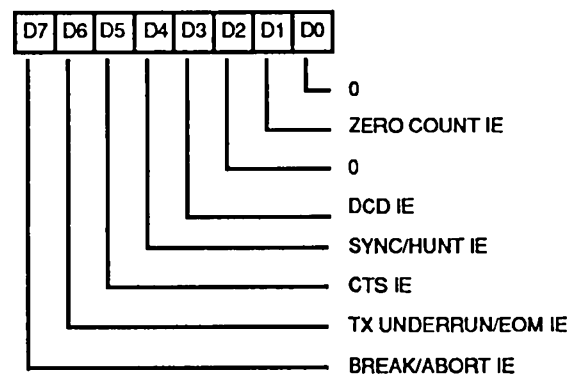


FIGURE 29. READ CYCLE TIMING

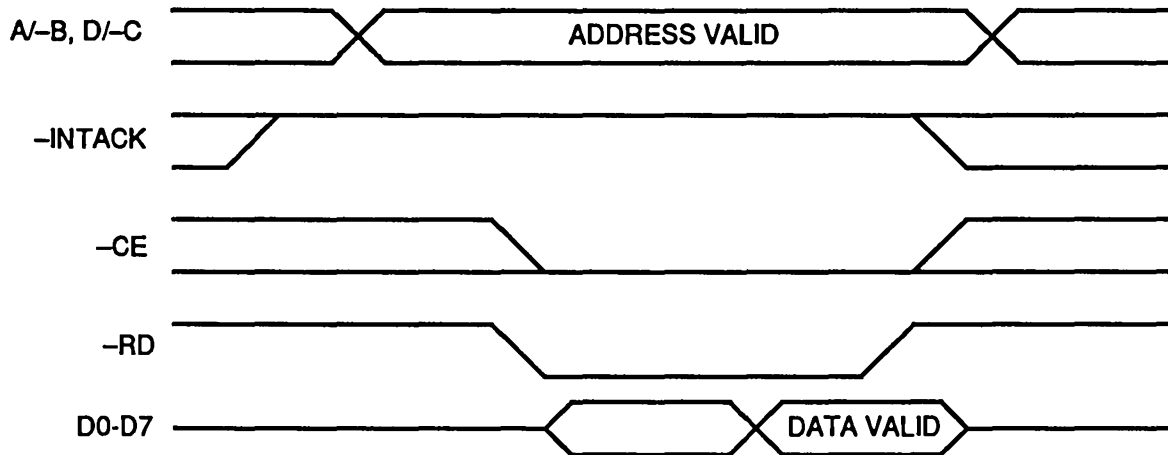


FIGURE 30. WRITE CYCLE TIMING

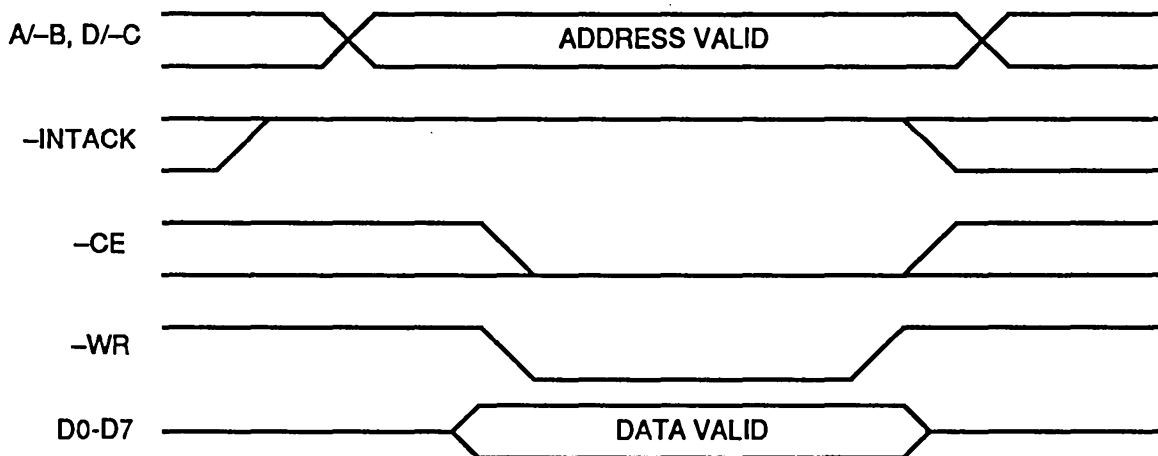


FIGURE 31. INTERRUPT ACKNOWLEDGE CYCLE TIMING



FIGURE 32. READ AND WRITE TIMING (SEE TABLE 1)

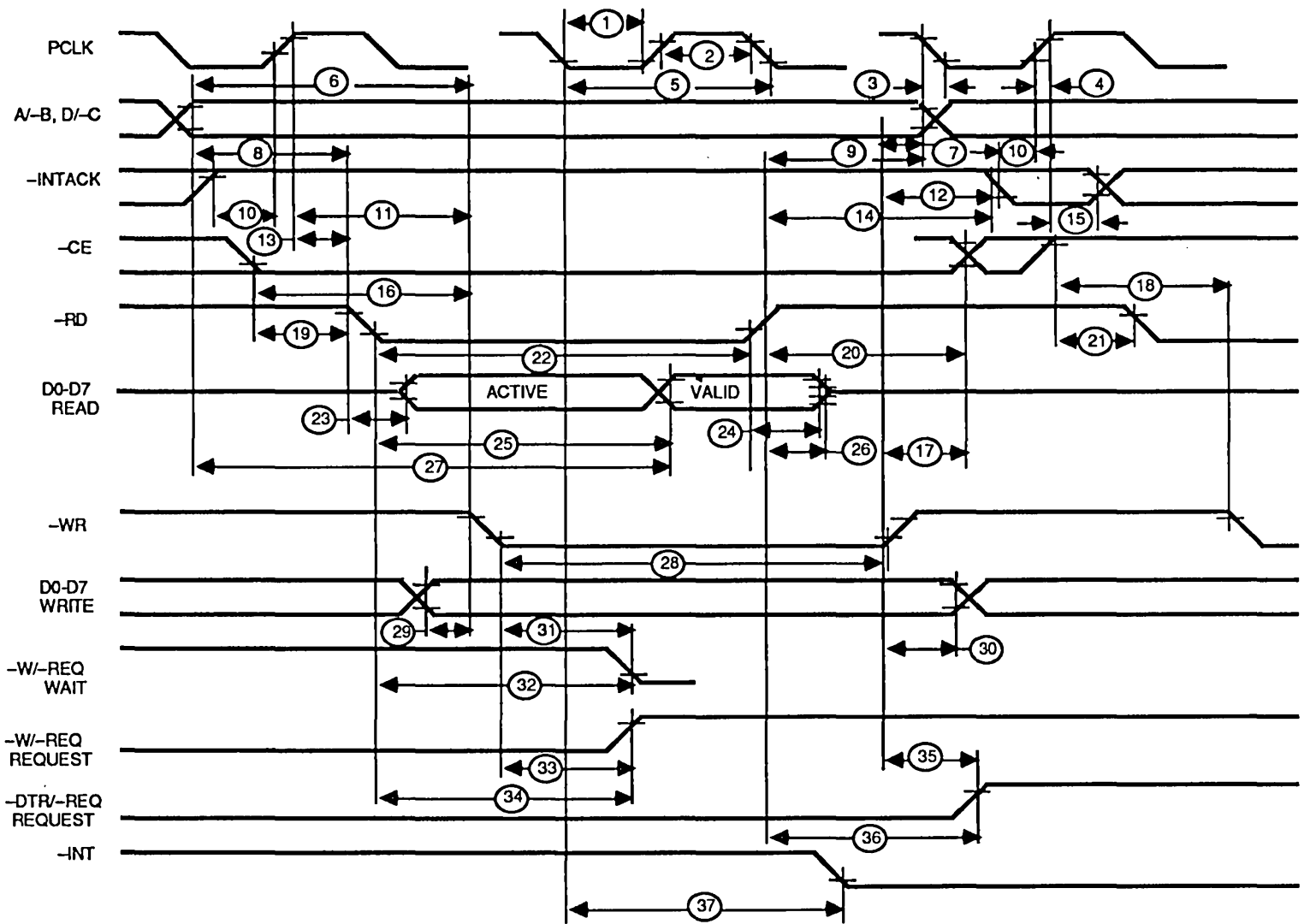


FIGURE 33. RESET TIMING (SEE TABLE 1)

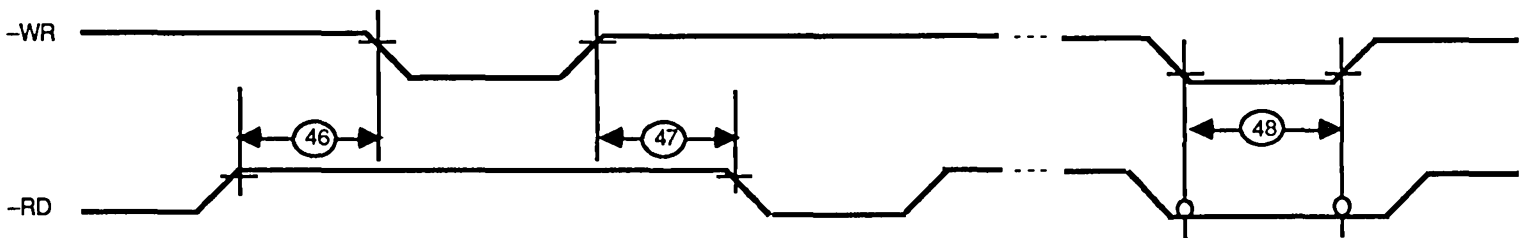


FIGURE 34. CYCLE TIMING (SEE TABLE 1)

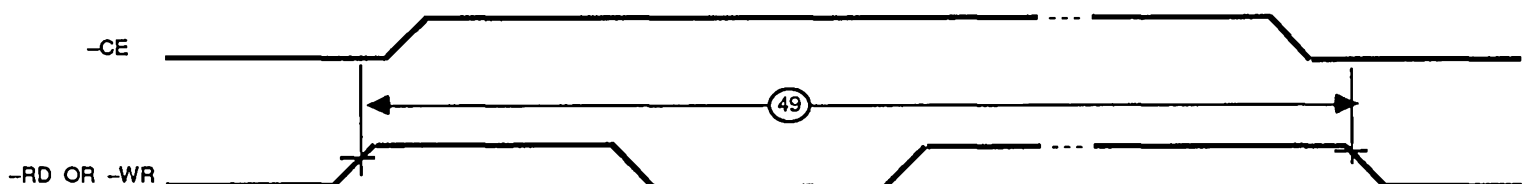


TABLE 1. READ AND WRITE TIMING CHARACTERISTICS: TA = 0°C TO +70°C

No.	Symbol	Parameter	4 MHz		6 MHz		Min	Max	Notes
			Min	Max	Min	Max			
1	TwPCI	PCLK Low Width	105	2000	70	1000			
2	TwPCh	PCLK High Width	105	2000	70	1000			
3	TfPC	PCLK Fall Time		20		10			
4	TrPC	PCLK Rise Time		20		15			
5	TcPC	PCLK Cycle Time	250	4000	165	2000			
6	TsA(WR)	Address to –WR Setup Time	80		80				
7	ThA(WR)	Address to –WR Hold Time	0		0				
8	TsA(RD)	Address to –RD Setup Time	80		80				
9	ThA(RD)	Address to –RD Hold Time	0		0				
10	TsIA(PC)	–INTACK to PCLK Setup Time	0		0				
11	TsIAi(WR)	–INTACK to –WR Setup Time	200		160				2
12	ThIA(WR)	–INTACK to –WR Hold Time	0		0				
13	TsIAi(RD)	–INTACK to –RD Setup Time	200		160				2
14	ThIA(RD)	–INTACK to –RD Hold Time	0		0				
15	ThIA(PC)	–INTACK to PCLK Hold Time	100		100				
16	TsCE1(WR)	–CE Low to –WR Setup Time	0		0				
17	ThCE(WR)	–CE to –WR Hold Time	0		0				
18	TsCEh(WR)	–CE High to –WR Setup Time	100		70				2
19	TsCE1(RD)	–CE Low to –RD Setup Time	0		0				2
20	ThCE(RD)	–CE to –RD Hold Time	0		0				2
21	TsCEh(RD)	–CE High to –RD Setup Time	100		70				2
22	TwRD1	–RD Low Width	390		250				
23	TdRD(DRA)	–RD to Read Data Active Delay	0		0				
24	TdRDrd(DR)	–RD to Read Data Not Valid Delay	0		0				
25	TdRDf(DR)	–RD to Read Data Valid Delay		250		180			
26	TdRD(DRz)	–RD to Read Data Float Delay		70		45			3
27	TdA(DR)	Address Required Valid to Read Data Valid Delay		590		420			
28	TwWR1	–WR Low Width	390		250				
29	TsDW(WR)	Write Data to –WR Setup Time	0		0				
30	ThDW(WR)	Write Data to –WR Hold Time	0		0				
31	TdWR(W)	–WR to Wait Valid Delay		240		200			5
32	TdRD(W)	–RD to Wait Valid Delay		240		200			5
33	TdWRf(REQ)	–WR to –W/–REQ Not Valid Delay		240		200			
34	TdRDf(REQ)	–RD to –W/–REQ Not Valid Delay		240		200			
35	TdWRr(REQ)	–WR to –DTR/–REQ Not Valid Delay		(5TcPC +300)		(5TcPC +250)			
36	TdRDrd(REQ)	–RD to –DTR/–REQ Not Valid Delay		(5TcPC +300)		(5TcPC +250)			
37	TdPC(INT)	PCLK to –INT Valid Delay		500		500			5
38	TdIAi(RD)	–INTACK to –RD (Acknowledge) Delay	250		250				6
39	TwRDA	–RD (Acknowledge) Width	285		250				
40	TdRDA(DR)	–RD (Ack.) to Read Data Valid Delay		190		180			
41	TsIEI(RDA)	IEI to –RD (Acknowledge) Setup Time	120		100				
42	ThIEI(RDA)	IEI to –RD (Acknowledge) Hold Time	0		0				
43	TdIEI(IEO)	IEI to IEO Delay Time		120		100			
44	TdPC(IEO)	PCLK to IEO Delay		250		250			
45	TdRDA(INT)	–RD to –INT Inactive Delay		500		500			4
46	TdRD(WRQ)	–RD to –WR Delay for No Reset	30		15				
47	TdWRQ(RD)	–WR to –RD Delay for No Reset	30		30				
48	TwRES	–WR and –RD Coincident Low for Reset	250		250				
49	Trc	Valid Access Recovery Time	(6TcPC +200)		(6TcPC +130)				

Read and Write Timing Notes:

1. Units are in nanoseconds.
2. Parameter does not apply to Interrupt Acknowledge transactions.
3. Float delay is defined as the time required for a ± 0.5 V change at the output with a maximum dc load and minimum ac load.
4. Parameter applies only between transactions involving the ESCC.
5. Open-drain output, measured with open-drain test load.
6. Parameter is system-dependent. For any ESCC in the daisy chain, $T_{dIAi}(\text{RD})$ must be greater than the sum of $T_{dPC}(\text{IEO})$ for the highest priority device in the daisy chain, $T_{sIEI}(\text{RDA})$ for the ESCC, and $T_{dIEIf}(\text{IEO})$ for each device separating them in the daisy chain.

FIGURE 35. INTERRUPT ACKNOWLEDGE TIMING (SEE TABLE 1)

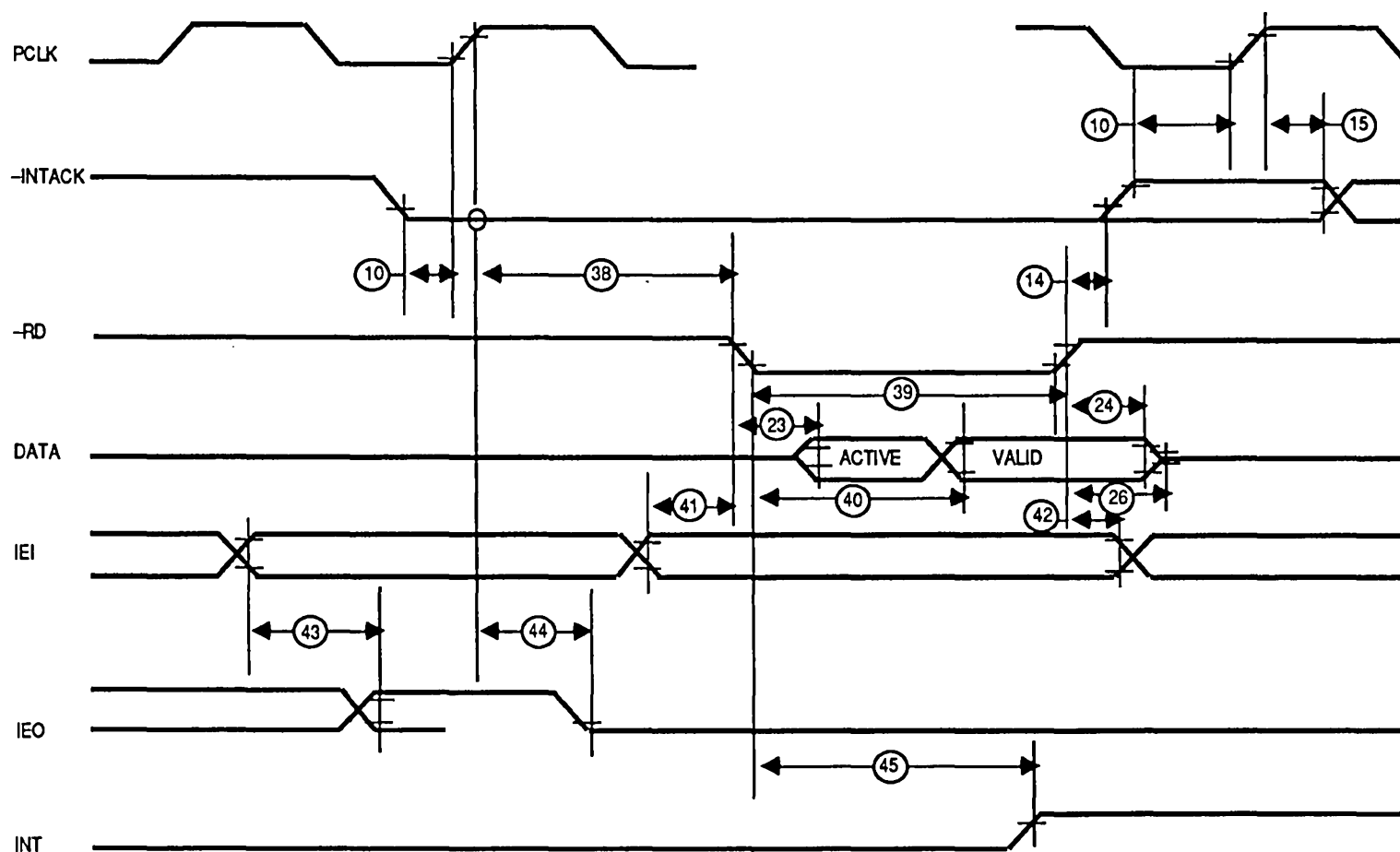




FIGURE 36. GENERAL TIMING (SEE TABLE 2)

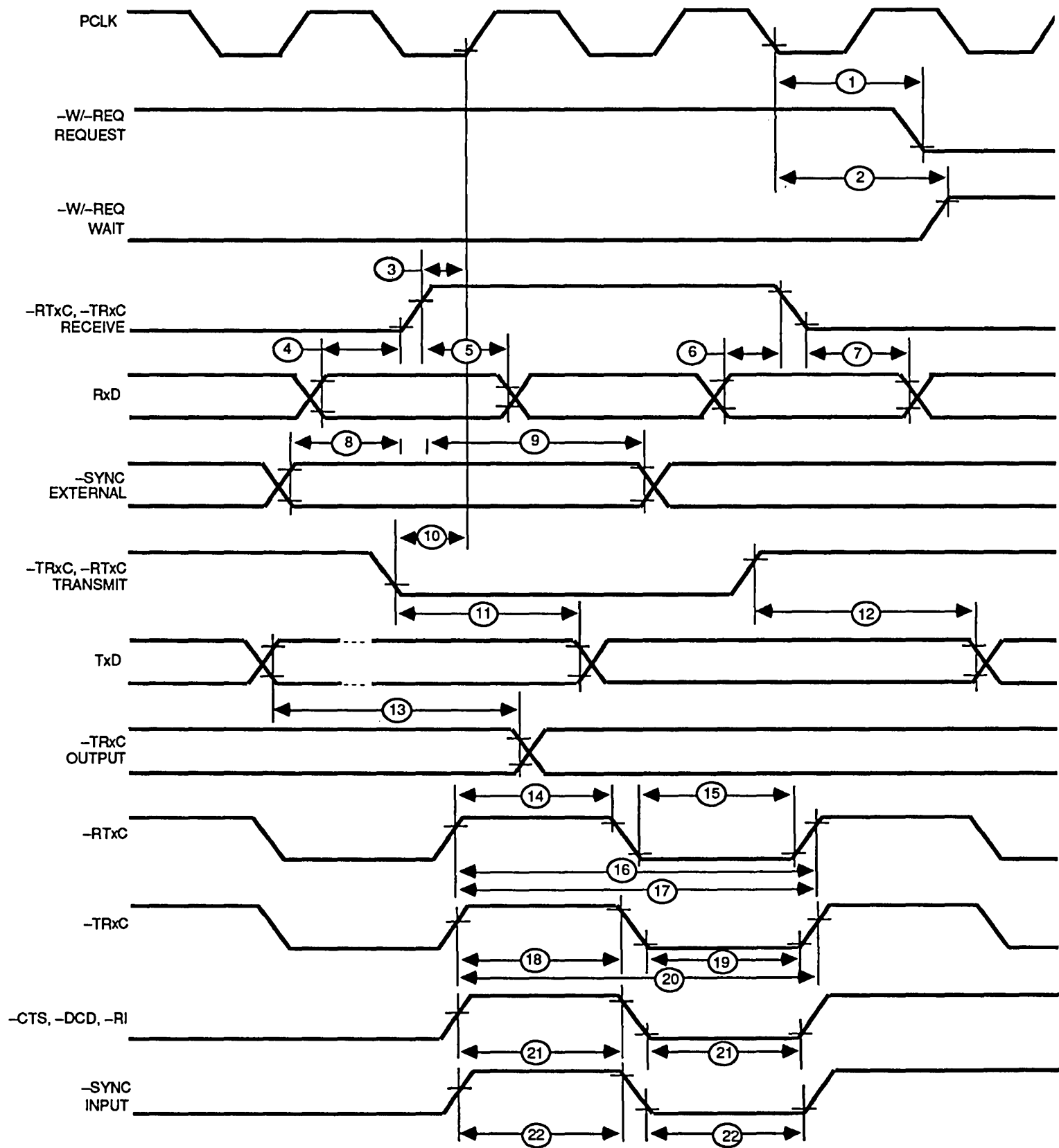




TABLE 2. GENERAL TIMING

No.	Symbol	Parameter	4 MHz		6 MHz				Notes
			Min	Max	Min	Max	Min	Max	
1	TdPC(REQ)	PCLK to -W/-REQ Valid Delay		250		250			
2	TdPC(W)	PCLK to Wait Inactive Delay		350		350			
3	Ts RxC(PC)	-RxC to PCLK Setup Time (PCLK + 4 Case Only)	80	TwPC1	70	TwPC1			2,5
4	TsRXD(RXCr)	RxD to -RxC Setup Time (X1 Mode)		0		0			2
5	ThRXD(RXCr)	RxD to -RxC Hold Time (X1 Mode)		150		150			2
6	TsRXD(RXCf)	RxD to -RxC Setup Time (X1 Mode)		0		0			2,6
7	ThRXD(RXCf)	RxD to -RxC Hold Time (X1 Mode)		150		150			2,6
8	TsSY(RXC)	-SYNC to -RxC Setup Time		-200		-200			4,2
9	ThSY(RXC)	-SYNC to -RxC Hold Time	3TcPC +200		3TcPC +200				4,2
10	TsTXC(PC)	-TxC to PCLK Setup Time	0		0				3,5
11	TdTXCf(TXD)	-TxC to Tx D Delay (X1 Mode)		300		230			3
12	TdTXCr(TXD)	-TxC to Tx D Delay (X1 Mode)		300		230			3,5
13	TdTXD(TRX)	TxD to -TRxC Delay (Send Clk Echo)		200		200			
14	TwRTXh	-RTxC High Width	180		180				7
15	TwRTXI	-RTxC Low Width	180		180				7
16	TcRTX	-RTxC Cycle Time	400		400				7
17	TcRTXX	Crystal Oscillator Period	250	1000	250	1000			3
18	TwTRXh	-TRxC High Width	180		180				4,7
19	TwTRXI	-TRxC Low Width	180		180				4,7
20	TcTRX	-TRxC Cycle Time	400		400				4,7
21	TwEXT	-DCD or -CTS Pulse Width	200		200				
22	TwSY	-SYNC Pulse Width	200		200				

TABLE 3. SYSTEM TIMING

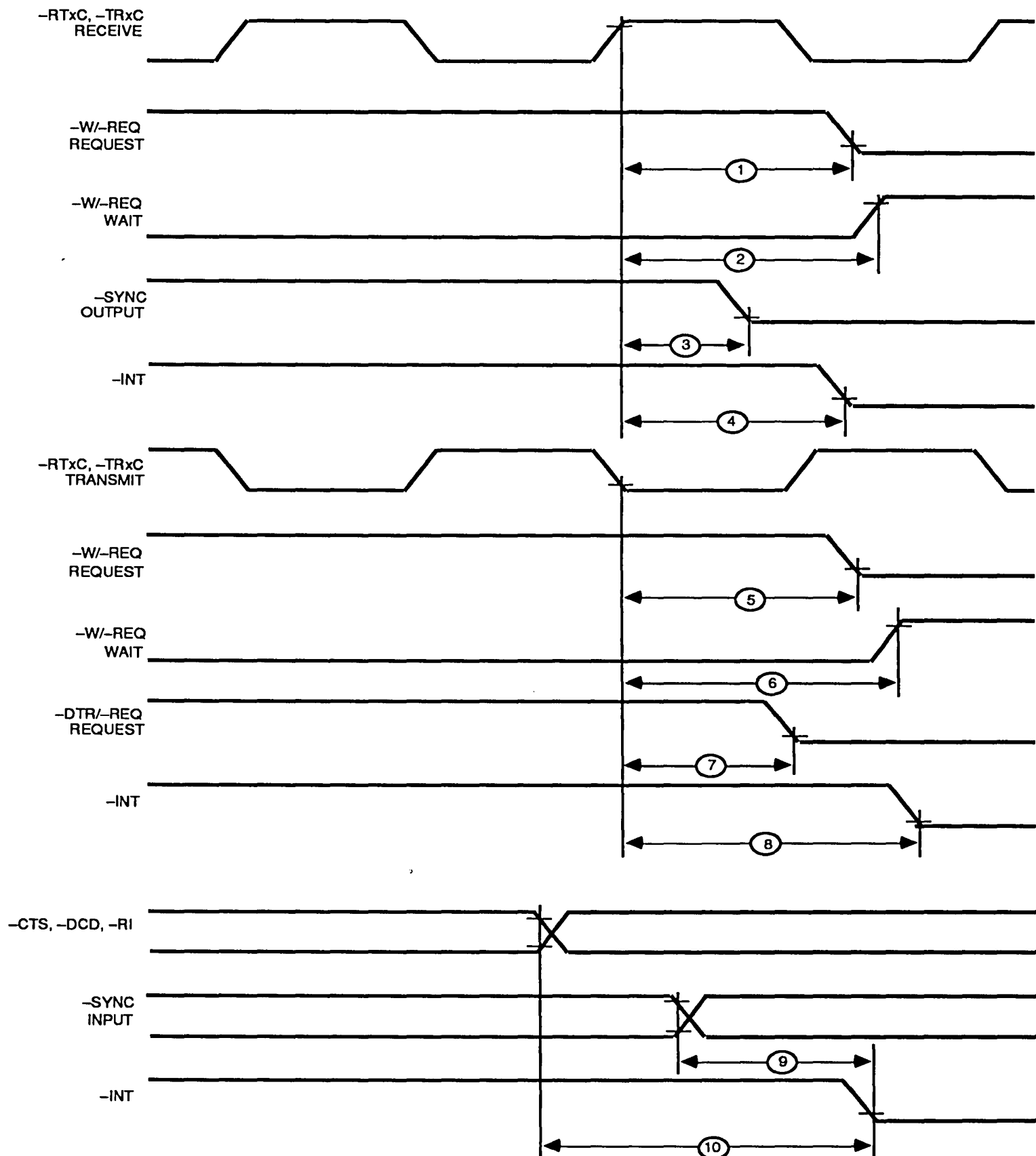
No.	Symbol	Parameter	4 MHz		6 MHz				Notes
			Min	Max	Min	Max	Min	Max	
1	TdRXC(REQ)	-RxC to -W/-REQ Valid Delay	8	12	8	12			2
2	TdRXC(W)	-RxC to Wait Inactive Delay	8	12	8	12			1,2
3	TdRXC(SY)	-RxC to -SYNC Valid Delay	4	7	4	7			2
4	TdRXC(INT)	-RxC to -INT Valid Delay	10	16	10	16			1,2
5	TdTXC(REQ)	-Tx C to -W/-REQ Valid Delay	5	8	5	8			3
6	TdTXC(W)	-Tx C to Wait Inactive Delay	5	8	5	8			1,3
7	TdTXC(DRQ)	-Tx C to -DTR/-REQ Valid Delay	4	7	4	7			3
8	TdTXC(INT)	-Tx C to -INT Valid Delay	6	10	6	10			1,3
9	TdSY(INT)	-SYNC to -INT Valid Delay	2	6	2	6			1
10	TdEXT(INT)	-DCD or -CTS to -INT Valid Delay	2	6	2	6			1

General and System Timing Notes:

1. Open-drain output, measured with open-drain test load.
2. RxC is RTxC or TRxC, whichever is supplying the transmit clock.
3. Tx C is TRxC or RTxC, whichever is supplying the transmit clock.
4. Both TrxC and SYNC have 30 pF capacitors connected to ground.
5. Applies only if the data rate is one-fourth the PCLK rate. In all other cases, no phase relationship between RxC and PCLK or Tx C and PCLK is required.
6. Applies only to FM encoding/decoding.
7. Applies only for transmitter and receiver; DPLL and baud rate generator timing are identical to chip PCLK requirements.
8. Units are in nanoseconds (ns).



FIGURE 37. SYSTEM TIMING (SEE TABLE 3)



ABSOLUTE MAXIMUM RATINGS

Voltages on all pins with respect to GND -0.3V to 7.0V

Operating Ambient Temperature 0°C to +70°C

Storage Temperature -65°C to +150°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above

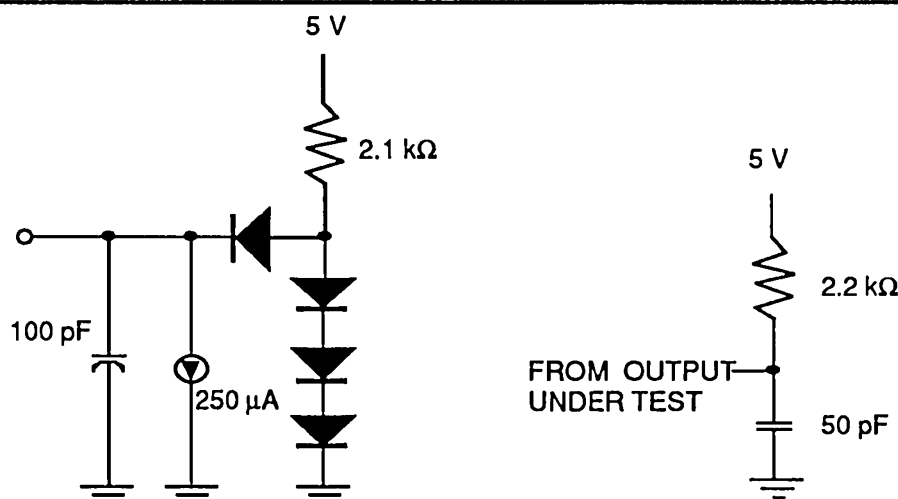
those listed on the operational sections of this specification is not implied and exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

STANDARD TEST CONDITIONS

The dc characteristics and capacitance section below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND. Positive current flows into the referenced pin.

Standard conditions are as follows:

- $+4.75\text{ V} \leq V_{CC} \leq +5.25\text{ V}$
- $GND = 0\text{ V}$
- TA as shown in Ordering Information


DC CHARACTERISTICS: $V_{CC} = 5\text{ V} \pm 5\%$, $T_A = 0^\circ\text{C}$ to 70°C

Symbol	Parameter	Min	Max	Unit	Conditions
V_{IH}	Input High Voltage	2.0	$V_{CC} + 0.3$	V	
V_{IL}	Input Low Voltage	-0.3	0.8	V	
V_{OH}	Output High Voltage	2.4		V	$I_{OH} = -250\text{ }\mu\text{A}$
V_{OL}	Output Low Voltage		0.4	V	$I_{OH} = +2.0\text{ mA}$
I_{IL}	Input Leakage		± 10.0	μA	$0.4\text{ V} \leq V_{IN} \leq +2.4\text{ V}$
I_{OL}	Output Leakage		± 10.0	μA	$0.4\text{ V} \leq V_{IN} \leq +2.4\text{ V}$
I_{CC}	V_{CC} Supply Current		250	mA	Clock Frequency = 8 MHz

CAPACITANCE: $T_A = 0^\circ\text{C}$ to 70°C , $f = 1\text{ MHz}$

Symbol	Parameter	Min	Max	Unit	Conditions
C_{IN}	Input Capacitance		10	pF	Unused Inputs Grounded
C_{OU}	Output Capacitance		15	pF	
$C_{I/O}$	Bidirectional Capacitance		20	pF	Unused Inputs Grounded

ENHANCED SERIAL COMMUNICATIONS CONTROLLER (ESCC)

FEATURES

- Enhanced SCC functions support DMA
 - 14-bit byte counter
 - 19-bit-wide FIFO
- Completely downward compatible with the NMOS 8530
- Two independent full-duplex channels
- Programmable clock factor
- Break generation and error detection
- Intelligent SDLC/HDLC
- Local loopback and auto echo modes
- Internal or external character synchronization
- Low power consuming CMOS

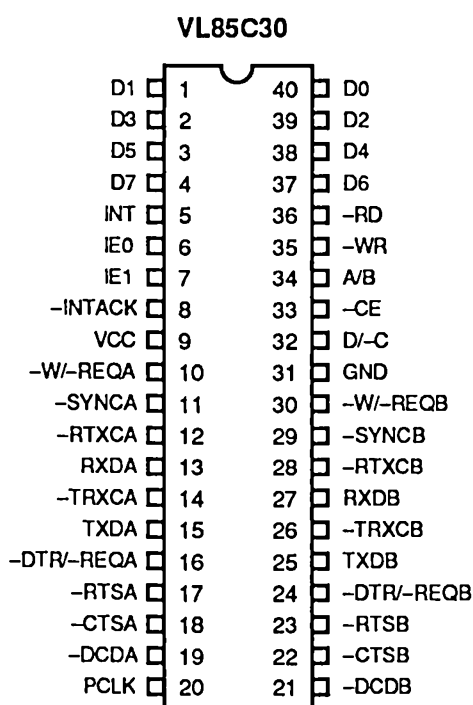
DESCRIPTION

The VL85C30 CMOS Enhanced Serial Communications Controller (ESCC) is a dual-channel, multi-protocol data communications peripheral designed for use with non-multiplexed buses. The ESCC can be software configured for a wide variety of serial communications applications. The device contains a variety of new, sophisticated internal functions, including all of the features of the NMOS 8530. In addition, the VL85C30 Enhanced SCC contains a 10 x 19-bit FIFO array and 14-bit byte counter. These features, in addition to the new higher clock frequency capabilities, allow the ESCC to be used with a direct memory access (DMA) controller.

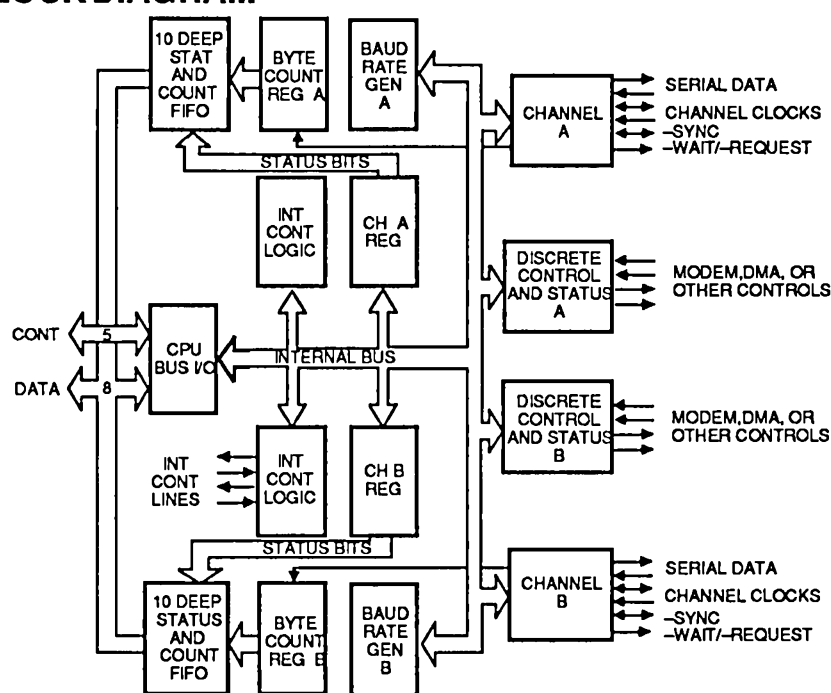
The ESCC handles asynchronous formats, such as synchronous byte-oriented protocols as IBM Bisync and such synchronous bit-oriented protocols as HDLC and IBM SDLC. This versatile device supports virtually any serial data transfer application (cassette, diskette, tape drives, etc.), including DMA.

The device can generate and check CRC codes in any synchronous mode and can be programmed to check data integrity in various modes. The ESCC also has facilities for modem controls in both channels, in addition to its Byte - Counting Register and FIFO in SDLC mode.

PIN DIAGRAM



BLOCK DIAGRAM

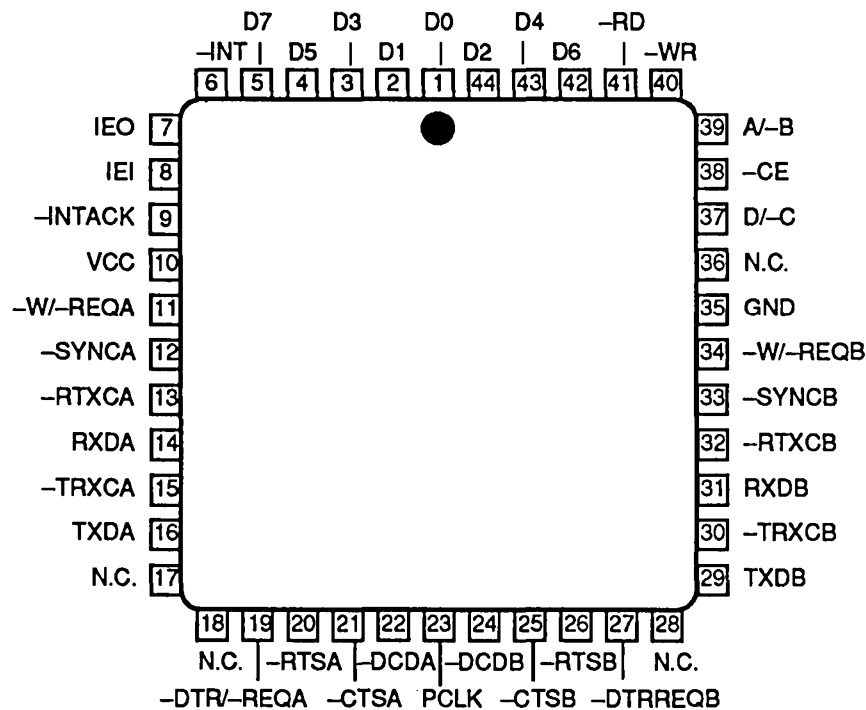


ORDER INFORMATION

Part Number	Clock Frequency	Package
VL85C30-8PC VL85C30-8QC VL85C30-8CC	8 MHz	Plastic DIP Plastic Leaded Chip Carrier (PLCC) Ceramic DIP
VL85C30-10PC VL85C30-10QC VL85C30-10CC	10 MHz	Plastic DIP Plastic Leaded Chip Carrier (PLCC) Ceramic DIP
VL85C30-12PC VL85C30-12QC VL85C30-12CC	12 MHz	Plastic DIP Plastic Leaded Chip Carrier (PLCC) Ceramic DIP

Note: Operating temperature range is 0°C to +70°C.

PIN DIAGRAM



SIGNAL DESCRIPTIONS

Signal Name	DIP Pin Number	Signal Description
A/-B	34	Channel A/Channel B Select - This input signal selects the channel on which the read or write operation occurs.
-CE	33	Chip Enable - This active low input signal selects the ESCC for a read or write operation.
-CTSA, -CTSB	18, 22	Clear To Send - Active low inputs - If these pins are programmed as auto enables, a low on the inputs enables the respective transmitters. If not programmed as auto enables, they may be used as general-purpose inputs. Both inputs are Schmitt trigger buffered to accommodate slow rise time inputs. The ESCC detects pulses on these inputs and can interrupt the CPU on both logic level transitions.
D/-C	32	Data/Control Select - This input signal defines the type of information transferred to or from the ESCC. A HIGH means data is transferred; a low indicates a command.
-DCDA, -DCDB	19 21	Data Carrier Detect - Active low inputs - These pins function as receiver enables if they are programmed for auto enables; otherwise, they may be used as general-purpose input pins. Both pins are Schmitt trigger buffered to accommodate slow rise time signals. The ESCC detects pulses on these pins and can interrupt the CPU on both logic level transitions.
D0-D7	40,1,39,2,38,	Data Bus - These bidirectional, three-state lines carry data and commands to and from the ESCC.
-DTR/-REQA -DTR/-REQB	16, 24	Data Terminal Ready/Request - These active low outputs follow the state programmed into the -DTR bit. They can also be used as general-purpose outputs or as request lines for a direct memory access (DMA) controller.
IEI	7	Interrupt Enable In - Active high output - IEI is used with IEO to form an interrupt daisy chain when there is more than one interrupt-driven device. A high IEI indicates that no other higher priority device has an interrupt underservice or is requesting an interrupt.
IEO	6	Interrupt Enable Out - Active high output - IEO is high only if IEI is high and the CPU is not servicing an ESCC interrupt or the SCC is not requesting an interrupt (Interrupt Acknowledge cycle only). IEO is connected to the next lower priority device's IEI input and thus inhibits interrupts from lower priority devices.
-INT	5	Interrupt Request - Active low open-drain output - This signal is activated when the ESCC requests an interrupt.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	DIP Pin Number	Signal Description
-INTACK	8	Interrupt Acknowledge - Active low input - This signal indicates an active Interrupt Acknowledge cycle. During this cycle, the ESCC interrupt daisy chain settles. When -RD becomes active, the ESCC places an interrupt vector on the data bus (if IEI is high). The -INTACK signal is latched by the rising edge of PCLK.
PCLK	20	Clock - This input is the master ESCC clock used to synchronize internal signals. PCLK is a TTL level signal.
-RD	36	Read - Active low input - This signal indicates a read operation and, when the ESCC is selected, enables the ESCC's bus drivers. During the Interrupt Acknowledge cycle, this signal gates the interrupt vector onto the bus if the ESCC is the highest priority device requesting an interrupt.
RXDA, RXDB	13, 27	Receive Data - Active high inputs - These input signals receive serial data at standard TTL levels.
-RTXCA, -RTXCB	12, 28	Receive/Transmit Clocks - Active low inputs - These pins can be programmed in several different modes of operation. In each channel, -RTXC may supply the receive clock, the transmit clock, the clock for the baud rate generator, or the clock for the digital phase locked loop. These pins can also be programmed for use with the respective -SYNC pins as a crystal oscillator. The receive clock may be 1, 16, 32, or 64 times the data rate in asynchronous modes.
-RTSA, -RTSB	17, 23	Request To Send - Active low outputs - When the -RTS bit in write register 5 (figure 7) is set, the -RTS signal goes low. When the -RTS bit is reset in the asynchronous mode and auto enable is on, the signal goes high after the transmitter is empty. In synchronous mode or in asynchronous mode with auto enable off, the -RTS pin strictly follows the state of the -RTS bit. Both pins can be used as general purpose outputs.
-SYNCA, -SYNCB	11, 29	Synchronization - Active low inputs or outputs - These pins can act either as inputs or outputs, or part of the crystal oscillator circuit. In the asynchronous receive mode (crystal oscillator option not selected), these pins are inputs similar to -CTS and -DCD. In this mode, transitions on these lines affect the state of the synchronous/hunt status bits in read register 0 (Figure 6) but have no other function. In external synchronization mode with the crystal oscillator not selected, these lines also act as inputs. In this mode, -SYNC must be driven low to receive clock cycles after the last bit in the synchronous character is received. Character assembly begins on the rising edge of the receive clock immediately preceding the activation of -SYNC. In the internal synchronization mode (Monosync and Bisync) with the crystal oscillator not selected, these pins act as outputs and are active only during the part of the receive clock cycle in which synchronous characters are recognized. The synchronous condition is not latched, so these outputs are active each time a synchronization pattern is recognized (regardless of character boundaries). In SDLC mode, these pins act as outputs and are valid on receipt of a flag.
TXDA, TXDB	15, 25	Transmit Data - Active high outputs - These output signals transmit serial data at standard TTL levels.
-TRXCA, -TRXCB	14, 26	Transmit/Receive Clocks - Active low inputs or outputs - These pins can be programmed in several different modes of operation. -TRXC may supply the receive clock or the transmit clock in the input mode or supply the output of the digital phase-locked loop, the crystal oscillator, the baud rate generator, or the transmit clock in the output mode.
-WR	35	Write - Active low input - When the ESCC is selected, this signal indicates a write operation. The coincidence of -RD and -WR is interpreted as a reset.
-W/-REQA, -W/-REQB	10, 30	Wait/Request - Open-drain outputs when programmed for a wait function, driven high or low when programmed for a Request function - These dual-purpose outputs may be programmed as Request lines for a DMA controller or as Wait lines to synchronize the CPU to the ESCC data rate. The reset state is Wait.

FUNCTIONAL DESCRIPTION

The functional capabilities of the ESCC can be described from two different points of view. As a data communications device, it transmits and receives data in a wide variety of data communications protocols. As a microprocessor peripheral, the ESCC offers valuable features as vectored interrupts, polling, and simple handshake capability.

DATA COMMUNICATIONS CAPABILITY

The ESCC provides two independent full-duplex channels programmable for use in any common asynchronous or synchronous data communication protocol. Figure 1 and the following description briefly detail these protocols.

Asynchronous modes - Transmission and reception can be accomplished independently on each channel with 5 to 8 bits per character, plus optional even or odd parity. The transmitters can supply 1, 1 1/2, or 2 stop bits per character and a break output at any time. The receiver break-detection logic interrupts the CPU both at the start and at the end of a received break.

Reception is protected from spikes by a transient spike-rejection mechanism that checks the signal one-half a bit time after a low level is detected on the receive data input (RXDA or RXDB). If the low does not persist (as in the case of a transient), the character assembly process does not start.

Framing errors and overrun errors are detected and buffered together with the partial character on which they occur. Vectored interrupts allow fast servicing or error conditions using dedicated routines. Furthermore, a built-in checking process avoids the interpretation of a framing error as a new start bit: a framing error results in the addition of one-half a bit time to the point at which the search for the next start bit begins.

The ESCC does not require symmetric transmit and receive clock signals a feature allowing use of the wide variety of clock sources. The transmitter and receiver can handle data at a rate of 1, 1/16, 1/32, or 1/64 of the clock rate supplied to the receive and transmit clock inputs. In asynchronous modes,

the -SYNC pin may be programmed as an input used for such functions as monitoring a ring indicator.

Synchronous modes. The ESCC supports both byte-oriented and bit-oriented synchronous communication. Synchronous byte-oriented protocols can be handled in several modes, allowing character synchronization with a 6-bit or 8-bit synchronous character (Monosync) any 12-bit synchronization pattern (Bisync), or with an external synchronous signal. Leading sync characters can be removed without interrupting the CPU.

5- or 7-bit synchronous characters are detected with 8- or 16-bit patterns in the ESCC by overlapping the larger pattern across multiple incoming synchronous characters.

The CRC checking for synchronous byte-oriented modes is delayed by one character time so that the CPU may disable CRC checking on specific characters. This allows the implementation of IBM Bisync. protocols.

Both CRC-16 ($X^{16} + X^5 + X^2 + 1$) and CCITT ($X^{16} + X^{12} + X^5 + 1$) error checking polynomials are supported. Either polynomial may be selected in all Synchronous modes. Users may preset the CRC generator and checker to all ones or all zeros. The ESCC also provides a feature that automatically transmits CRC data when no other data is available for transmission. This allows for high-speed transmissions under DMA control, with no need for CPU intervention at the end of a message. When there is no data or CRC to send in synchronous modes, the transmitter inserts 6-, 8-, or 16-bit synchronous characters, regardless of the programmed character length.

The ESCC supports synchronous bit-oriented protocols, such as SDLC and HDLC, by performing automatic flag sending, zero insertion, and CRC generation. A special command can be used to abort a frame in transmission. At the end of a message, the ESCC automatically transmits the CRC and trailing flag when the transmitter underruns. The transmitter may also be

programmed to send an idle line consisting of continuous flag characters or a steady marking condition.

If a transmit underrun occurs in the middle of a message, an external/status interrupt warns the CPU of this status change so that an abort may be issued. The ESCC may also be programmed to send an abort itself in case of an underrun, relieving the CPU of this task. One to eight bits per character can be sent, allowing reception of a message with no prior information about the character structure in the information field of a frame.

The receiver automatically acquires synchronization on the leading flag of a frame in SDLC or HDLC and provides a synchronization signal on the -SYNC pin (an interrupt can also be programmed). The receiver can be programmed to search for frames addressed by a single byte (or four bits within a byte) of a user-selected address or to a global broadcast address. In this mode, frames not matching either the user-selected or broadcast address are ignored. The number of address bytes can be extended under software control. For receiving data, an interrupt on the first received character, or an interrupt on every character, or on special condition only (end-of-frame) can be selected. The receiver automatically deletes all zeros inserted by the transmitter during character assembly. The CRC is also calculated and is automatically checked to validate frame transmission. At the end of transmission, the status of a received frame is available in the status registers. In SDLC mode, the ESCC must be programmed to use the SDLC CRC polynomial, but the generator and checker may be preset to all ones or all zeros.

The CRC is inverted before transmission and the receiver checks against the bit pattern 0001110100001111.

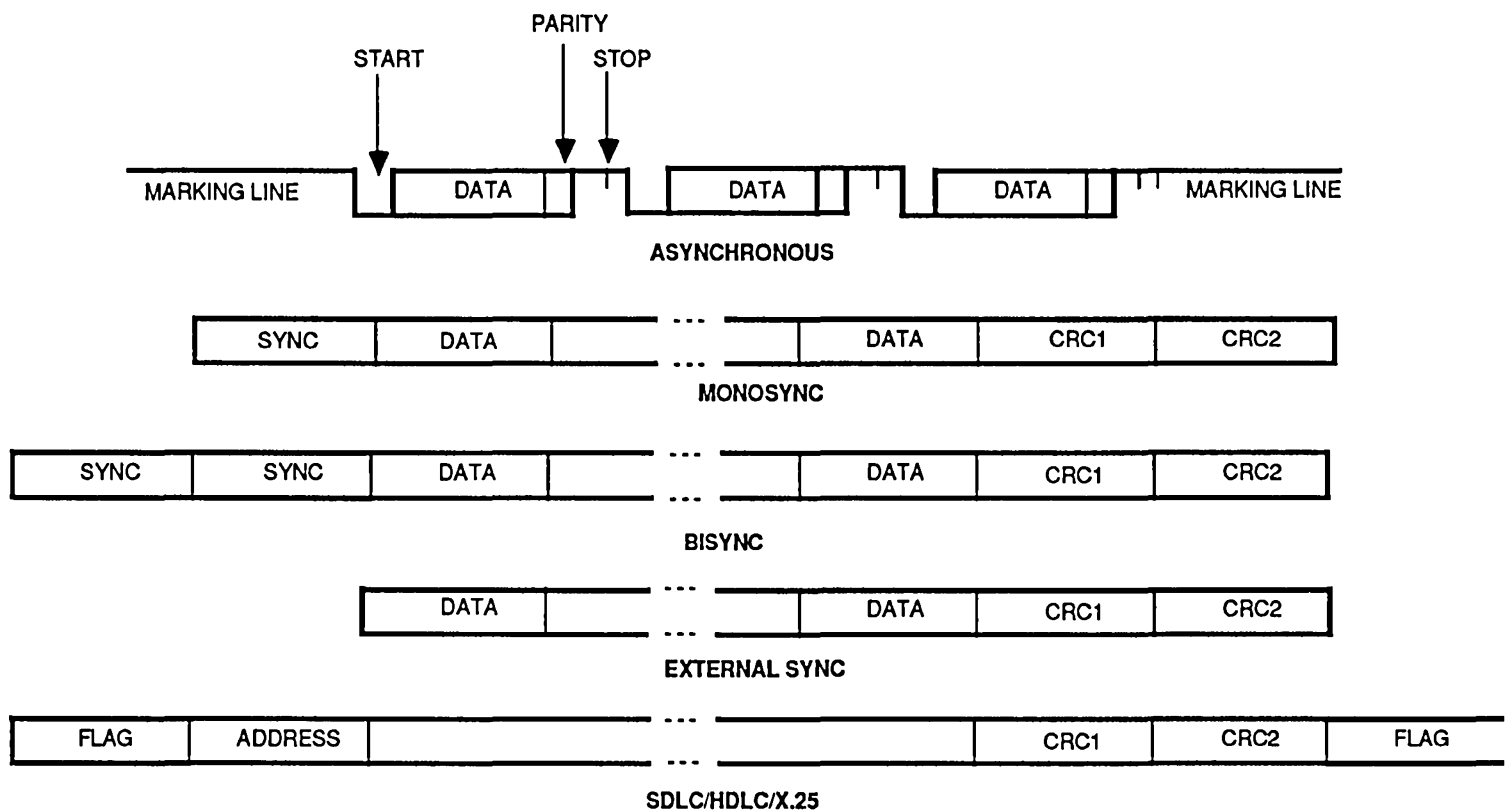
The NRZ, NRZI, or FM coding may be used in any 1x mode. The parity options available in asynchronous modes are available in synchronous modes.

The ESCC can be conveniently used under DMA control to provide high-speed reception or transmission. In reception, for example, the ESCC can

interrupt the CPU when the first character of a message is received. The CPU then enables the DMA to

transfer the message to memory. The ESCC then issues an end-of-frame interrupt and the CPU can check the status of the received message.

FIGURE 1. ESCC PROTOCOLS



The CPU is thereby freed for other service while the message is being received. The CPU may also enable the DMA first and have the ESCC interrupt only on end-of-frame. This procedure allows all data to be transferred via the DMA.

SDLC LOOP MODE

The ESCC supports SDLC loop mode in addition to normal SDLC. In an SDLC loop, there is a primary controller station that manages the message traffic flow on the loop and any number of secondary stations. In SDLC loop mode, the ESCC performs the functions of a secondary station while an ESCC operating in regular SDLC mode can act as a controller (Figure 3).

A secondary station in an SDLC Loop is always listening to the messages being sent around the loop, and in fact must pass these messages to the rest of the loop by retransmitting them with a one-bit time delay. The secondary station can place its own message on the loop only at specific times. The controller signals that secondary stations may transmit messages by sending a special character, called an End Of Poll (EOP), around the loop. The EOP character is the bit pattern 11111110. Because of zero insertion during messages, this bit pattern is unique and easily recognized.

When a secondary station has a message to transmit and recognizes an EOP on the line, it changes the last binary 1 of the EOP to a 0 before transmission. This has the effect of turning the EOP into a flag sequence. The secondary station now places its message on the loop and terminates the message with an EOP. Any secondary stations, further down the loop with messages to transmit, can then append their messages to the message of the first secondary station without messages to send. The following stations merely echo the incoming messages and are prohibited from placing messages on the loop (except upon recognizing an EOP). The SDLC loop mode is a programmable option in the ESCC; NRZ, NRZI, and FM coding may all be used in SDLC Loop mode.

BAUD RATE GENERATOR

Each channel in the ESCC contains a programmable baud rate generator. Each generator consists of two 8-bit time constant registers that form a 16-bit time-constant, a 16-bit down counter, and a flip-flop on the output producing a square wave. On startup, the flip-flop on the output is set in a HIGH state, the value in the time-constant register is loaded into the counter, and the counter starts counting down. The output of the baud rate generator toggles upon reaching 0, the value in the time-constant register

process is repeated. The time constant may be changed at any time, but the new value does not take effect until the next load of the counter.

The output of the baud rate generator may be used as either the transmit clock, the receive clock, or both. It can also drive the digital phase-locked loop (see next section).

If the receive clock or transmit clock is not programmed to come from the -TRxC pin, the output of the baud rate generator may be echoed out via the -TRxC pin.

The following formula relates the time constant to the baud rate (the baud rate is in bits/second and BR clock period is in seconds):

$$\text{baud rate} = \frac{1}{2 (\text{time constant} + 2) \times (\text{BR clock period})}$$

DIGITAL PHASE-LOCKED LOOP

The ESCC contains a digital phase-locked-loop (DPLL) to recover clock information from a data stream with NRZI or FM encoding. The DPLL is driven by a clock that is nominally 32 (NRZI) or 16 (FM) times the data rate. The DPLL uses this clock, along with the data stream, to construct a clock for the data. This clock may then be used as the ESCC receive clock, the transmit clock, or both.

FIGURE 2. DETECTING 5- OR 7-BIT SYNCHRONOUS CHARACTERS

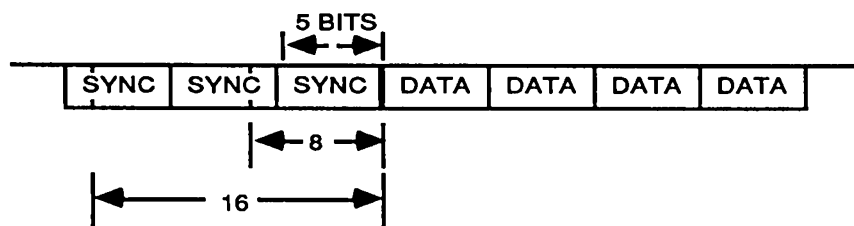
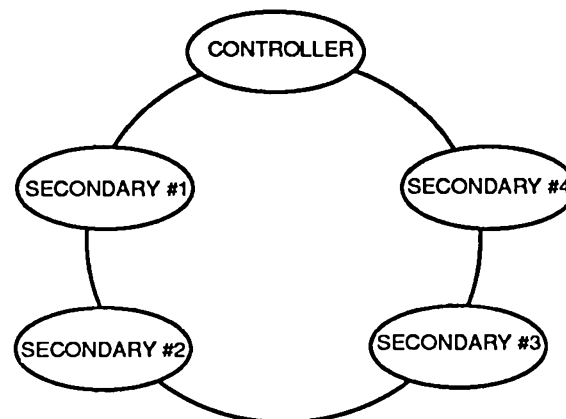


FIGURE 3. AN SDLC LOOP



For NRZI encoding, the DPLL counts the 32x clock to create nominal bit times. As the 32x clock is counted, the DPLL is searching the incoming data stream for edges (either 1 to 0 or 0 to 1). Whenever an edge is de-tected, the DPLL makes a count adjustment (during the next counting cycle), producing a terminal count closer to the center of the bit cell.

For FM encoding, the DPLL still counts from 0 to 31, but with a cycle corresponding to two bit times. When the DPLL is locked, the clock edges in the data stream should occur between counts 15 and 16, and between counts 31 and 0. The DPLL looks for edges only during a time centered on the 15 to 16 counting transition.

The 32x clock for the DPLL can be programmed to come from either the -RTxC input or the output of the baud rate generator. The DPLL output may be programmed to be echoed out of the ESCC via the -TRxC pin (if this pin is not being used as an input).

DATA ENCODING

The ESCC may be programmed to encode and decode the serial data in four different ways (Figure 4). In NRZ encoding, a 1 is represented by a HIGH level and a 0 is represented by a LOW level. In NRZI encoding, a 1 is represented by no change in level and a 0 is represented by a change in level.

In FM1 (more properly, bi-phase mark), a transition occurs at the beginning of every bit cell. A 1 is represented by

an additional transition at the center of the bit cell and a 0 is represented by no additional transition at the center of the bit cell. In FM0 (bi-phase space), a transition occurs at the beginning of every bit cell. A 0 is represented by an additional transition at the center of the bit cell, and a 1 is represented by no additional transition at the center of the bit cell.

In addition to these four methods, the ESCC can be used to decode Manchester (bi-phase level) data by using the DPLL in the FM mode and programming the receiver for NRZ data. Manchester encoding always produces a transition at the center of the bit cell. If the transition is 0 to 1, the bit is a 0. If the transition is 1 to 0, the bit is a 1.

AUTO ECHO AND LOCAL LOOPBACK

The ESCC is capable of automatically echoing everything it receives. This feature is useful mainly in Asynchronous modes, but works in Synchronous and SDLC modes as well. In Auto Echo mode, TxD is RxD. Auto Echo mode can be used with NRZI or FM encoding with no additional delay, because the data stream is not decoded before retransmission. In Auto Echo mode, the -CTS input is ignored as a transmitter enable (although transitions on this input can still cause interrupts if programmed to do so). In this mode, the transmitter is actually bypassed and the programmer is responsible for disabling transmitter interrupts and Wait/Request on transmit.

The ESCC is also capable of local loopback. In this mode TxD is RxD, just as in auto echo mode. However, in local loopback mode, the internal transmit data is tied to the internal receive data and RxD is ignored (except to be echoed out via TxD). The -CTS and -DCD inputs are also ignored as transmit and receive enables. However, transitions on these inputs can still cause interrupts. Local loopback works in asynchronous, synchronous, and SDLC modes with NRZ, NRZI, or FM coding of the data stream.

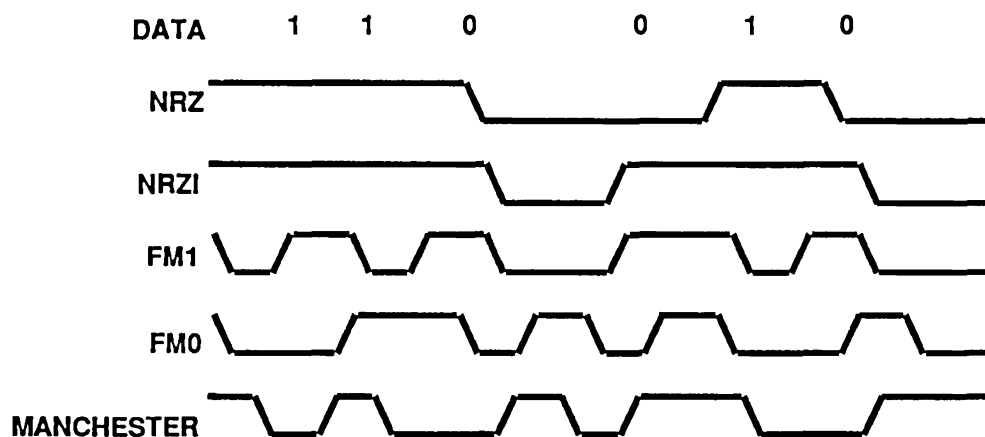
I/O INTERFACE CAPABILITIES

The ESCC offers the choice of polling, interrupt (vectored or nonvectored), and block transfer modes to transfer data, status, and control information to and from the CPU. The block transfer mode can be implemented under CPU or DMA control.

POLLING

All interrupts are disabled. Three status registers in the ESCC are automatically updated whenever any function is performed. For example, end-of-frame in SDLC mode sets a bit in one of these status registers. The idea behind polling is for the CPU to periodically read a status register until the register contents indicate the need for data to be transferred. Only one register needs to be read; depending on its contents, the CPU either writes data, reads data, or continues. Two bits in the register indicate the need for data transfer.

FIGURE 4. DATA ENCODING METHODS



An alternative is a poll of the Interrupt Pending register to determine the source of an interrupt. The status for both channels resides in one register.

INTERRUPTS

When an ESCC responds to an Interrupt Acknowledge signal (-INTACK) from the CPU, an interrupt vector may be placed on the data bus. This vector is written in Write Register 2 (WR2) and may be read in Read Register 2A (RR2A) or Read Register 2B (RR2B) (Figures 8).

To speed interrupt response time, the ESCC can modify three bits in this vector to indicate status. If the vector is read in Channel A, status is never included; if it is read in Channel B, status is always included.

Each of the six sources of interrupts in the ESCC (Transmit, Receive, and External/Status interrupts in both channels) has three bits associated with the interrupt source: Interrupt Pending (IP), Interrupt Under Service (IUS), and Interrupt Enable (IE). Operation of the IE bit is straightforward. If the IE bit is set for a given interrupt source, that source can request interrupts. The exception is when the MIE (Master Interrupt Enable) bit in WR9 is reset and no interrupts may be requested. The IE bits are write only.

The other two bits are related to the interrupt priority chain (Figure 5). As a microprocessor peripheral, the ESCC may request an interrupt only when no higher priority device is requesting one; e.g., when IEI is high. If the device in question requests an interrupt, it pulls

down -INT . The CPU then responds with -INTACK , and the interrupting device places the vector on the data bus.

In the ESCC, the IP bit signals a need for interrupt servicing. When an IP bit is 1 and the IEI input is high, the INT output is pulled low, requesting an interrupt. In the ESCC, if the IE bit is not set by enabling interrupts, then the IP for that source can never be set. The IP bits are readable in RR3A.

The IUS bits signal that an interrupt request is being serviced. If an IUS is set, all interrupt sources of lower priority in the ESCC and external to the ESCC are prevented from requesting interrupts. The internal interrupt sources are inhibited by the state of the internal daisy chain, while lower priority devices are inhibited by the IEO output of the ESCC being pulled LOW and propagated to subsequent peripherals. An IUS bit is set during an interrupt acknowledge cycle if there are no higher priority devices requesting interrupts.

There are three types of interrupts: transmit, receive, and external/status. Each interrupt type is enabled under program control with Channel A having higher priority than Channel B, and with receive, transmit, and external/status interrupts prioritized in that order within each channel. When the transmit interrupt is enabled, the CPU is interrupted when the transmit buffer becomes empty. (This implies that the transmitter must have had a data character written into it so that it can become empty.) When enabled, the

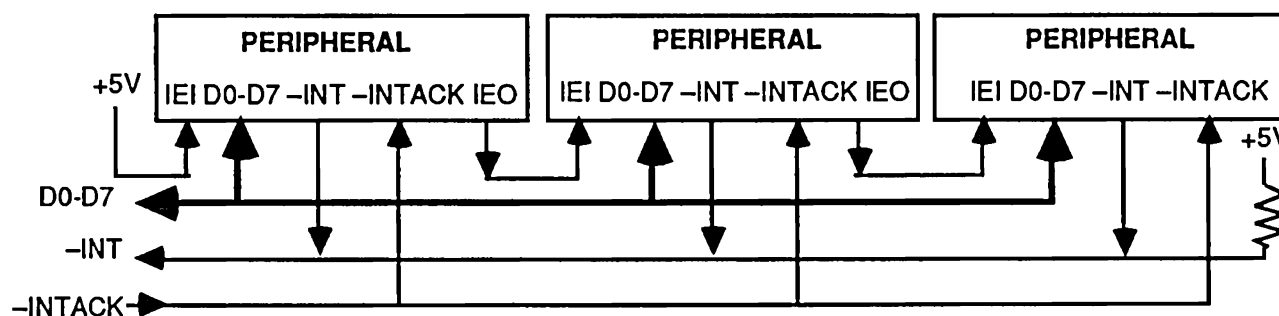
receiver can interrupt the CPU in one of three ways:

- On first receive character or special receive condition
- On all receive characters or special receive condition
- On special receive condition only.

Interrupt on first character or special condition and interrupt on special condition only are typically used with the Block Transfer mode. A special receive condition is one of the following: receiver overrun, framing error in Asynchronous mode, end-of-frame in SDLC mode, and optionally, a parity error. The special receive condition interrupt is different from an ordinary receive character interrupt only in that the status is placed in the vector during the Interrupt Acknowledge cycle. In interrupt on first receive character, an interrupt can occur from special receive conditions any time after the first receive character interrupt.

The main function of the external/status interrupt is to monitor the signal transitions of the -CTS , -CCD , and -SYNC pins; however, an external/status interrupt is also caused by a transmit underrun condition, or a zero count in the baud rate generator, or by the detection of a break (asynchronous mode), abort (SDLC mode) or EOP (SDLC loop mode) sequence in the data stream.

FIGURE 5. INTERRUPT SCHEDULE



The interrupt caused by the abort or EOP has a special feature allowing the ESCC to interrupt when the abort or EOP sequence is detected or terminated. This feature facilitates the proper termination of the current message, correct initialization of the next message, and the accurate timing of the Abort condition in external logic in SDLC mode. In SDLC Loop mode, this feature allows secondary stations to recognize the need of the primary station to regain

control of the loop during a poll sequence.

CPU/DMA BLOCK TRANSFER

The ESCC provides a Block Transfer mode to accommodate CPU block transfer functions and DMA controllers. The Block Transfer mode uses the Wait/Request output in conjunction with the Wait/Request bits in WR1. The Wait/Request output can be defined under software control as a Wait line in the

CPU Block Transfer mode or as a Request line in the DMA Block Transfer mode.

To a DMA controller, the ESCC Request output indicates that the ESCC is ready to transfer data to or from memory. To the CPU, the Wait line indicates that the ESCC is not ready to transfer data, thereby requesting that the CPU extend the I/O cycle. The DTR/Request line allows full-duplex operation under DMA control.

PROGRAMMING

The ESCC contains 13 write registers in each channel that are programmed by the system separately to configure the functional personality of the channels.

In the ESCC, register addressing is direct for the data registers only, which are selected by a high on the D/-C pin. In all other cases (with the exception of WR0 and RR0), programming the write registers requires two write operations and reading the read registers requires both a write and a read operation. The first write is to WR0 and contains three bits that point to the selected register. The second write is the actual control word for the selected register, and if the second operation is read, the selected read register is accessed. All of the registers in the ESCC, including the data registers, may be accessed in this fashion. The pointer bits are automatically cleared after the read or write operation so that WR0 (or RR0) is addressed again.

The system program first issues a series of commands to initialize the basic mode of operation. This is followed by other commands to qualify conditions within the selected mode. For example, the asynchronous mode, character length, clock rate, number of stop bits, and even or odd parity might be set first. Then the interrupt mode would be set, and, finally, receiver or transmitter enable.

READ REGISTERS

The ESCC contains ten read registers (eleven counting receive buffer RR8) in each channel. Four of these may be read to obtain status information (RR0, RR1, RR10, and RR15). Two registers (RR12 and RR13) may be read to learn the baud rate generator time constant. The RR2 contains either the unmodified interrupt vector (Channel A) or the vector modified by status information (Channel B). Both RR7 and RR6 read the DMA FIFO. The RR3 contains the Interrupt Pending (IP) bits (Channel A).

Figures 6 through 13 and Figure 31 show the formats for each read register.

The status bits of RR0 and RR1 are carefully grouped to simplify status monitoring; e.g., when the interrupt vector indicates a special receive condition interrupt, all the appropriate error bits can be read from a single register (RR1).

WRITE REGISTERS

The ESCC contains 13 write registers (14 counting WR8, the transmit buffer) in each channel. These write registers are programmed separately to configure the functional personality of the channels. In addition, there are two registers (WR2 and WR9) shared by the two channels that may be accessed through either of them; WR2 contains the interrupt vector for both channels, while WR9 contains the interrupt control bits. Figures 14 through 28 and Figure 31 show the format of each write register.

TIMING

The ESCC generates internal control signals from -WR and -RD that are related to PCLK. Since PCLK has no phase relationship with -WR and -RD, the circuitry generating these internal control signals must provide time for metastable conditions to disappear. This gives rise to a recovery time related to PCLK. The recovery time applies only between bus transactions involving the ESCC. The recovery time required for proper operation is specified from the rising edge of -WR or -RD in the first transaction involving the SCC, to the falling edge of WR or RD in the second transaction involving the ESCC. This

time must be at least four PCLK cycles plus 200 ns.

READ CYCLE TIMING

Figure 32 illustrates Read cycle timing. Addresses on A/-B and D/-C and the status on -INTACK must remain stable through the cycle. If -CE falls after -RD falls or if it rises before -RD rises, the effective -RD is shortened.

WRITE CYCLE TIMING

Figure 33 illustrates Write cycle timing. Addresses on A/-B and D/-C and the status on -INTACK must remain stable throughout the cycle. If -CE falls after -WR falls, or if it rises before -WR rises, the effective -WR is shortened.

INTERRUPT ACKNOWLEDGE CYCLE TIMING

Figure 34 illustrates Interrupt Acknowledge cycle timing. Between the time -INTACK goes low and the falling edge of -RD, the internal and external IEI/IEO daisy chains settle. If there is an interrupt pending in the ESCC and IEI is high when -RD falls, the Acknowledge cycle is intended for the ESCC. In this case, the ESCC may be programmed to respond to -RD low by placing its interrupt vector on D0-D7 and it then internally sets the appropriate Interrupt-Under-Service latch.

FIFO DETAIL

For a better understanding of details of the FIFO operation, refer to the block diagram in Figure 39.

ENABLE/DISABLE

This FIFO is implemented so that it is only enabled when Channel A register WR15 bit 2 is set and the ESCC is in the SDLC/HDLC mode, otherwise the status register contents bypass the FIFO and go directly to the bus interface (the FIFO pointer logic is reset either when disabled or via a channel or power-on reset). When the FIFO mode is disabled, the ESCC is completely downward-compatible with the HMOS VL8530. The FIFO mode is disabled on power-up (WR15 bit 2 is set to 0 on reset). The effects of backward com-

RR4 is an image of RR0, RR5 is an image of RR1, RR6 is an image of RR2, and RR7 is an image of RR3. For details of the added registers, refer to Figure 3. The status of the FIFO Enable signal can be obtained by reading Channel A RR15 bit 2. If the FIFO is enabled, the bit will be set to 1; otherwise, it will be reset. Channel B WR15 and RR15 behave exactly as in the VL8530 standard product.

READ OPERATION

When WR15 bit 2 is set and the FIFO is not empty, the next read to any of status register RR1 or the additional registers RR7 and RR6 will actually be from the FIFO. Reading status register RR1

causes one location of the FIFO to be emptied, so status should be read after reading the byte count, otherwise the count will be incorrect. Before the FIFO underflows, it is disabled. In this case, the multiplexer is switched to allow status to read directly from the status register, and reads from RR7 and RR6 will contain bits that are undefined. Bit 6 of RR7 (FIFO Data Available) can be used to determine if status data is coming from the FIFO or directly from the status register, since it is set to one whenever the FIFO is not empty.

Since not all status bits must be stored in the FIFO, the All Sent, Parity, and EOF bits will bypass the FIFO. The status bits sent through the FIFO will be Residue Bits (3), Overrun, and CRC Error.

The sequence for proper operation of the byte count and FIFO logic is to read the registers in the following order: RR7, RR6, and RR1 (reading RR6 is optional). Additional logic prevents the FIFO from being emptied by multiple reads from RR1. The read from RR7 latches the FIFO empty/full status bit (bit 6) and steers the status multiplexer to read from the ESCC megacell instead of the status FIFO (since the status FIFO is empty). The read from RR1 allows an entry to be read from the FIFO (if the FIFO was empty, logic is added to prevent a FIFO underflow condition).

WRITE OPERATION

When the end of an SDLC frame (EOF) has been received and the FIFO is enabled, the contents of the status and byte-count registers are loaded into the FIFO. The EOF signal is used to increment the FIFO. If the FIFO overflows, the MSB of RR7 (FIFO Overflow) is set to indicate the overflow. This bit and the FIFO control logic is reset by disabling and re-enabling the FIFO control bit (WR15 bit 2). For details of FIFO control timing during an SDLC frame, refer to Figure 40.

BYTE COUNTER DETAIL

The 14-bit byte counter allows for packets up to 16K bytes to be received. For a better understanding of its operation, refer to Figures 39 and 40.

ENABLE

The byte counter is enabled in the SDLC/HDLC mode.

RESET

The byte counter is reset whenever an SDLC flag character is received. The reset is timed so that the contents of the byte counter are successfully written into the FIFO.

INCREMENT

The byte counter is incremented by writes to the data FIFO. The counter represents the number of bytes received by the ESCC, rather than the number of bytes transferred from the ESCC. (These counts may differ by up to the number of bytes in the receive data FIFO contained in the ESCC.)

FIGURE 6. READ REGISTER 0

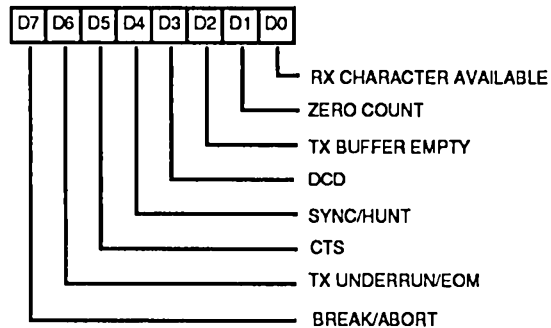


FIGURE 10. READ REGISTER 10

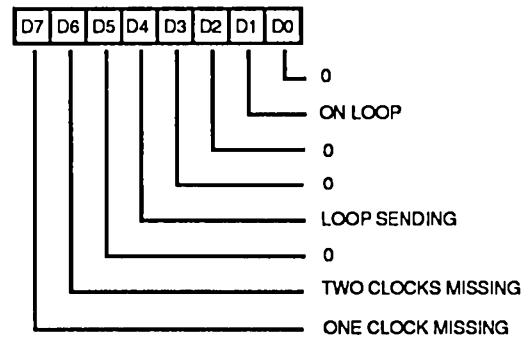


FIGURE 7. READ REGISTER 1

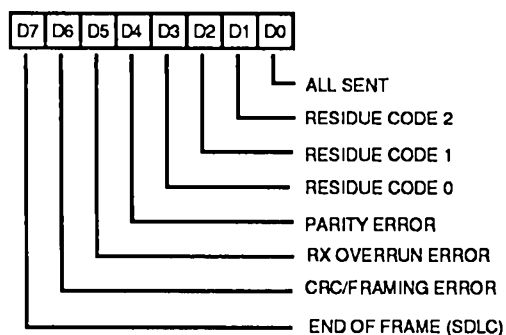


FIGURE 11. READ REGISTER 12

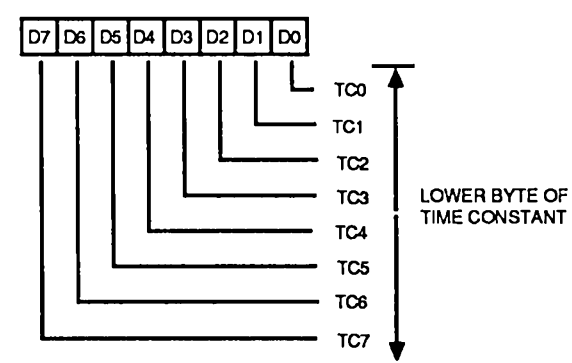


FIGURE 8. READ REGISTER 2

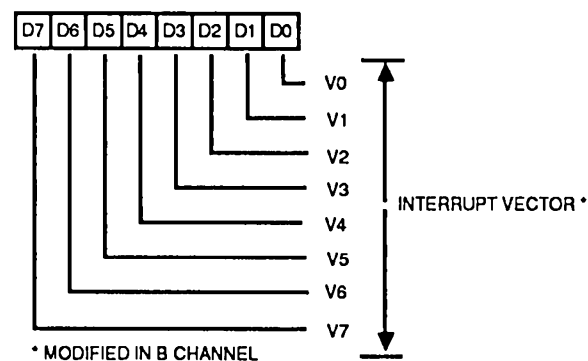


FIGURE 12. READ REGISTER 13

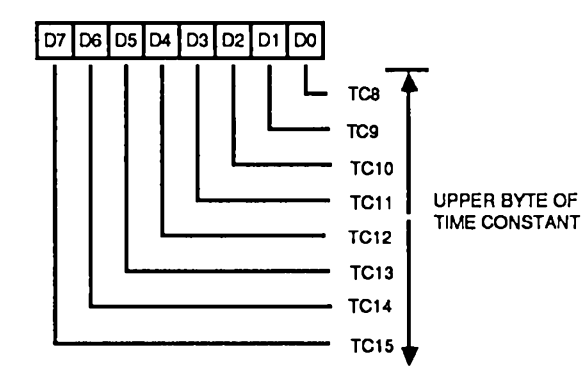


FIGURE 9. READ REGISTER 3

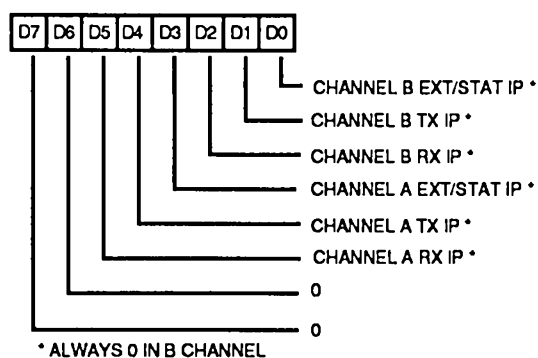


FIGURE 13. READ REGISTER 15

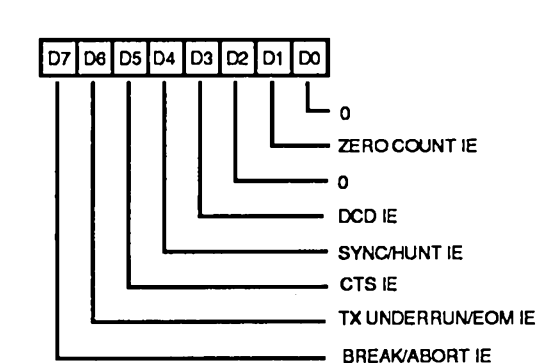


FIGURE 14. WRITE REGISTER 0

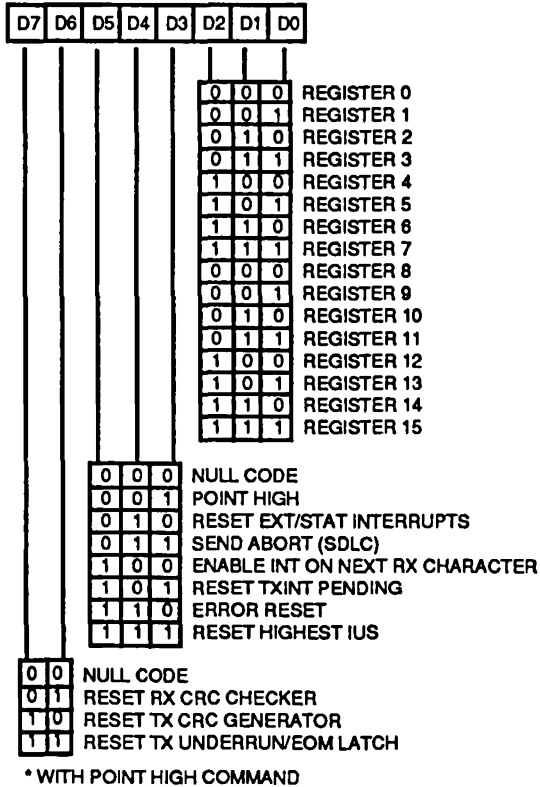


FIGURE 15. WRITE REGISTER 1

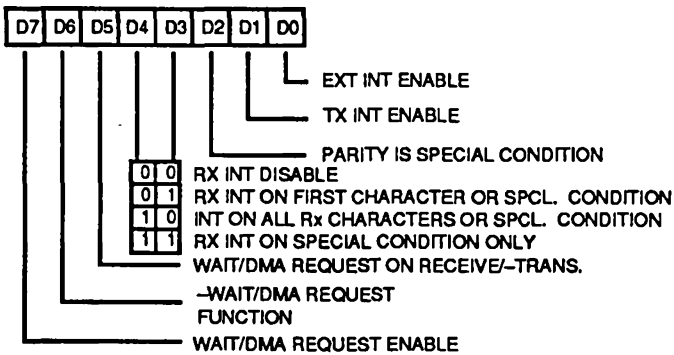


FIGURE 16. WRITE REGISTER 2

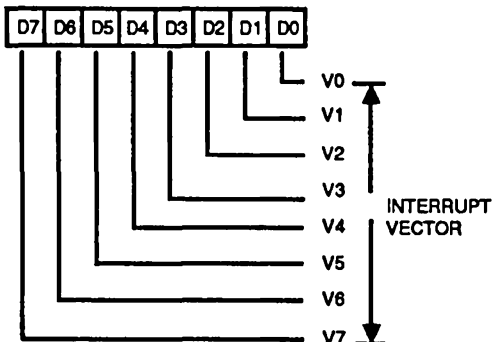


FIGURE 17. WRITE REGISTER 3

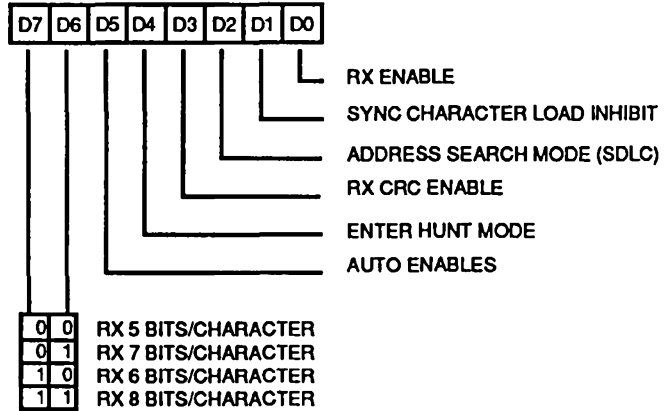


FIGURE 18. WRITE REGISTER 4

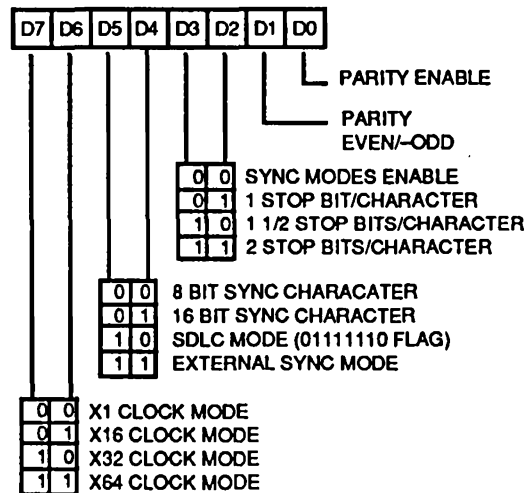


FIGURE 19. WRITE REGISTER 5

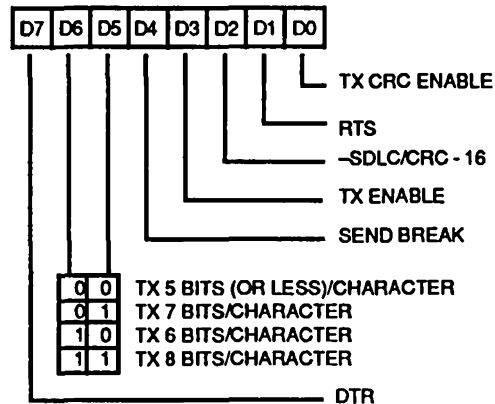


FIGURE 20. WRITE REGISTER 6

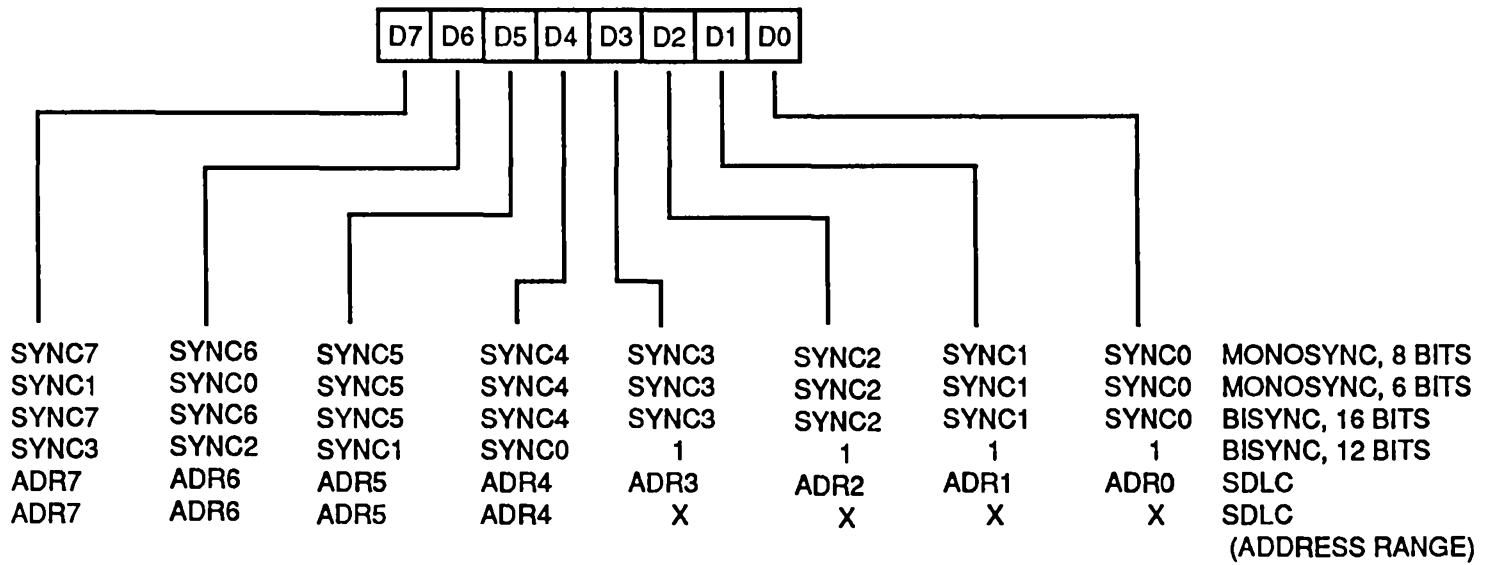


FIGURE 21. WRITE REGISTER 7

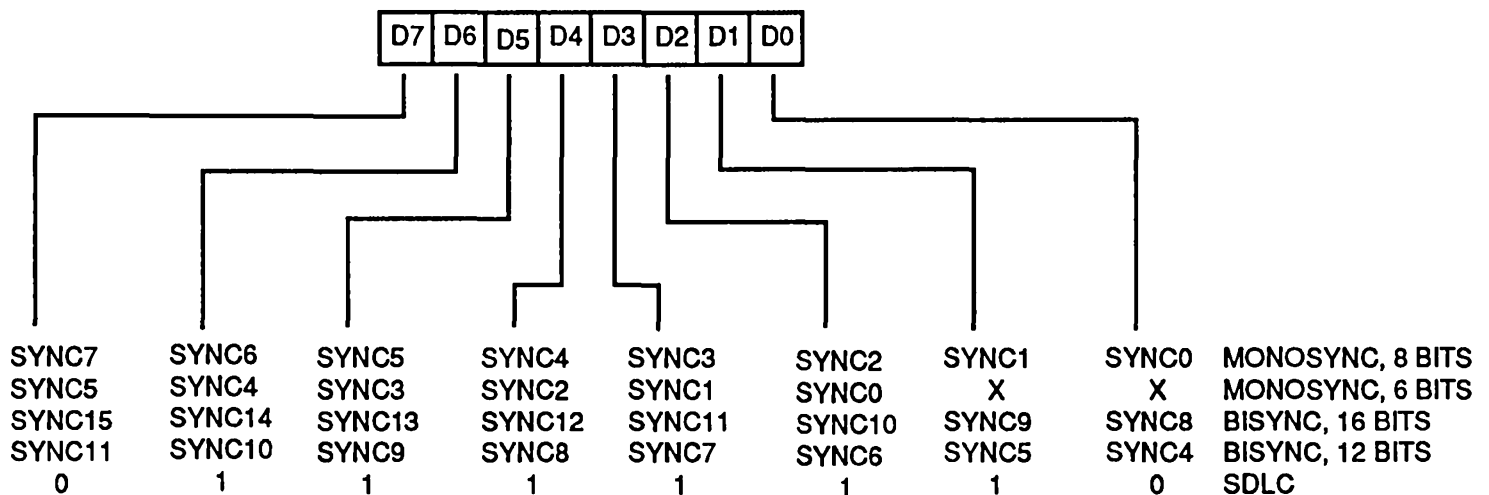




FIGURE 22. WRITE REGISTER 9

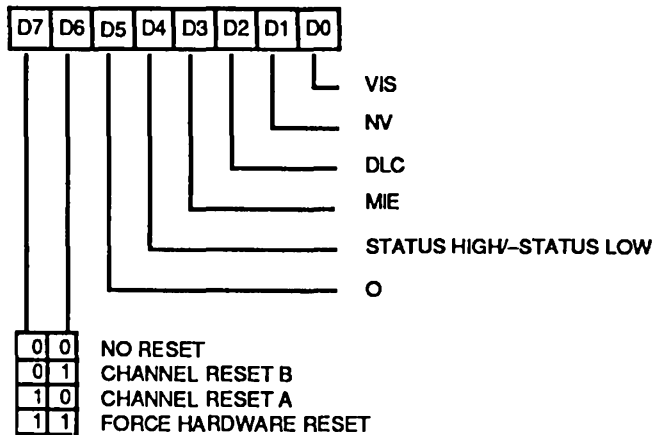


FIGURE 23. WRITE REGISTER 10

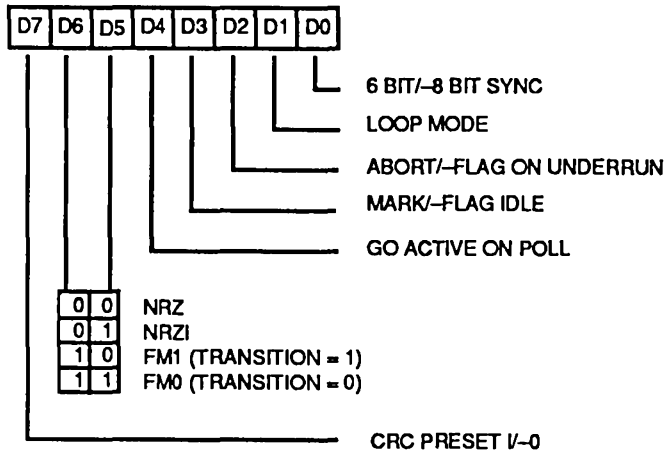


FIGURE 24. WRITE REGISTER 11

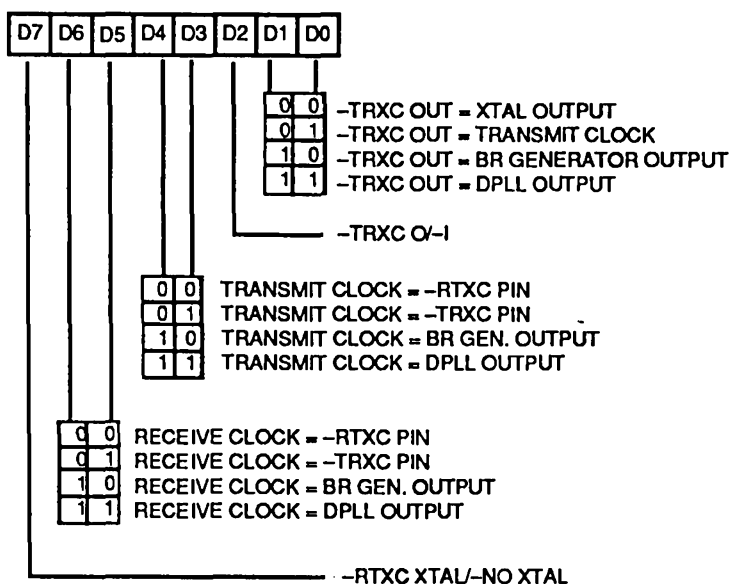


FIGURE 25. WRITE REGISTER 12

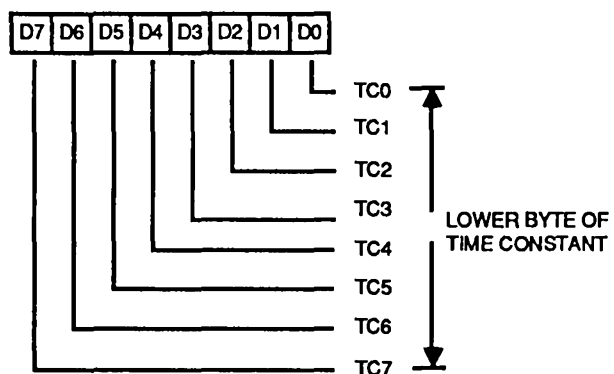


FIGURE 26. WRITE REGISTER 13

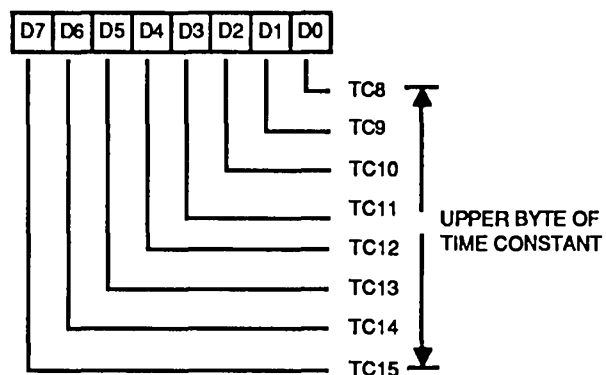


FIGURE 27. WRITE REGISTER 14

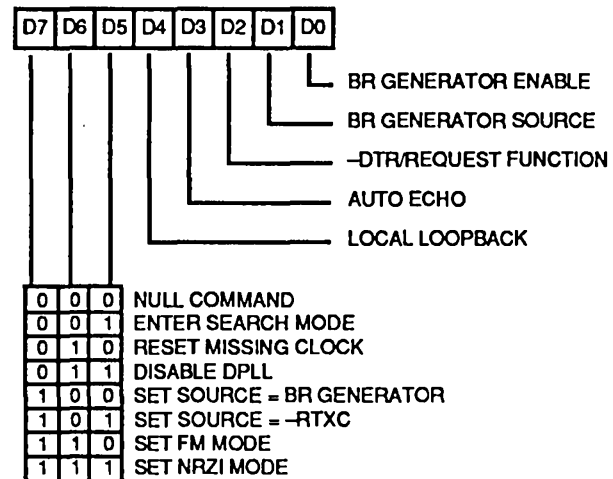


FIGURE 28. WRITE REGISTER 15

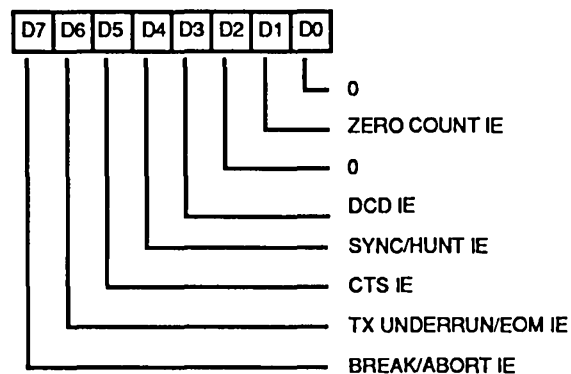


FIGURE 29. ESCC STATUS REGISTER

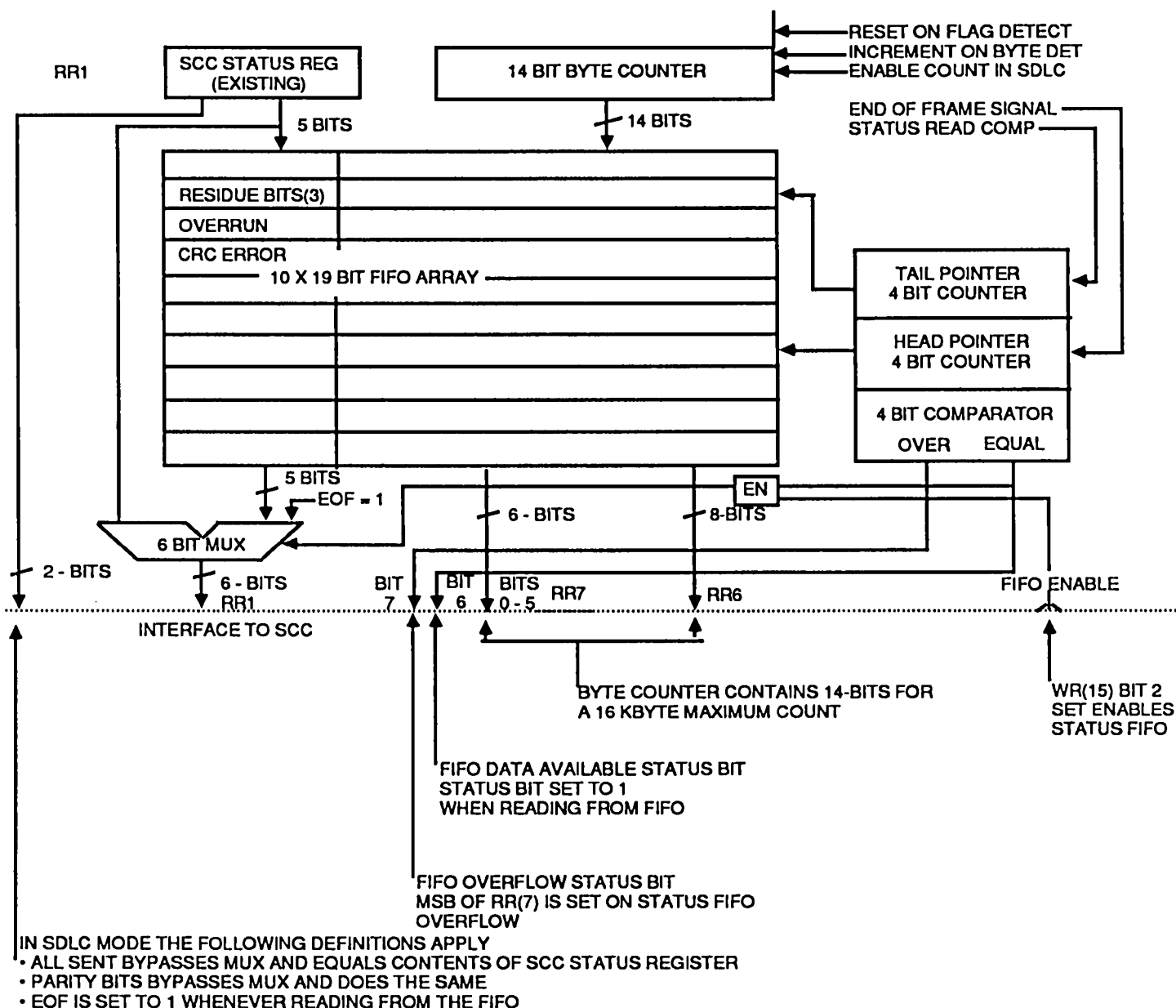


FIGURE 30. SDLC BYTE COUNTING DETAIL

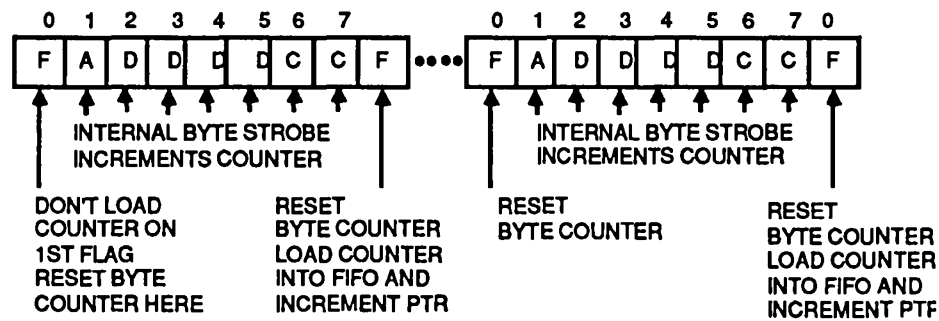


FIGURE 31. ESCC REGISTERS

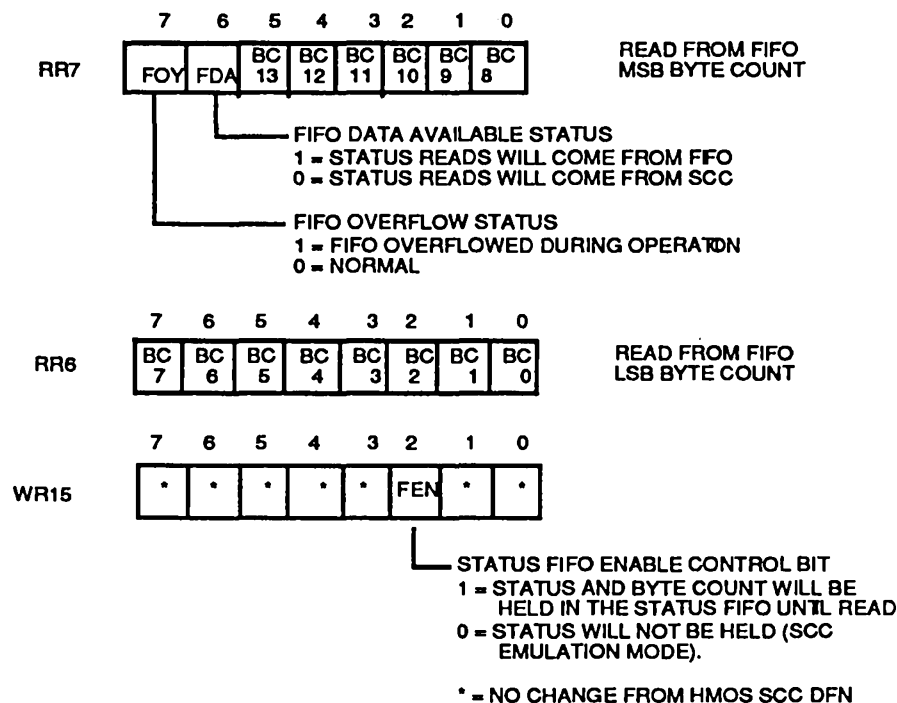


FIGURE 32. READ CYCLE TIMING

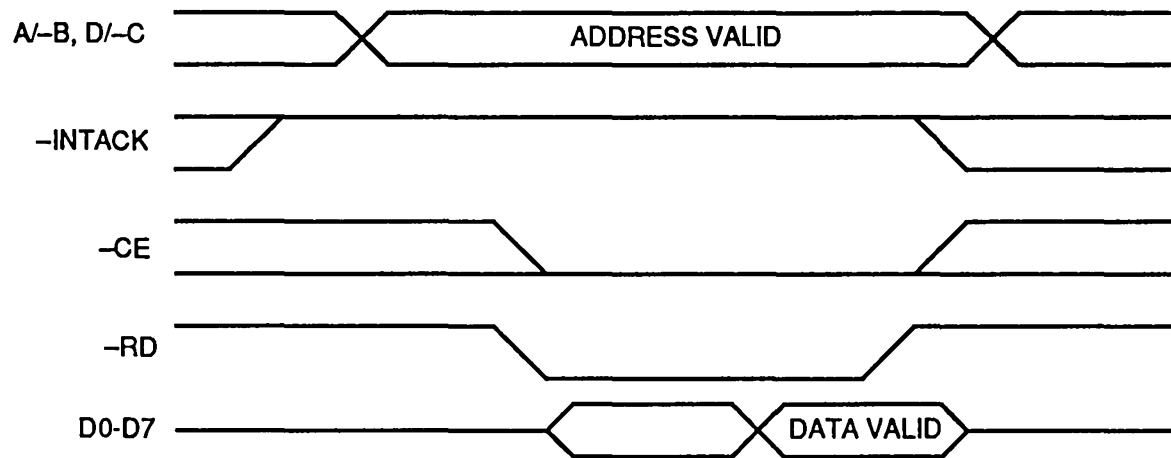


FIGURE 33. WRITE CYCLE TIMING

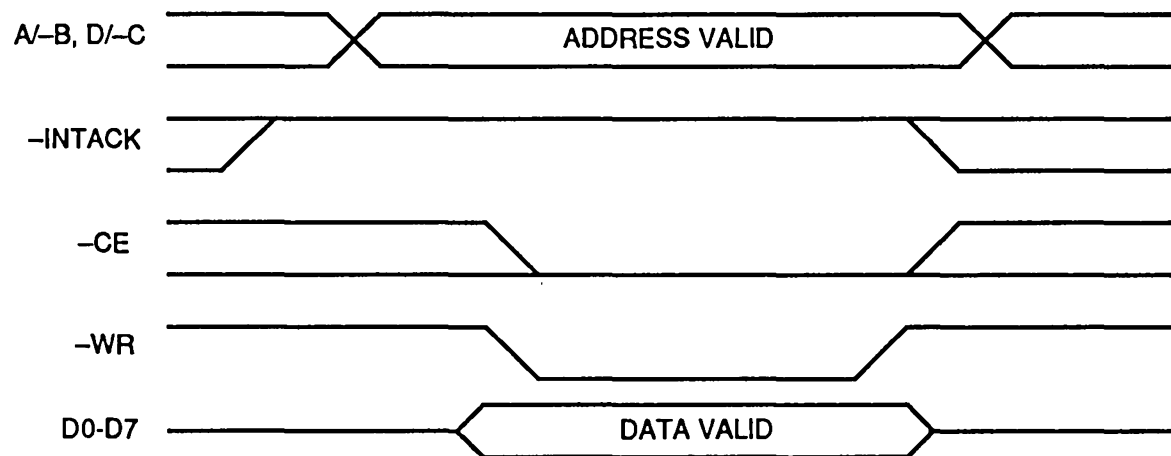


FIGURE 34. INTERRUPT ACKNOWLEDGE CYCLE TIMING

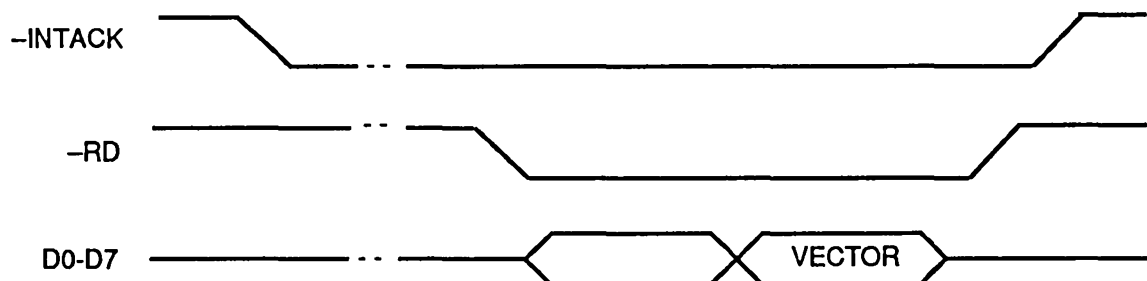


FIGURE 35. READ AND WRITE TIMING (SEE TABLE 1)

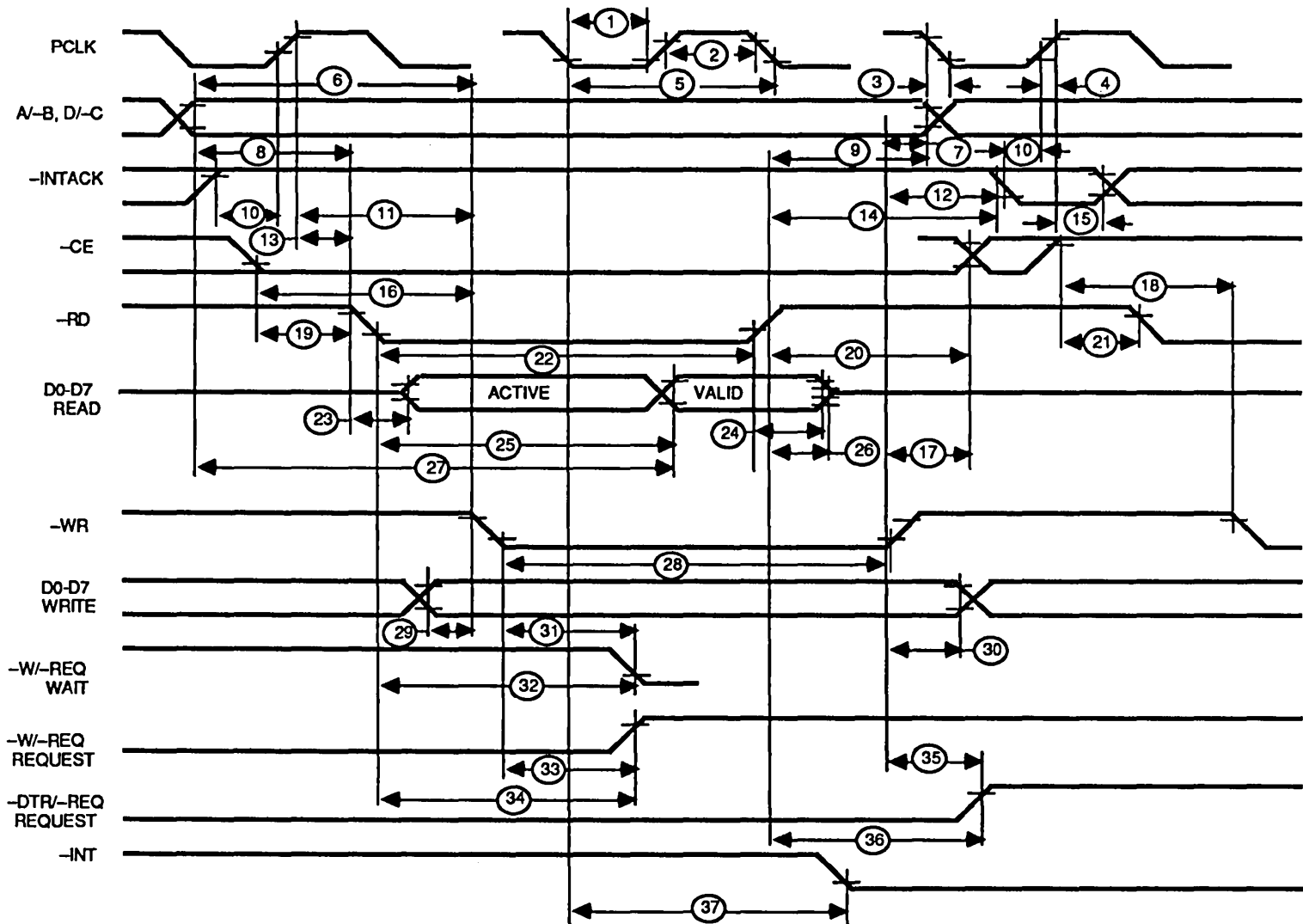


FIGURE 36. RESET TIMING (SEE TABLE 1)

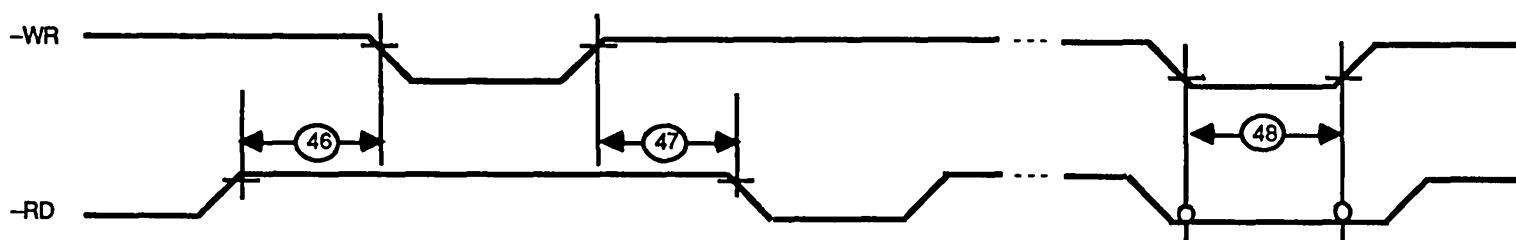


FIGURE 37. CYCLE TIMING (SEE TABLE 1)

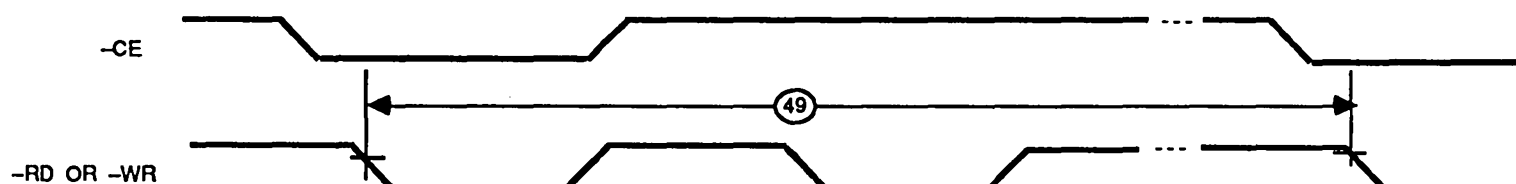


TABLE 1. READ AND WRITE TIMING CHARACTERISTICS: TA = 0°C TO +70°C

No.	Symbol	Parameter	8 MHz		10 MHz		12 MHz		Notes
			Min	Max	Min	Max	Min	Max	
1	TwPCI	PCLK Low Width	50	1000	40	1000			
2	TwPCh	PCLK High Width	50	1000	40	1000			
3	TfPC	PCLK Fall Time		10		10			
4	TrPC	PCLK Rise Time		15		10			
5	TcPC	PCLK Cycle Time	125	2000	100	2000			
6	TsA(WR)	Address to –WR Setup Time	70		50				
7	ThA(WR)	Address to –WR Hold Time	0		0				
8	TsA(RD)	Address to –RD Setup Time	70		50				
9	ThA(RD)	Address to –RD Hold Time	0		0				
10	TsIA(PC)	–INTACK to PCLK Setup Time	20		20				
11	TsIAi(WR)	–INTACK to –WR Setup Time	145		130				2
12	ThIA(WR)	–INTACK to –WR Hold Time	0		0				
13	TsIAi(RD)	–INTACK to –RD Setup Time	145		130				2
14	ThIA(RD)	–INTACK to –RD Hold Time	0		0				
15	ThIA(PC)	–INTACK to PCLK Hold Time	40		30				
16	TsCE1(WR)	–CE Low to –WR Setup Time	0		0				
17	ThCE(WR)	–CE to –WR Hold Time	0		0				
18	TsCEh(WR)	–CE High to –WR Setup Time	60		50				2
19	TsCE1(RD)	–CE Low to –RD Setup Time	0		0				2
20	ThCE(RD)	–CE to –RD Hold Time	0		0				2
21	TsCEh(RD)	–CE High to –RD Setup Time	60		50				2
22	TwRD1	–RD Low Width	150		125				
23	TdRD(DRA)	–RD to Read Data Active Delay	0		0				
24	TdRDrd(DR)	–RD to Read Data Not Valid Delay	0		0				
25	TdRDf(DR)	–RD to Read Data Valid Delay		140		120			
26	TdRD(DRz)	–RD to Read Data Float Delay		40		35			3
27	TdA(DR)	Address Required Valid to Read Data Valid Delay		220		180			
28	TwWR1	–WR Low Width	150		125				
29	TsDW(WR)	Write Data to –WR Setup Time	10		10				
30	ThDW(WR)	Write Data to –WR Hold Time	0		0				
31	TdWR(W)	–WR to Wait Valid Delay		170		160			5
32	TdRD(W)	–RD to Wait Valid Delay		170		160			5
33	TdWRf(REQ)	–WR to –W/–REQ Not Valid Delay		170		160			
34	TdRDf(REQ)	–RD to –W/–REQ Not Valid Delay		170		160			
35	TdWRr(REQ)	–WR to –DTR/–REQ Not Valid Delay		4TcPC		4TcPC			
36	TdRDrd(REQ)	–RD to –DTR/–REQ Not Valid Delay		4TcPC		4TcPC			
37	TdPC(INT)	PCLK to –INT Valid Delay		500		500			5
38	TdIAi(RD)	–INTACK to –RD (Acknowledge) Delay	150		125				6
39	TwRDA	–RD (Acknowledge) Width	150		125				
40	TdRDA(DR)	–RD (Ack.) to Read Data Valid Delay		140		120			
41	TsIEI(RDA)	IEI to –RD (Acknowledge) Setup Time	95		95				
42	ThIEI(RDA)	IEI to –RD (Acknowledge) Hold Time	0		0				
43	TdIEI(IEO)	IEI to IEO Delay Time		95		90			
44	TdPC(IEO)	PCLK to IEO Delay		200		175			
45	TdRDA(INT)	–RD to –INT Inactive Delay		500		500			4
46	TdRD(WRQ)	–RD to –WR Delay for No Reset	15		15				
47	TdWRQ(RD)	–WR to –RD Delay for No Reset	15		15				
48	TwRES	–WR and –RD Coincident Low for Reset	150		100				
49	Trc	Valid Access Recovery Time	4TcPC		4TcPC				

Read and Write Timing Notes:

1. Units are in nanoseconds.
2. Parameter does not apply to Interrupt Acknowledge transactions.
3. Float delay is defined as the time required for a ± 0.5 V change at the output with a maximum dc load and minimum ac load.
4. Parameter applies only between transactions involving the ESCC.
5. Open-drain output, measured with open-drain test load.
6. Parameter is system-dependent. For any ESCC in the daisy chain, $TdIAi(RD)$ must be greater than the sum of $TdPC(IEO)$ for the highest priority device in the daisy chain, $TsIEI(RDA)$ for the ESCC, and $TdIEIf(IEO)$ for each device separating them in the daisy chain.

FIGURE 38. INTERRUPT ACKNOWLEDGE TIMING (SEE TABLE 1)

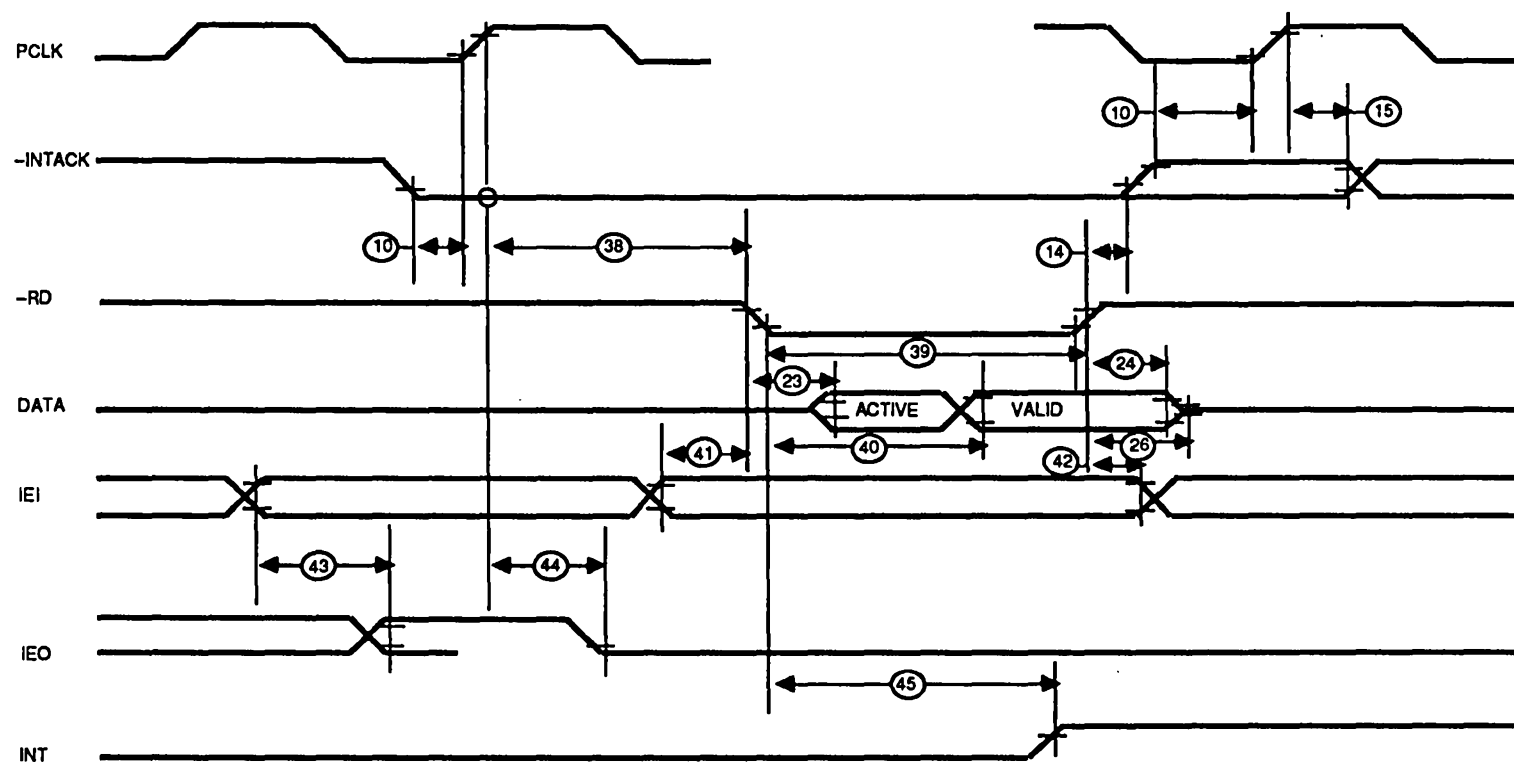


FIGURE 39. GENERAL TIMING (SEE TABLE 2)

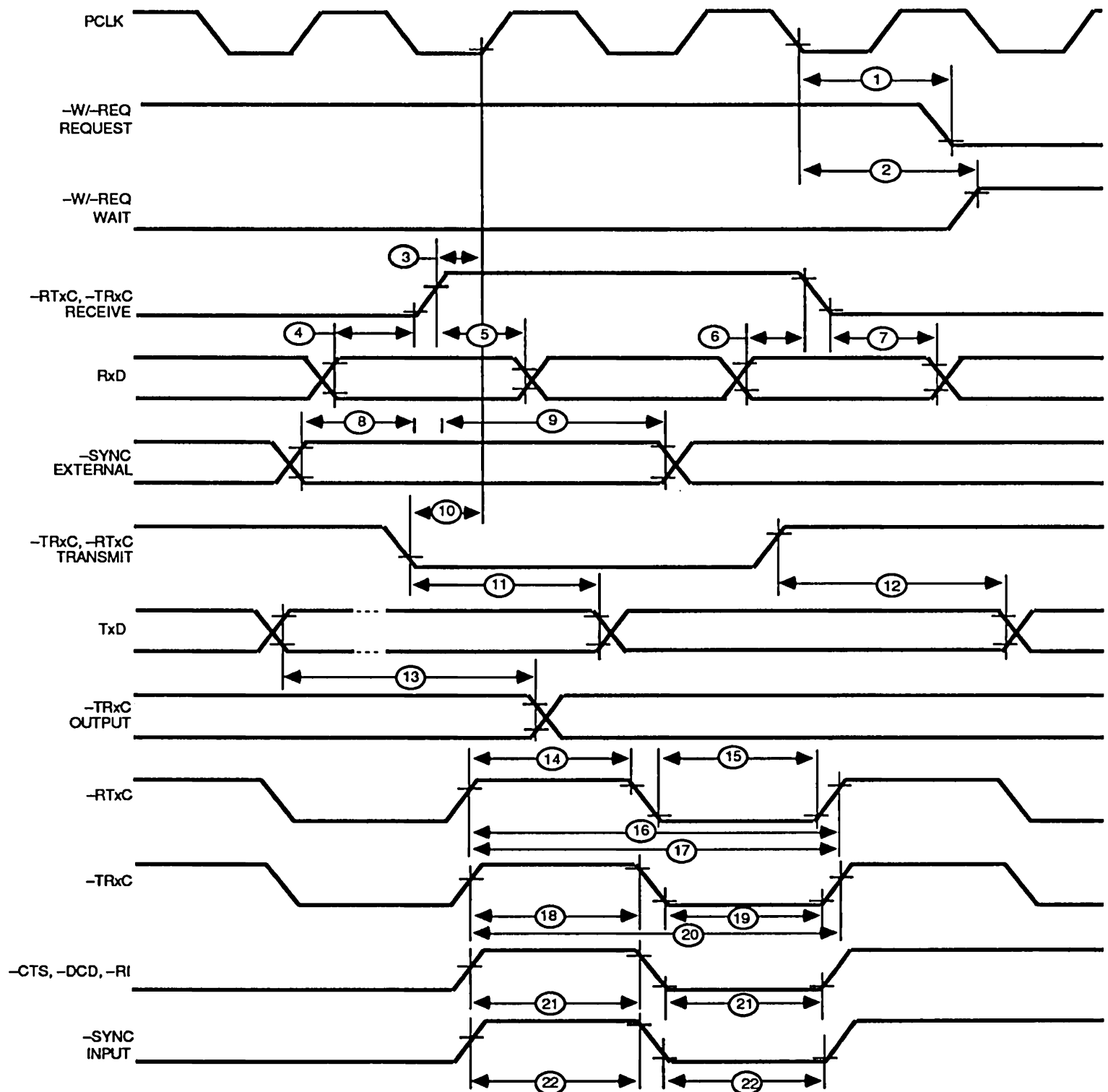


TABLE 2. GENERAL TIMING

No.	Symbol	Parameter	8 MHz		10 MHz		12 MHz		Notes
			Min	Max	Min	Max	Min	Max	
1	TdPC(REQ)	PCLK to -W/-REQ Valid Delay		250		250			
2	TdPC(W)	PCLK to Wait Inactive Delay		350		350			
3	Ts RXC(PC)	-RxC to PCLK Setup Time (PCLK + 4 Case Only)	60	TwPCl	40	TwPCl			2,5
4	TsRXD(RXCr)	RxD to -RxC Setup Time (X1 Mode)		0		0			2
5	ThRXD(RXCr)	RxD to -RxC Hold Time (X1 Mode)		150		150			2
6	TsRXD(RXCf)	RxD to -RxC Setup Time (X1 Mode)		0		0			2,6
7	ThRXD(RXCf)	RxD to -RxC Hold Time (X1 Mode)		150		150			2,6
8	TsSY(RXC)	-SYNC to -RxC Setup Time		-200		-200			4,2
9	ThSY(RXC)	-SYNC to -RxC Hold Time	5TcPC		5TcPC				4,2
10	TsTXC(PC)	-TxC to PCLK Setup Time	0		0				3,5
11	TdTXCf(TXD)	-TxC to Tx D Delay (X1 Mode)		200		150			3
12	TdTXCr(TXD)	-TxC to Tx D Delay (X1 Mode)		200		150			3,5
13	TdTXD(TRX)	TxD to -TRxC Delay (Send Clk Echo)		200		200			
14	TwRTXh	-RTxC High Width	150		150				7
15	TwRTXI	-RTxC Low Width	150		150				7
16	TcRTX	-RTxC Cycle Time	500		400				7
17	TcRTXX	Crystal Oscillator Period	125	1000	100	1000			3
18	TwTRXh	-TRxC High Width	150		150				4,7
19	TwTRXI	-TRxC Low Width	150		150				4,7
20	TcTRX	-TRxC Cycle Time	500		400				4,7
21	TwEXT	-DCD or -CTS Pulse Width	200		200				
22	TwSY	-SYNC Pulse Width	200		200				

TABLE 3. SYSTEM TIMING

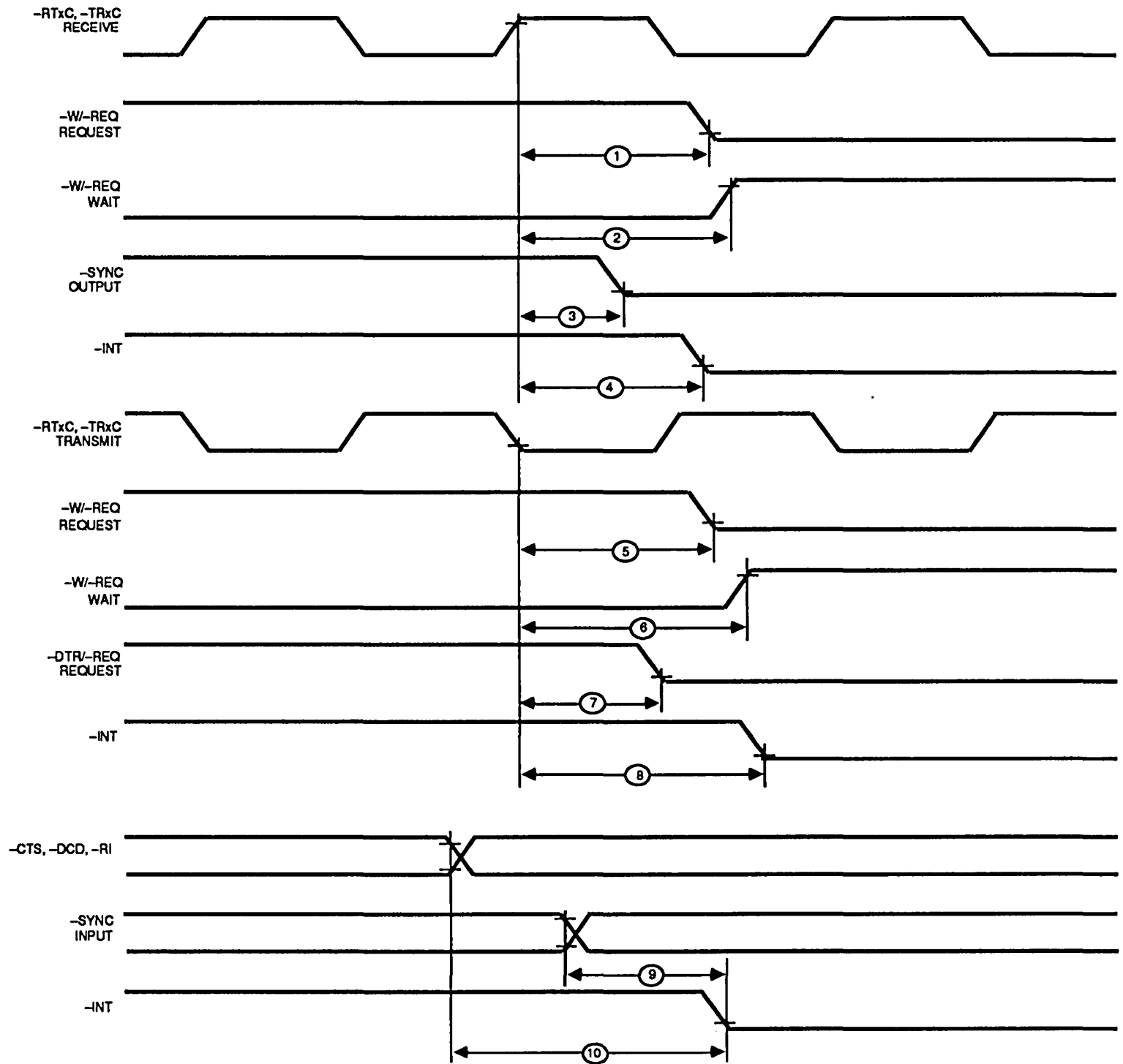
No.	Symbol	Parameter	8 MHz		10 MHz		12 MHz		Notes
			Min	Max	Min	Max	Min	Max	
1	TdRXC(REQ)	-RxC to -W/-REQ Valid Delay	8	12	8	12			2
2	TdRXC(W)	-RxC to Wait Inactive Delay	8	14	8	14			1,2
3	TdRXC(SY)	-RxC to -SYNC Valid Delay	4	7	4	7			2
4	TdRXC(INT)	-RxC to -INT Valid Delay	10	16	10	16			1,2
5	TdTXC(REQ)	-Tx C to -W/-REQ Valid Delay	5	8	5	8			3
6	TdTXC(W)	-Tx C to Wait Inactive Delay	5	11	5	11			1,3
7	TdTXC(DRQ)	-Tx C to -DTR/-REQ Valid Delay	4	7	4	7			3
8	TdTXC(INT)	-Tx C to -INT Valid Delay	6	10	6	10			1,3
9	TdSY(INT)	-SYNC to -INT Valid Delay	2	6	2	6			1
10	TdEXT(INT)	-DCD or -CTS to -INT Valid Delay	2	6	2	6			1

General and System Timing Notes:

- Open-drain output, measured with open-drain test load.
- RxC is RTxC or TRxC, whichever is supplying the transmit clock.
- TxC is TRxC or RTxC, whichever is supplying the transmit clock.
- Both TrxC and SYNC have 30 pF capacitors connected to ground.
- Applies only if the data rate is one-fourth the PCLK rate. In all other cases, no phase relationship between RxC and PCLK or TxC and PCLK is required.
- Applies only to FM encoding/decoding.
- Applies only for transmitter and receiver; DPLL and baud rate generator timing are identical to chip PCLK requirements.
- Units are in nanoseconds (ns).



FIGURE 40. SYSTEM TIMING (SEE TABLE 3)



ABSOLUTE MAXIMUM RATINGS

Voltages on all pins with respect to GND -0.3V to 7.0V

Operating Ambient Temperature 0°C to +70°C

Storage Temperature -65°C to +150°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above

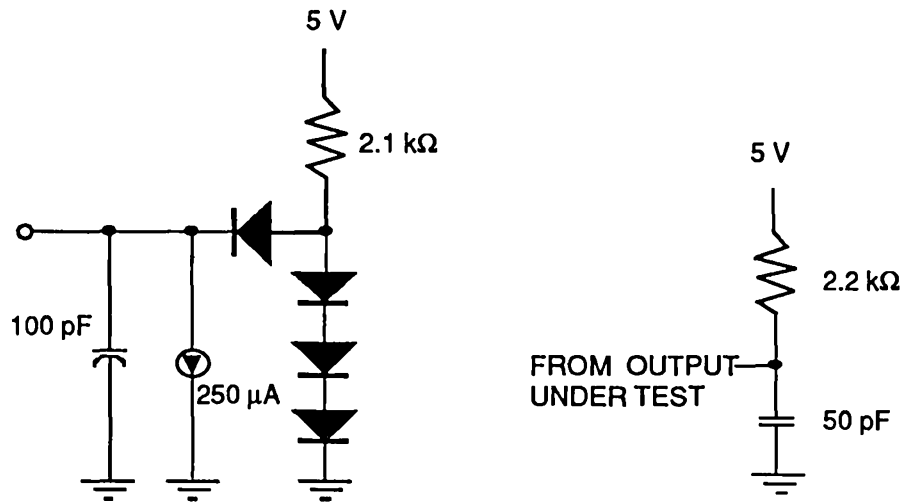
those listed on the operational sections of this specification is not implied and exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

STANDARD TEST CONDITIONS

The dc characteristics and capacitance section below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND. Positive current flows into the referenced pin.

Standard conditions are as follows:

- $+4.75\text{ V} \leq V_{CC} \leq +5.25\text{ V}$
- GND = 0 V
- TA as shown in Ordering Information


DC CHARACTERISTICS: $V_{CC} = 5\text{ V} \pm 5\%$, $T_A = 0^\circ\text{C}$ to 70°C

Symbol	Parameter	Min	Max	Unit	Conditions
V _{IH}	Input High Voltage	2.0	$V_{CC} + 0.3$	V	
V _{IL}	Input Low Voltage	-0.3	0.8	V	
V _{OH}	Output High Voltage	2.4		V	I _{OH} = -1.0 mA
V _{OH}	Output High Voltage	$V_{CC} - 0.8$		V	I _{OH} = -250 μA
V _{OL}	Output Low Voltage		0.4	V	I _{OH} = +2.0 mA
I _{IL}	Input Leakage		±10.0	μA	$0.4\text{ V} \leq V_{IN} \leq +2.4\text{ V}$
I _{OL}	Output Leakage		±10.0	μA	$0.4\text{ V} \leq V_{IN} \leq +2.4\text{ V}$
I _{CC}	VCC Supply Current		3.0	mA/MHz	See Note

Note: Add 0.5 mA quiescent current to determine total maximum VCC supply current. (Example: at 10 MHz clock frequency, the total maximum VCC supply current equals 30 mA plus 0.5 mA or 30.5 mA.)

CAPACITANCE: $T_A = 0^\circ\text{C}$ to 70°C , $f = 1\text{ MHz}$

Symbol	Parameter	Min	Max	Unit	Conditions
C _{IN}	Input Capacitance		10	pF	Unused Inputs Grounded
C _{OU}	Output Capacitance		15	pF	
C _{I/O}	Bidirectional Capacitance		20	pF	Unused Inputs Grounded

32-BIT RISC MICROPROCESSOR

FEATURES

- 32-bit internal architecture
- 32-bit external data bus
- 64M-byte linear address space
- Bus timing optimized for standard DRAM usage with page mode operation
- 40M-byte/second bus bandwidth
- Simple/powerful instruction set providing an excellent high level language compiler target
- Hardware support for virtual memory systems
- Low interrupt latency for real-time application requirements
- Full CMOS implementation results in low power consumption
- Single 5 V \pm 5% operation
- 84-pin JEDEC Type-B leadless chip carrier (PLCC)

DESCRIPTION

The VL86C010 Acorn RISC Machine (ARM) is a full 32-bit general-purpose microprocessor designed using reduced instruction set computer (RISC) methodologies. The processor is targeted for the microcomputer, graphics, industrial and controller markets for use in stand-alone or embedded systems. Applications in which the processor is useful include laser printers, graphics engines, N.C. machines and any other systems requiring fast real-time response to external interrupt sources and high processing throughput.

The VL86C010 features a 32-bit data bus, 27 registers of 32 bits each, a load-store architecture, a partially overlapping register set, 2.6 μ s worst-case interrupt latency, conditional instruction execution, a 26-bit linear address space and an average instruction execution rate of from four-to-five million instructions per second (MIPS). Additionally, the processor supports two addressing modes: program counter (PC) and base register relative modes. The ability to do pre- and post-indexing allows

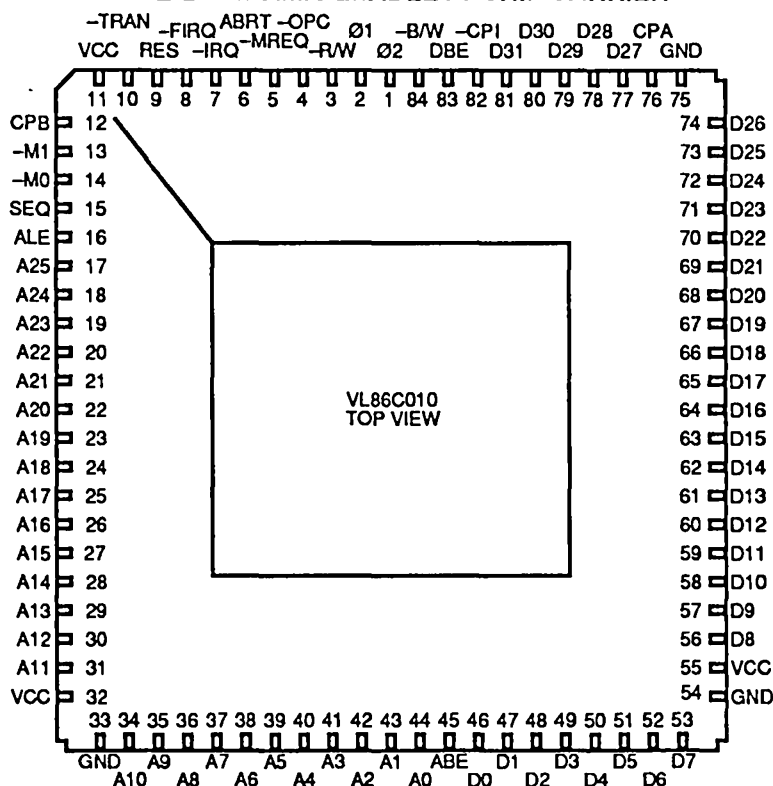
stacks and queues to be easily implemented in software. All instructions are 32 bits long (aligned on word boundaries), with register-to-register operations executing in one cycle. The two data types supported are 8-bit bytes and 32-bit words.

Using a load-store architecture simplifies the execution unit of the processor, since only a few instructions deal directly with memory and the rest operate register-to-register. Load and store multiple register instructions provide enhanced performance, making context switches faster and exploiting sequential memory access modes.

The processor supports two types of interrupts that differ in priority and register usage. The lowest latency is provided by the fast interrupt request (FIRQ) which is used primarily for I/O to peripheral devices. The other interrupt type (IRQ) is used for interrupt routines that do not demand low-latency service or where the overhead of a full context switch is small compared with the interrupt process execution time.

PIN DIAGRAM

JEDEC TYPE-B CERAMIC LEADLESS CHIP CARRIER



ORDER INFORMATION

Part Number	Clock Frequency	Package
VL86C010-10QC	10 MHz	Plastic Leaded Chip Carrier (PLCC)
VL86C010-10LC		JEDEC Type-B Ceramic Carrier
VL86C010-12QC	12 MHz	Plastic Leaded Chip Carrier (PLCC)
VL86C010-12LC		JEDEC Type-B Ceramic Carrier

Note: Operating temperature range is 0°C to +70°C

PLEASE CONSULT RISC FAMILY DATA MANUAL FOR DETAILED INFORMATION

RISC MEMORY CONTROLLER (MEMC)

FEATURES

- Drives up to 32 standard dynamic RAMs giving 4M bytes of real memory with 1M bit devices
- Logical-to-physical address translation (32M byte logical address space) supporting three protection levels:
 - Supervisor Mode
 - Operating System Mode
 - User Mode
- Uses fast page mode DRAM accesses to maximize bandwidth from commodity memories
- Internal DMA address generators for video, cursor and sound data buffers
- Various ROM speeds supported (access times of 450 ns, 325 ns, 200 ns)
- Provides all critical system timing including processor clocks, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, and DMA data transfer strobes
- Arbitrates memory between the processor and DMA systems

DESCRIPTION

The memory controller (MEMC) acts as the interface between the ARM (Acorn RISC Machine) processor and other functions in the system. The four circuits in the RISC family: MEMC, ARM, VIDE-video controller, and IOC-I/O controller, can be used to implement a small computer system. MEMC uses a single clock input to derive timing information for the other components.

In addition to providing interface signals to the other controllers, MEMC generates all the control signals for several access times of read-only memory (ROM) plus high-resolution timing and refresh control for dynamic RAM (DRAM). The controller outputs can drive up to 32 memory devices directly in a wide variety of configurations using various architectures of standard DRAMs. A logical-to-physical address translator maps the 4M byte physical memory into the 32M byte logical address space with three levels of protection.

Address translation is performed by a simple 128 entry content-addressable

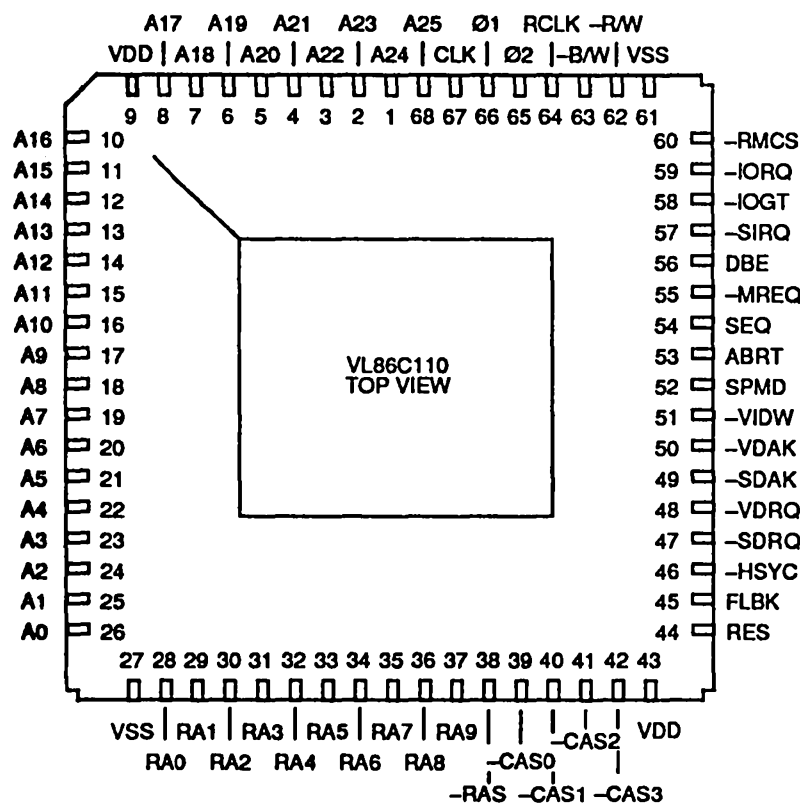
memory (CAM). MEMC provides a descriptor entry for every page of physical memory which eliminates descriptor thrashing (address translation misses) from degrading system performance.

The simple structure allows memory address translation to be performed without increasing required memory access time or decreasing the system clock. MEMC allows virtual memory and multi-tasking operations to be implemented without the usual performance degradation associated with each function. Fast page mode DRAM accesses are used to maximize memory bandwidth from inexpensive commodity memory devices.

MEMC supports direct memory access (DMA) read operations with three programmable address generators. Video refresh is performed using a circular buffer to enhance scrolling capability plus a separate linear buffer for a cursor sprite. Sound data uses a double buffering system.

PIN DIAGRAM

JEDEC TYPE-B CERAMIC LEADLESS CHIP CARRIER



ORDER INFORMATION

Part Number	Bus Clock Frequency	Package
VL86C110-08QC	8 MHz	Plastic Leaded Chip Carrier (PLCC)
VL86C110-08LC		JEDEC Type-B Ceramic Carrier

Note: Operating temperature range is 0°C to + 70°C.

PLEASE CONSULT RISC FAMILY DATA MANUAL FOR DETAILED INFORMATION

RISC VIDEO CONTROLLER (VIDC)

FEATURES

- Pixel rate selectable as 8, 12, 16, or 24 MHz
- Serializes data to 1-, 2-, 4-, or 8- bits per pixel
- 16 x 13 bit words - 4096 color lookup palette
- Three 4-bit DACs (one for each CRT gun)
- Fully programmable screen parameters
- Screen border in any of the 4096 possible colors
- Flexible cursor sprite
- Support for interlaced display format
- External synchronization capability
- Very high resolution monochrome mode support
- High quality stereo sound generation

DESCRIPTION

The Video Controller (VIDC) accepts video data from DRAM under DMA control, serializes and passes it through a color look-up palette, and converts it to analog signals for driving the CRT guns. The chip also controls all the display timing parameters plus the position and pattern of the cursor sprite. In addition, the VIDC includes an exponential DAC and stereo image table for the generation of high quality sound from data in the DRAM.

The VIDC requests data from the RAM when required, and buffers it in one of three first-in, first-out memories (FIFOs). Note that the addressing of the data in RAM is controlled elsewhere in the system (usually in the VL86C110 Memory Controller, MEMC). Data is requested in blocks of four 32-bit words, allowing efficient use of page-mode DRAM without locking up the system data bus for long periods.

The VIDC is a highly programmable device, offering a very wide choice of display formats. The pixel rate can be se-

lected in a range between 8 and 24 MHz and the data can be serialized to either 8-, 4-, 2-, or 1-bit per pixel. The horizontal timing parameters can be controlled to units of 2 pixels, and the vertical timing parameters can be controlled in units of a raster. The color lookup palette which drives the three on-chip DACs is 13 bits wide, offering a choice from 4096 colors or an external video source.

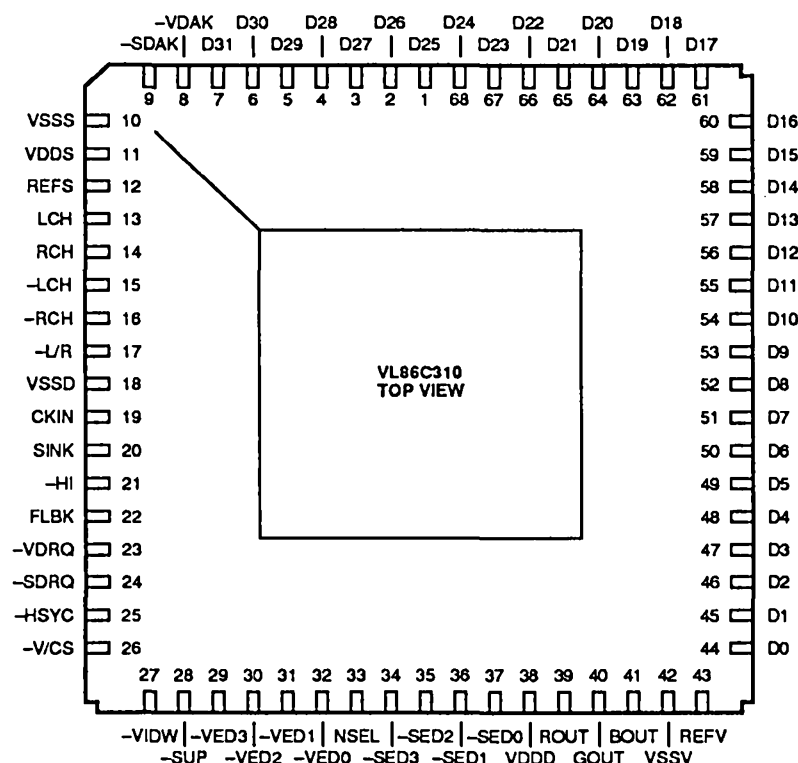
Extensive use is made of pipelining throughout the device.

The cursor sprite is 32 pixels wide, and any number of rasters high. Three simultaneous colors (from the 4096 possible) are supported, and any pixel can be defined as transparent, making possible cursors of many shapes. The cursor can be positioned anywhere on the screen.

The sound system implemented on the device can support up to eight channels, each with a separate stereo position.

PIN DIAGRAM

JEDEC TYPE-B CERAMIC LEADLESS CHIP CARRIER



ORDER INFORMATION

Part Number	Clock Frequency	Package
VL86C310-08QC	8 MHz	Plastic Leaded Chip Carrier (PLCC)
VL86C310-08LC		JEDEC Type-B Ceramic Carrier

Note: Operating temperature is 0°C to +70°C.

PLEASE CONSULT RISC FAMILY DATA MANUAL FOR DETAILED INFORMATION

FEATURES

- Power on reset control
- Four independent 16-bit programmable counters
 - Two timers
 - Two baud rate generators
- Bidirectional serial keyboard interface
- Six programmable bidirectional control pins
- Interrupt mask, request and status registers for –IRQ and –FIRQ
- 14 level triggered interrupt inputs
- Two edge triggered interrupt inputs
- Four programmable peripheral cycles
 - Slow
 - Medium
 - Fast
 - 2 MHz synchronous
- Seven external peripheral selects
- ARM/IO bus interface control
- Expansion bus buffer control

DESCRIPTION

The VL86C410 Input/Output Controller (IOC) is designed to interface to the VL86C010/VL86C110/VL86C310 chip set to provide a unified view of interrupts and peripherals within an Acorn RISC Machine (ARM) based computer. It controls an 8-to-32 bit I/O data bus to which on-board peripherals and any I/O expansions are connected. It provides a set of internal functions, which are accessed without wait states, and programmable speed access to external peripherals.

The VL86C410 provides system level I/O with six programmable control pins and a full-duplex, bidirectional serial keyboard interface. To support system timing requirements, the VL86C410 contains four independent programmable counters. Two of these counters are used as baud rate generators. One is dedicated to the keyboard and the other controls the BAUD output pin to

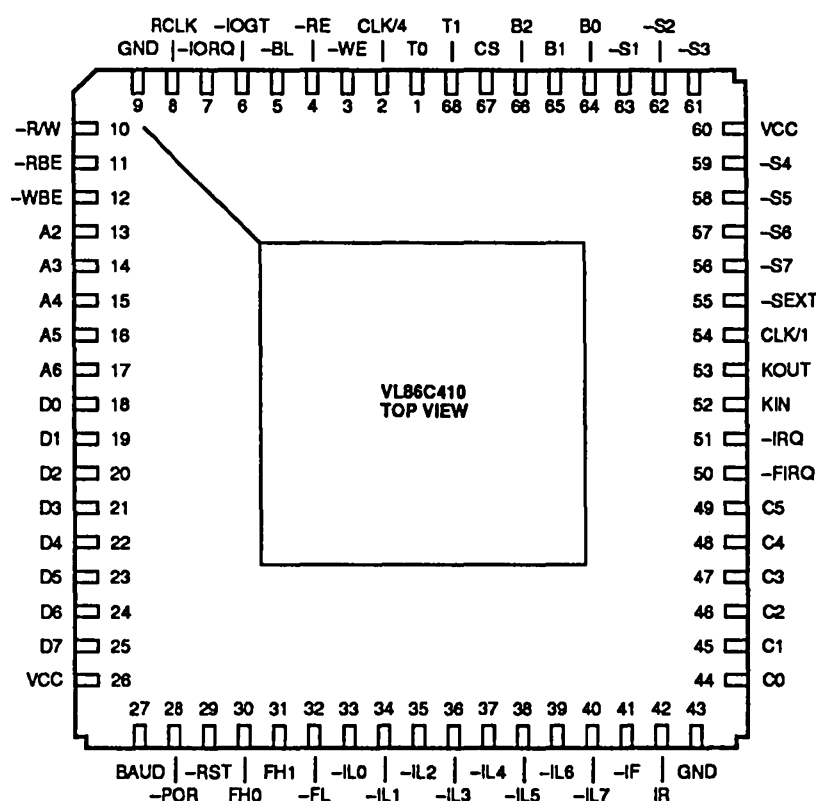
generate a free-running clock. The other two counters can be used to generate system timing events.

The IOC serves as the interface between the very high-speed RISC system bus and the slower I/O or expansion bus. The part provides all the buffer control required between the two buses. The VL86C410 supports an interruptable I/O cycle that allows the system to use slower, low-cost peripheral controllers such as the VL16C450 Asynchronous Communications Element and VL1772 Floppy Disk Controller without severe latency on the system bus.

Peripheral controllers are supported with 16 interrupt inputs (14 level sensitive and two edge-triggered), seven peripheral select outputs, and four programmable I/O cycle times.

PIN DIAGRAM

JEDEC TYPE-B CERAMIC LEADLESS CHIP CARRIER



ORDER INFORMATION

Part Number	Clock Frequency	Package
VL86C410-08QC	8 MHz	Plastic Leaded Chip Carrier (PLCC)
VL86C410-08LC		JEDEC Type-B Ceramic Carrier

Note: Operating temperature is 0°C to +70°C.

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